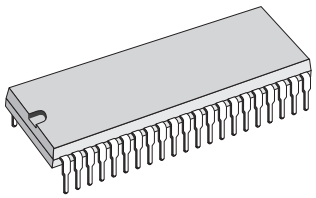
SGS-THOMSON MICROELECTRONICS

TDA8205

NICAM QPSK DEMODULATOR

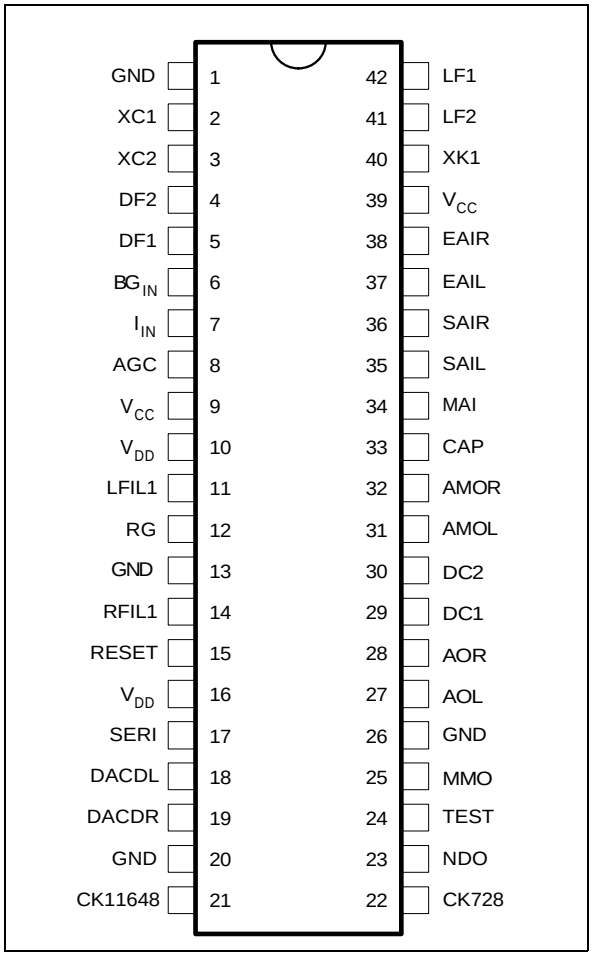
- HIGHLY INTEGRATED TWO CHIP SOLUTION FOR NICAM DEMODULATION (using TDA8204 decoder)
- AUTOMATIC DUAL STANDARD DEMODULATION 6.552MHz FOR I SYSTEM 5.85MHz FOR B/G SYSTEM
- 40dB RANGE AGC
- SINGLE CRYSTAL OPERATION
- NICAM 728 DATA AND CLOCK RECOVERY
- LOW PASS FILTER FOR PWM CODED AUDIO SIGNALS AND J-17 DE-EMPHASIS
- AUTOMATIC FM MONO SELECTION BY RESERVE SOUND SWITCH FUNCTION
- VERSATILE AUDIO SWITCHING MATRIX
- AUTOMATIC MUTE FUNCTION



SHRINK 42
(Plastic Package)

ORDER CODE : TDA8205

PIN CONNECTIONS



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DESCRIPTION

The TDA8205 is essentially divided into two signal processing sections. The first section handles all the NICAM signal acquisition, the QPSK demodulator and clock and data recovery circuits. The key point to note about this section is the dual frequency synthesiser. By use of only one quartz crystal, the IC is able to demodulate QPSK signals from either system I or system B/G in an automatic way. The second section of the TDA8205 manages the analog parts of the twin digital-to-analog converters (DACs) and all filtering and audio switching downstream of the DACs. A simple serial bus from the TDA8204 allows control of the switch functions by the CTV system microcontroller.

PIN ASSIGMENT

Pin No	Pin Name	Function	Pin No	Pin Name	Function
1	GND	Ground	22	CK728	728kHz Clock Intput
2	XC1	Optional Crystal	23	NDO	NICAM Data Output
3	XC2	Optional Crystal	24	TEST	To be connected to GND
4	DF2	Data Filter 2 (eye monitor)	25	MMO	Matrix Mute Out
5	DF1	Data Filter 1 (eye monitor)	26	GND	Ground
6	BG_{IN}	System B/G Input	27	AOL	Audio Output Left
7	I_{IN}	System I Input	28	AOR	Audio Output Right
8	AGC	AGC Filter Capacitor	29	DC1	Decoupling 1
9	V_{CC}	+12V Supply	30	DC2	Decoupling 2
10	V_{DD}	+5V Supply	31	AMOL	Audio Mutable Output Left
11	LFIL1	Left Filter 1 (J-17 De-emphasis)	32	AMOR	Audio Mutable Output Right
12	RG	Gain Setting Resistor for DAC	33	CAP	Decoupling Capacitor
13	GND	Ground	34	MAI	Mono Audio Input
14	RFIL1	Right Filter 1 (J-17 De-emphasis)	35	SAIL	Stereo Audio Input Left
15	RESET	Reset Chip	36	SAIR	Stereo Audio Input Right
16	V_{DD}	+5V Supply	37	EAIL	External Audio Input Left
17	SERI	Interchip Serial Bus Input	38	EAIR	External Audio Input Right
18	DACDL	DAC Data Left Input	39	V_{CC}	+12V Supply
19	DACDR	DAC Data Right Input	40	XK1	11.648MHz Crystal
20	GND	Ground	41	LF2	Loop Filter 2
21	CK11648	11.648MHz Clock Output	42	LF1	Loop Filter 1

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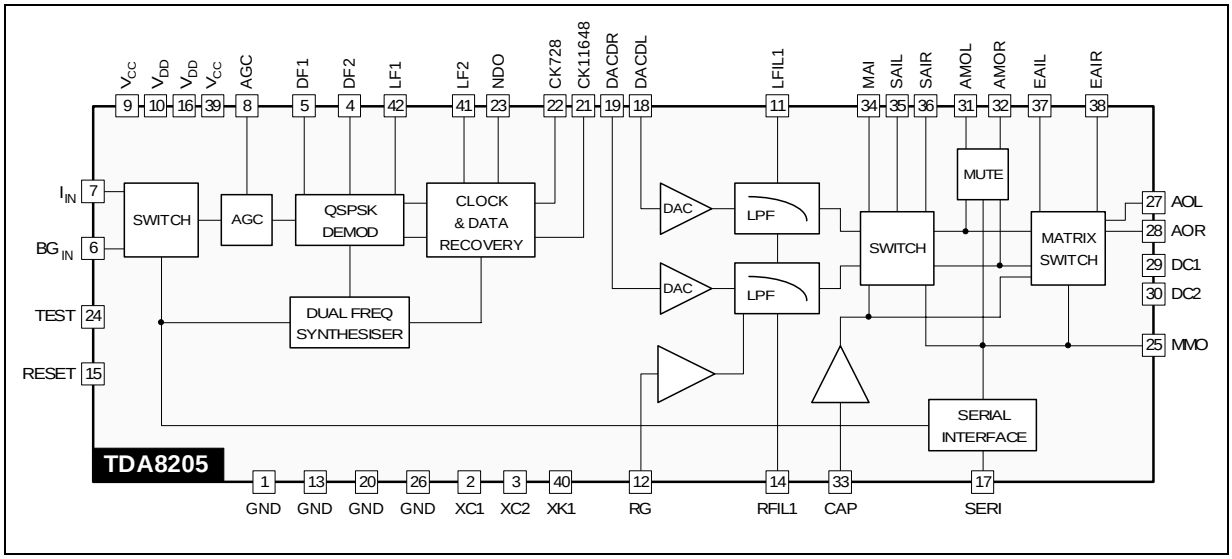
BLOCK DIAGRAM



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BLOCK DIAGRAM DESCRIPTION

The QPSK signal enters the IC via two inputs after passing through two external bandpass filters at the relevant frequencies of 6.552MHz and 5.85MHz for system I and B/G respectively. The two inputs enter a source selection switch and pass immediately to an AGC block which has a total range of 40dB. The resulting levelled signal passes to the QPSK demodulator which recovers the NICAM 728Kb/s data stream by means of carrier and clock recovery circuits.

Carrier recovery is achieved with a baseband remodulator which consists of a phase locked loop with a switchable phase detector. This allows it to lock to one of four possible phases of the QPSK

carrier without disruption due to the modulation. Dual frequency operation is made possible by synthesising the carrier reference frequency thus saving the need for two extra crystals. Dual VCXO can also be software selected (SYN bit of CR3 in TDA8204) with external crystal (Pin XC1/XC2) for new standards. Selection between XC1 and XC2 is done with bit "IBG" in CR3 register of TDA8204 (IBG = 0 XC1 selected, IBG = 1 XC2 selected).

The standards switch controls operation of the QSPK demodulator at either 6.552MHz or 5.85MHz. This can be controlled via the I^2C bus or the decoder set into automatic mode in which it determines the standard by alternately trying to lock to the two systems.

On chip low pass filters recover the in-phase and quadrature data channels which are then sliced by comparators. The symbol clock is recovered from this data and used to sample and re-time it. The two data channels are then decoded and serialized to obtain the NICAM-728 data which is then passed on to the NICAM decoder in the TDA8204.

After processing the NICAM into a digital bit-stream in the TDA8204, the data is passed back to the TDA8205 for the analog functions of the DACs to be performed.

Conversion of the pulse width modulated bit streams to analog takes place and is followed by low pass filtering which removes high frequency quantising noise and performs J-17 de-emphasis. The DACs signal level can be adjusted to match the reserve sound signal level.

$1V_{RMS}$ maximum on Pins LFIL1/RFIL1 can be obtained by selection of appropriate resistor on Pin RG.

Once the analog audio has been recovered, certain source switch functions are performed. If the NICAM signal fails and if the reserve sound flag (C4), of SRO register, is set the reserve sound switch automatically selects Mono Audio Input. If the reserve sound flag (C4) is reset, the reserve sound switch will not change and the audio outputs will be muted (DAC outputs muted).

If the NICAM signal only carries data, Mono Audio Input is selected. The reserve sound switch can be forced to select Mono Audio Input via I^2C bus, using Bit FS0 = 1 and FS1 =0 of CR3 Register.

This can be used in the case of NICAM marginal reception. To select Stereo Left and Right Audio Input Bit FS0 = 0 and FS1 = 1 of CR3 Register must be selected. The outputs from this reserve sound switch are available on Audio mutable output left and right, and are internaly connected to the audio matrix.

A simple audio switching matrix is provided internally for flexible control over the audio source and destination selection.

Audio signal left and right coming from the reserve sound switch and the external audio input left and right can be switched to the audio outputs left and right .

DAC and auxiliary audio outputs can be muted. An additional +6dB gain can be applied to raise the output levels to $2V_{RMS}$ maximum. For more information see Software Specification chapter (III.5.3/TDA8204).

The DAC outputs are automatically muted under the following conditions

- loss of frame alignement
- the bit error rate (Ber) is > error rate limit
- NICAM signal is conveying M1 only. The right DAC is muted unless M1 has been selected to be on both DAC outputs.
- NICAM signal is conveying data only.

For test purposes, the DAC outputs can be unmuted by forcing the bi-directional mute Pin 25 of TDA8204 or via I^2C bus.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
V_{DD}	Supply Voltage	7	V
P_{tot}	Total Power Dissipation	1.2	W
T_{oper}	Operating Temperature Range	0, + 70	^oC
T_{stg}	Storage Temperature Range	-20, + 150	^oC

8205-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-Ambient	Max.	67	$^oC/W$

8205-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{CC}	Supply Voltage Range	11.4	12	12.6	V
V_{DD}	Supply Voltage Range	4.75	5	5.25	V
I_{CC}	Supply Current	18	36	50	mA
I_{DD}	Supply Current	10	18	42	mA
DIGITAL PINS					
OUTPUTS					
	CK11, NDO				
V_{OL}	Low Level Output Voltage (I = -4mA)			0.4	V
V_{OH}	HIgh Level Output Voltage (I = 4mA)	0.7 V_{DD}			V
	MMO (open collector)				
V_{OL}	Low Level Output Voltage (I = -1mA)			0.4	V
I_{LK}	High Level Output Current (leakage)			± 2	µA
INPUTS					
	SERI, DACDL, DACDR, CK728				
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
ANALOG PINS					
I-B/G SELECTOR					
V_{DC}	DC Bias Voltage		2.8		V
R_{IN}	Input Resistance		10		kΩ
C_{IN}	Input Capacitance		10		pF
AGC					
V_{IN}	Input Voltage Range	10	200	1000	mV_{PP}
AGClv	AGC Low Voltage (V_{IN} = $1V_{PP}$)		2		V_{PP}
AGChv	AGC High Voltage (V_{IN} = $10mV_{PP}$)		11		V
AGCta	AGC Attack Time (V_{IN} = 10mV to 1V, C_{AGC} = 100nF)		15		ms
AGCtd	AGC Decay Time (V_{IN} = 1V to 10mV, C_{AGC} = 100nF)		220		ms
QPSK DEMODULATOR (LF1)					
V_{DC}	DC Bias Voltage (SYN = 1)	1	5	10	V
Kd	Phase Detector Constant (no mod.)		33		µA/rad
kv	VCO Constant		3.5		MHz/V
EYE DIAGRAM MONITORS (DF1, DF2)					
V_{DC}	DC Bias Voltage		2.5		V
R_{OUT}	Output Resistance		1.2		kΩ
V_{OUT}	Output Voltage (System I)		0.6		V_{PP}
CLOCK AND DATA RECOVERY (LF2)					
V_{DC}	DC Bias Voltage		2.5		V
Kd	Phase Detector Constant (all 1's)		7		µA/rad
kv	VCXO Constant		4.4		kHz/V

8205-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC AND FILTER (LFIL1, RFIL1)					
V_{DC}	DC Bias Voltage		2.5		V
I_{OUT}	Output Current (R_G = 5.6kΩ, DAC full scale)		340		μA_{PP}
V_{RG}	RG Pin DC Voltage		1.25		V
AUDIO MATRIX (AOL, AOR, AMOL, AMOR)					
	DAC SELECTED				
V_{OUT}	Output Voltage (1kHz at -11.75dB, J17 de-emphasis, R_G = 5.6kΩ)	0.39	0.5	0.63	V_{RMS}
S/N	Relative to $0.5V_{RMS}$, noise measured with IEC-179 A-filter	60	70		dB
THD	1kHz at $0.5V_{RMS}$, R_G = 5.6kΩ		0.05	0.2	%
	Crosstalk at 1kHz, $0.5V_{RMS}$		65		dB
Chm	Maximum Channel Matching Error			2	dB
	MONO OR STEREO AUDIO INPUT SELECTED (MAI, SAIL, SAIR)				
S/N	Relative to $0.5V_{RMS}$, noise measured with IEC-179 A-filter		88		dB
THD	1kHz at $0.5V_{RMS}$		0.02		%
	STEREO AUDIO INPUT SELECTED				
	Crosstalk at 1kHz, $0.5V_{RMS}$		75		dB
Chm	Maximum Channel Matching Error			2	dB

8205-05.TBL

APPLICATION DIAGRAMS

Figure 1 : Stand Alone Application (I standard)

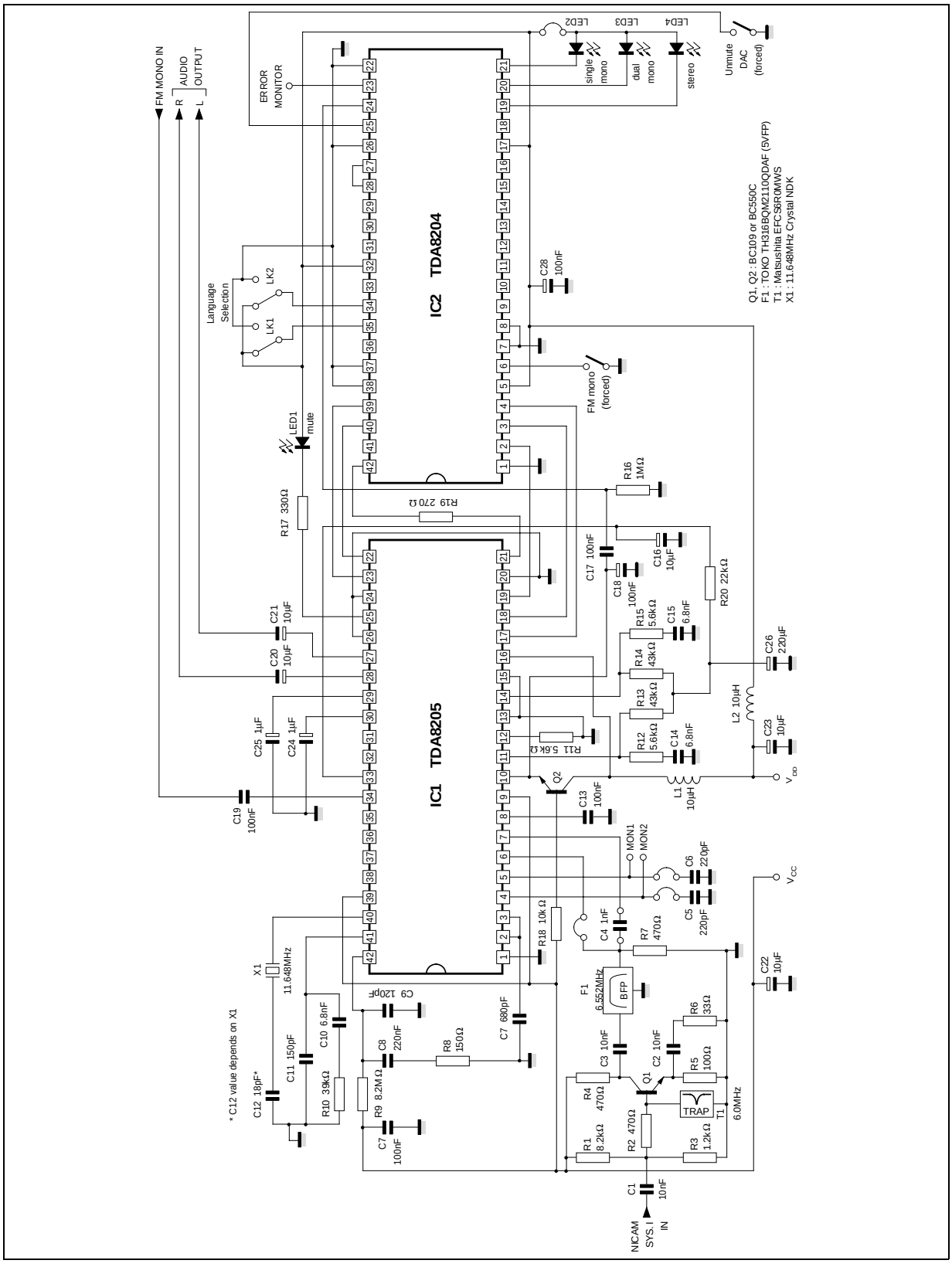
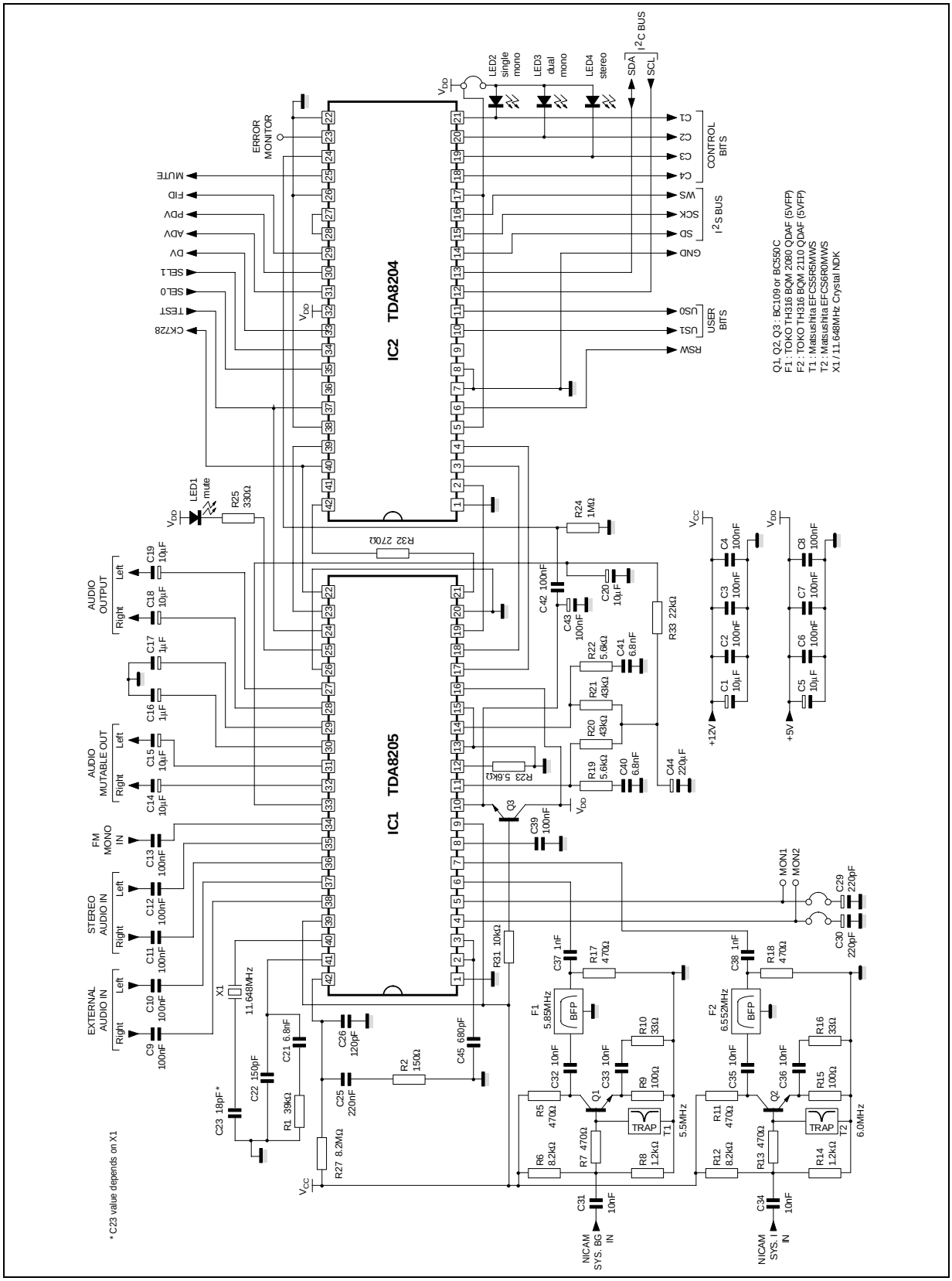
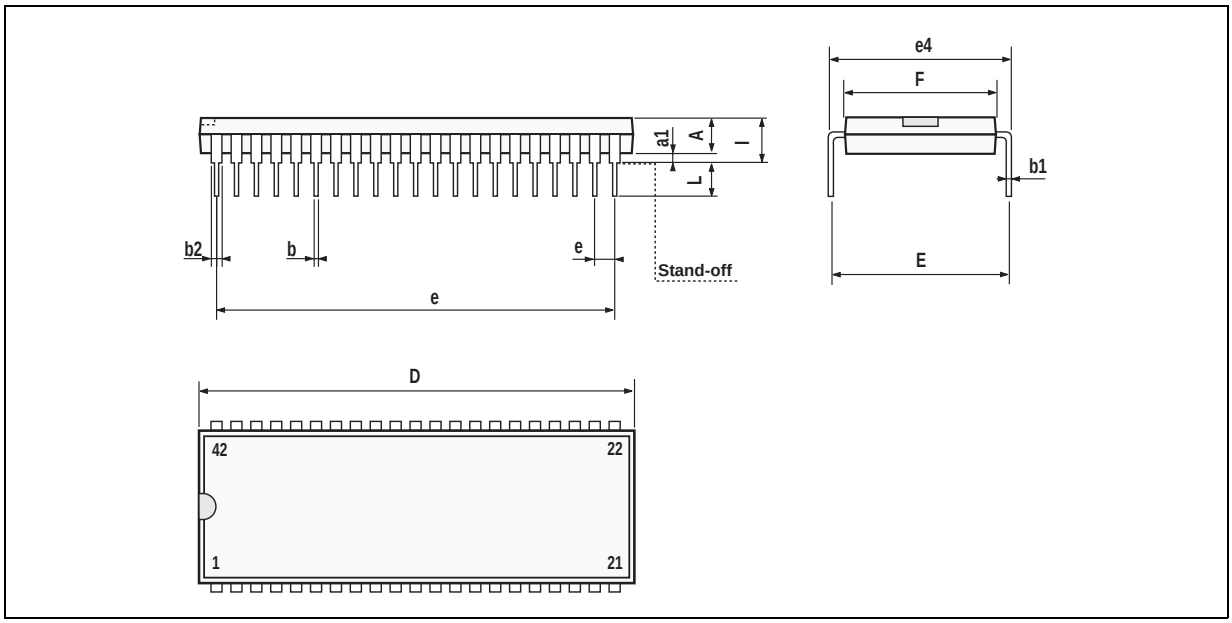


Figure 2 : I²C Bus Controlled Application (I and B/G standard)



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK



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Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

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