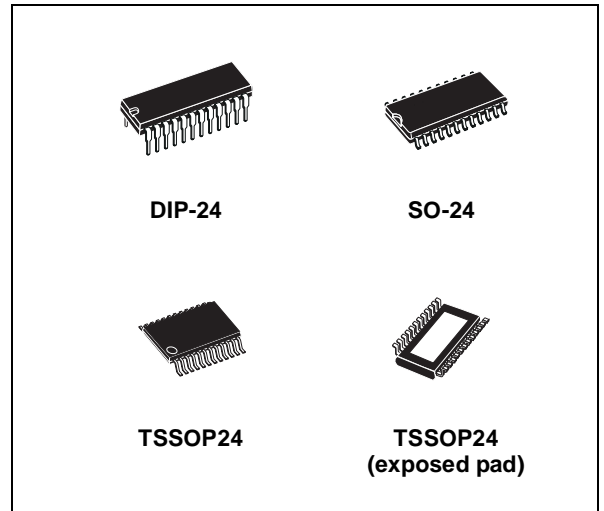




STP16CL596

LOW VOLTAGE 16-BIT CONSTANT CURRENT LED SINK DRIVER

- LOW VOLTAGE POWER SUPPLY DOWN TO 3V
- 16 CONSTANT CURRENT OUTPUT CHANNELS
- ADJUSTABLE OUTPUT CURRENT THROUGH EXTERNAL RESISTOR
- SERIAL DATA IN/PARALLEL DATA OUT
- SERIAL OUT CHANGES STATE ON THE FALLING EDGES OF CLOCK
- 3.3V MICRO DRIVER-ABLE
- OUTPUT CURRENT: 15-90 mA
- 25 MHz CLOCK FREQ.
- AVAILABLE IN HIGH THERMAL EFFICIENCY TSSOP EXPOSED PAD



DESCRIPTION

The STP16CL596 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CL596 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources were designed to provide 15-90mA constant current to drive the LEDs.

Compared with the STPIC6C595, the device provides great flexibility and improved performance in LED panel system design.

Through an external resistor, users can adjust the STP16CL596 output current, controlling in this way the light intensity of LEDs.

The STP16CL596 guarantees a 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 25 MHz, also satisfies the system requirement of high volume data transmission. The 3.3V of voltage supply is well useful for applications that interface any micro from 3.3V. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

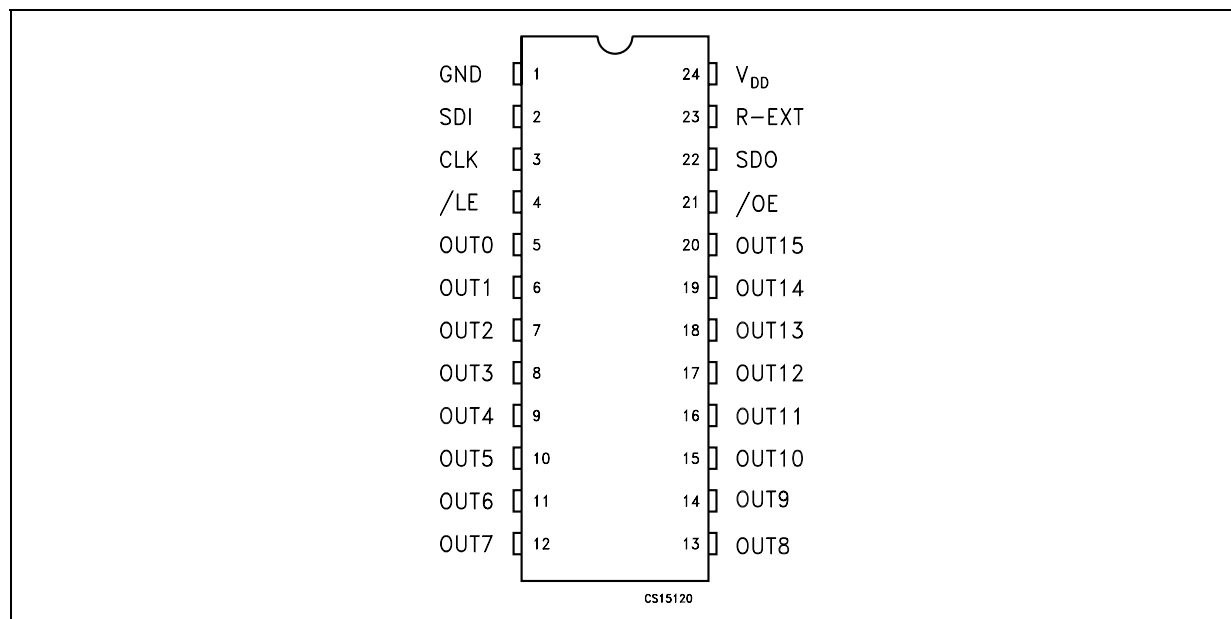
Table 1: Order Codes

Part Number	Package	Comments
STP16CL596B1R	DIP-24	15 parts per tube
STP16CL596M	SO-24 (Tube)	40 parts per tube
STP16CL596MTR	SO-24 (Tape & Reel)	1000 parts per reel
STP16CL596TTR	TSSOP24 (Tape & Reel)	2500 parts per reel
STP16CL596XTTR	TSSOP24 Exposed-Pad (Tape & Reel)	2500 parts per reel

Table 2: Current Accuracy

Output Voltage	Current accuracy		Output Current
	Between bits	Between ICs	
$\geq 0.7V$	$\pm 3\%$	$\pm 10\%$	15 to 90 mA

Figure 1: Pin Connection (Note 1)



Note 1: The exposed Pad is electrically not connected.

Table 3: Pin Description

PIN N°	Symbol	Name and Function
1	GND	Ground Terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	/LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	/OE	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V _{DD}	Supply voltage terminal

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	0 to 7	V
V_O	Output Voltage	-0.5 to 16	V
I_O	Output Current	90	mA
V_I	Input Voltage	-0.4 to $V_{DD}+0.4$	V
I_{GND}	GND Terminal Current	1440	mA
f_{CLK}	Clock Frequency	25	MHz
T_{OPR}	Operating Temperature Range	-40 to +125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Under these conditions, functional operation is not implied.

Table 5: Thermal Data

Symbol	Parameter	DIP-24	SO-24	TSSOP24	TSSOP24 (*) (exposed pad)	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient	60	75	85	37.5	°C/W

(*) The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

Table 6: Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_O	Output Voltage				16.0	V
I_O	Output Current	OUTn	5		90	mA
I_{OH}	Output Current	SERIAL-OUT			+1	mA
I_{OL}	Output Current	SERIAL-OUT			-1	mA
V_{IH}	Input Voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
V_{IL}	Input Voltage		-0.3		$0.3V_{DD}$	V
t_{wLAT}	/LE Pulse Width	$V_{DD} = 3.0$ to $3.6V$	20			ns
t_{wCLK}	CLK Pulse Width		20			ns
t_{wEN}	/OE Pulse Width		400			ns
$t_{SETUP(D)}$	Setup Time for DATA		20			ns
$t_{HOLD(D)}$	Hold Time for DATA		15			ns
$t_{SETUP(L)}$	Setup Time for LATCH		15			ns
f_{CLK}	Clock Frequency	Cascade Operation			25	MHz

Table 7: Electrical Characteristics ($V_{DD}=3V$, $T = 25^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage High Level		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input Voltage Low Level		GND		$0.3V_{DD}$	V
I_{OH}	Output Leakage Current	$V_{OH} = 16 V$			10	μA
V_{OL}	Output Voltage (Serial-OUT)	$I_{OL} = 1mA$			0.4	V
V_{OH}	Output Voltage (Serial-OUT)	$I_{OH} = -1mA$	$V_{DD}-0.4V$			V
I_{OL1}	Output Current	$V_O = 0.7V$ $R_{EXT} = 910 \Omega$	19.2	20.6	22.0	mA
I_{OL2}		$V_O = 0.7V$ $R_{EXT} = 360 \Omega$	46.2	50.5	54.0	mA
ΔI_{OL1}	Output Current Error between bit (All Output ON)	$V_O = 0.7V$ $R_{EXT} = 910 \Omega$		± 4	± 5	%
ΔI_{OL2}		$V_O = 0.7V$ $R_{EXT} = 360 \Omega$		± 3	± 4	%
$R_{SIN(up)}$	Pull-up Resistor		150	300	600	K Ω
$R_{SIN(down)}$	Pull-down Resistor		100	200	400	K Ω
$I_{DD(OFF1)}$	Supply Current (OFF)	$R_{EXT} = OPEN$ OUT 0 to 15 = OFF		0.3	0.6	mA
$I_{DD(OFF2)}$		$R_{EXT} = 470 \Omega$ OUT 0 to 15 = OFF		5.5	7.7	
$I_{DD(OFF3)}$		$R_{EXT} = 250 \Omega$ OUT 0 to 15 = OFF		10.1	14.1	
$I_{DD(ON1)}$	Supply Current (ON)	$R_{EXT} = 470 \Omega$ OUT 0 to 15 = ON		5.5	7.7	
$I_{DD(ON2)}$		$R_{EXT} = 250 \Omega$ OUT 0 to 15 = ON		10.1	14.1	

Table 8: Switching Characteristics ($V_{DD}=3V$, $T = 25^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation Delay Time, CLK-OUTn, /LE = H, /OE = L	$V_{DD} = 3 V$ $V_{IH} = V_{DD}$		250	280	ns
t_{PLH2}	Propagation Delay Time, /LE-OUTn, /OE = L	$V_{IL} = GND$ $C_L = 13pF$		220	250	ns
t_{PLH3}	Propagation Delay Time, /OE-OUTn, /LE = H	$I_O = 40mA$ $V_L = 3 V$		200	250	ns
t_{PLH}	Propagation Delay Time, CLK-SDO	$R_{EXT} = 470 \Omega$ $R_L = 65 \Omega$		25	50	ns
t_{PHL1}	Propagation Delay Time, CLK-OUTn, /LE = H, /OE = L			25	50	ns
t_{PHL2}	Propagation Delay Time, /LE-OUTn, /OE = L			25	50	ns
t_{PHL3}	Propagation Delay Time, /OE-OUTn, /LE = H			50	70	ns
t_{PHL}	Propagation Delay Time, CLK-SDO			25	50	ns
t_r	Output Rise Time			200	250	ns
t_f	Output Fall Time			17	25	ns

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

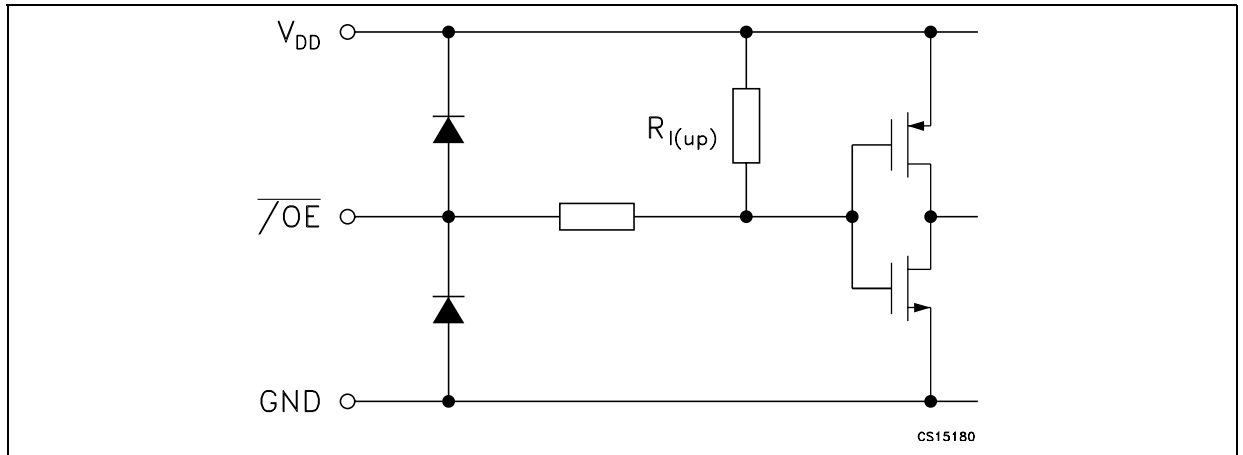
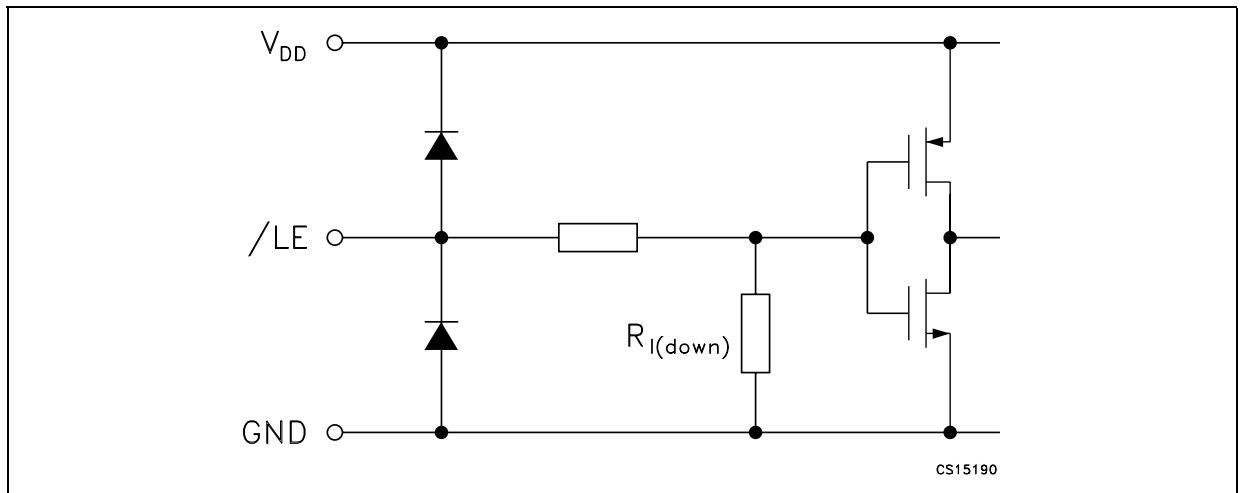
Figure 2: \overline{OE} TerminalFigure 3: \overline{LE} Terminal

Figure 4: CLK, SDI Terminal

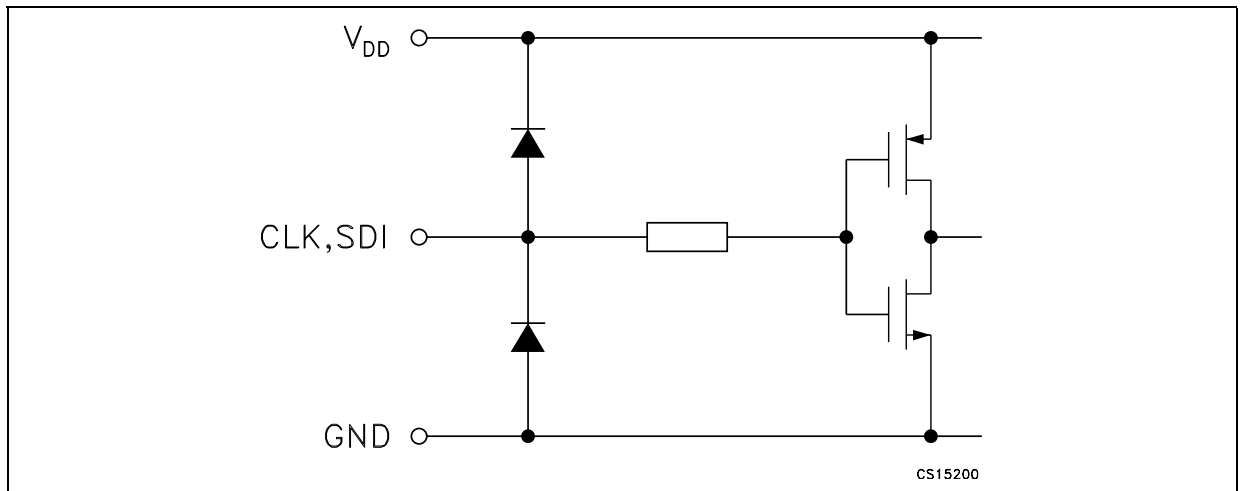


Figure 5: SDO Terminal

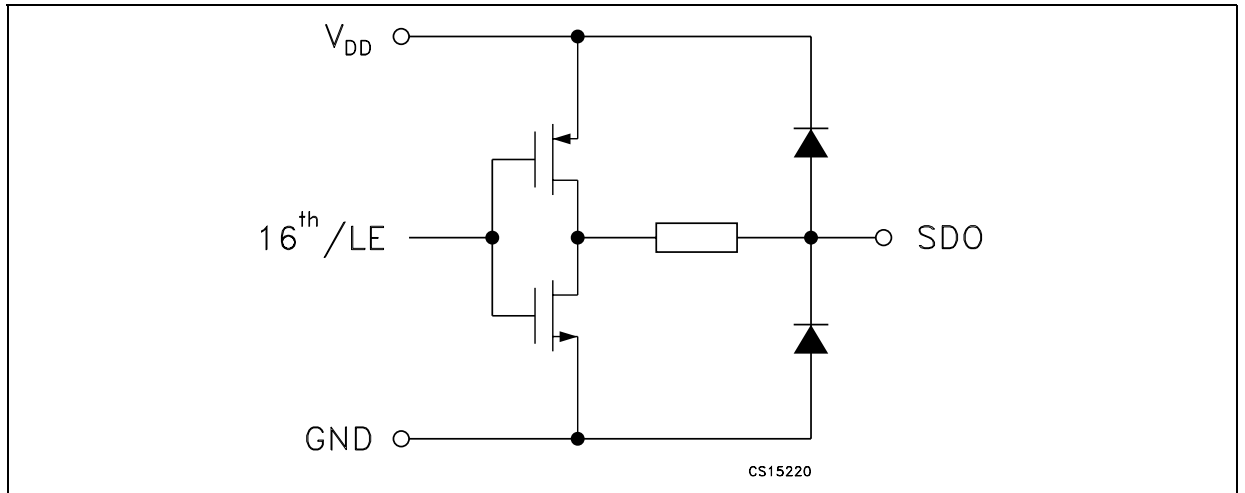


Figure 6: Block Diagram

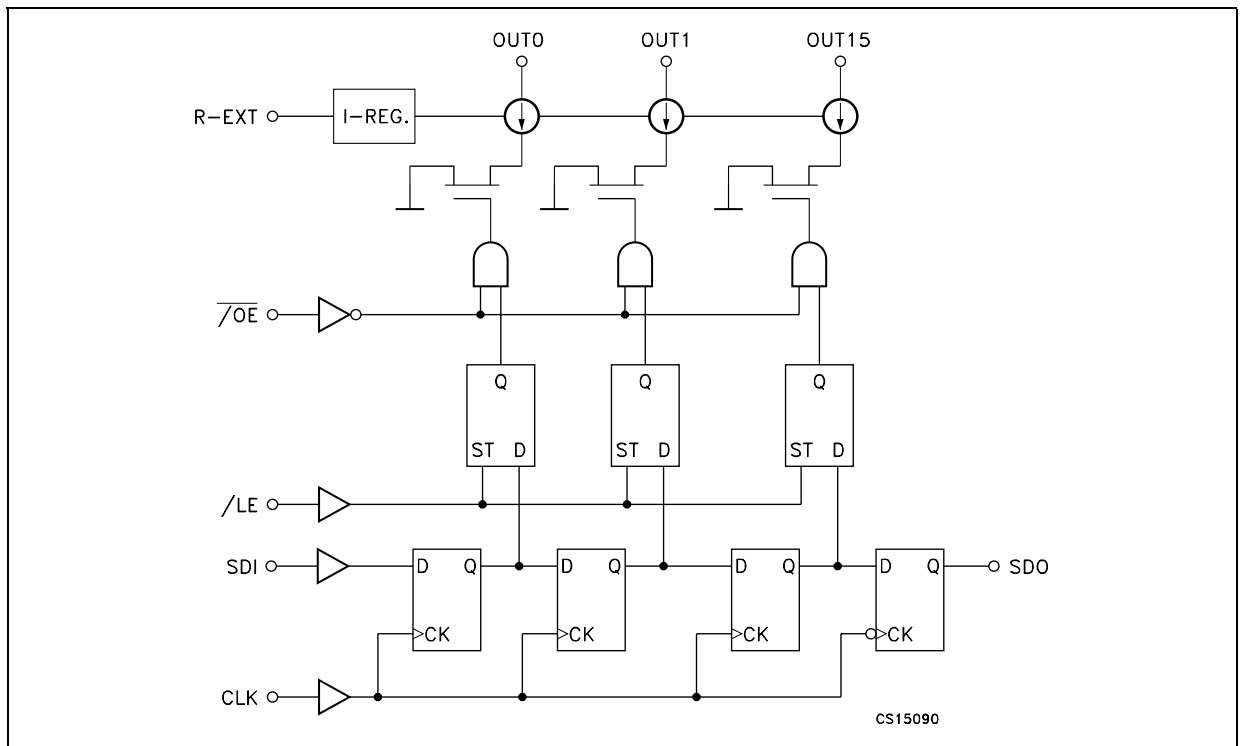
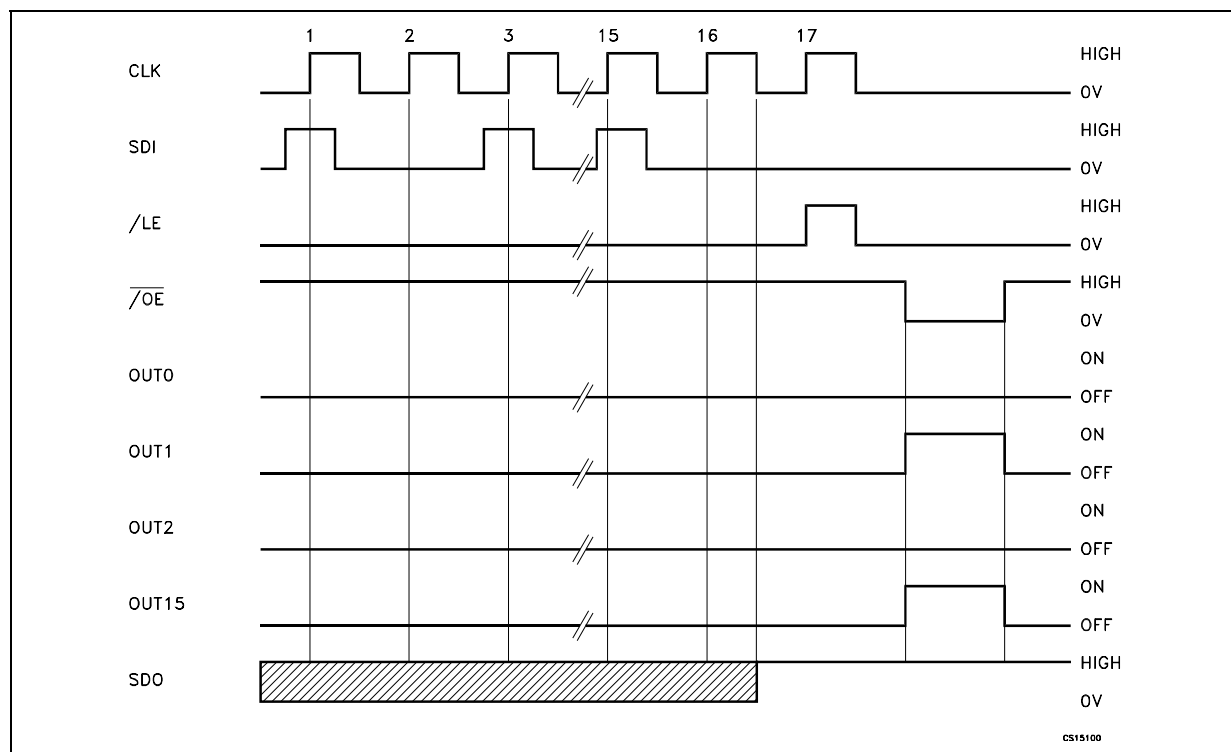


Table 9: Truth Table

CLOCK	/LE	/OE	SERIAL-IN	OUT0 OUT7 OUT15	SDO
	H	L	Dn	Dn Dn - 7 Dn -15	Dn - 15
	L	L	Dn + 1	No Change	Dn - 14
	H	L	Dn + 2	Dn - 2 Dn - 5 Dn -13	Dn - 13
	X	L	Dn + 3	Dn - 2 Dn - 5 Dn -13	Dn - 13
	X	L	Dn + 3	OFF	Dn - 13

Note 1: OUT0 to OUT15 = ON when Dn = H; OUT0 to OUT15 = OFF when Dn = L.

Figure 7: Timing Diagram



Note: The latches circuit holds data when the LE terminal is Low.

When LE terminal is at High level, latch circuit doesn't hold the data it passes from the input to the output.

When OE terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.

When OE terminal is at High level, it switches off all the data on the output terminal.

Figure 8: Clock, Serial-in, Serial-out

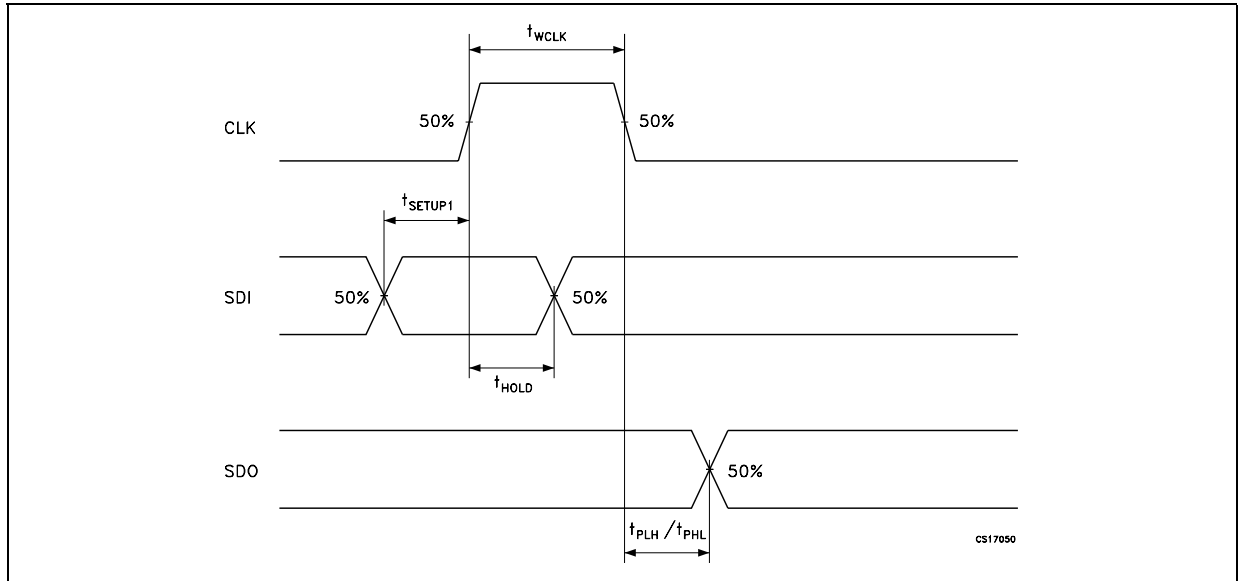


Figure 9: Clock, Serial-in, Latch, Enable, Outputs

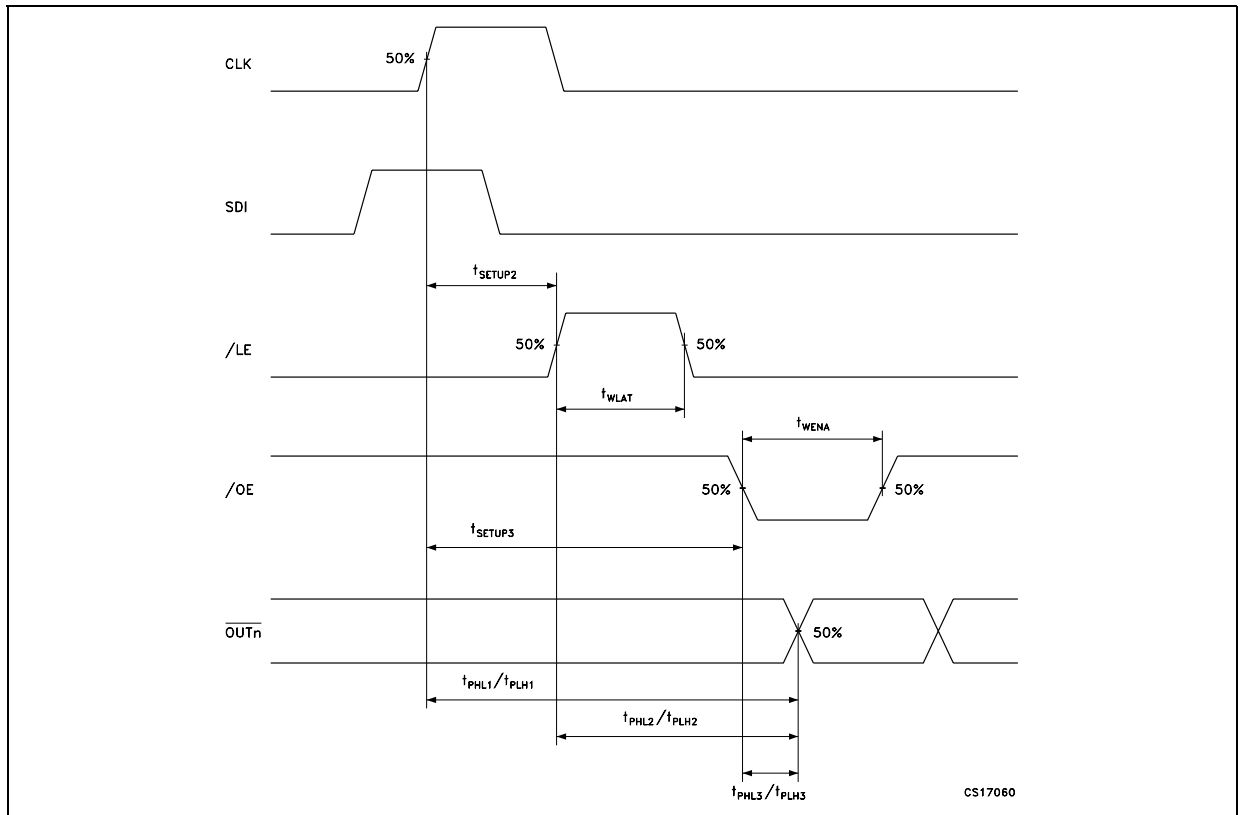
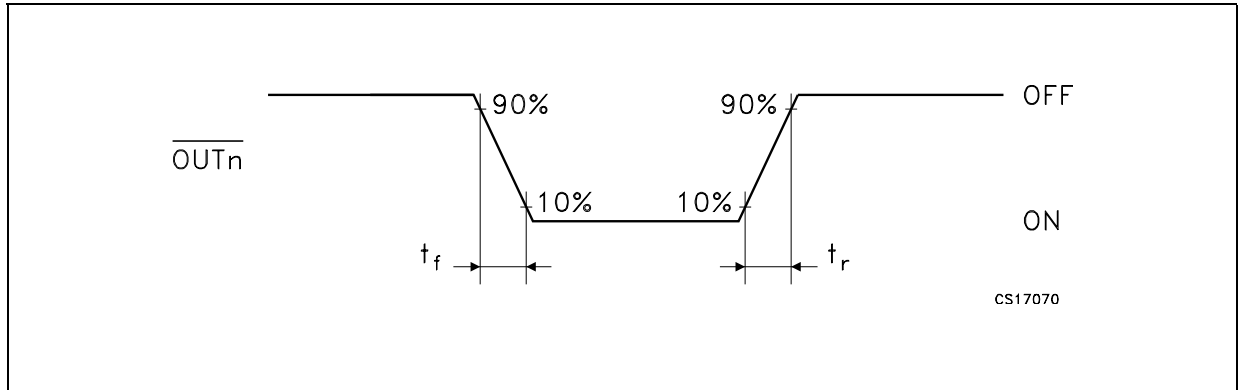


Figure 10: Outputs



TEST CIRCUIT

Figure 11: DC Characteristic

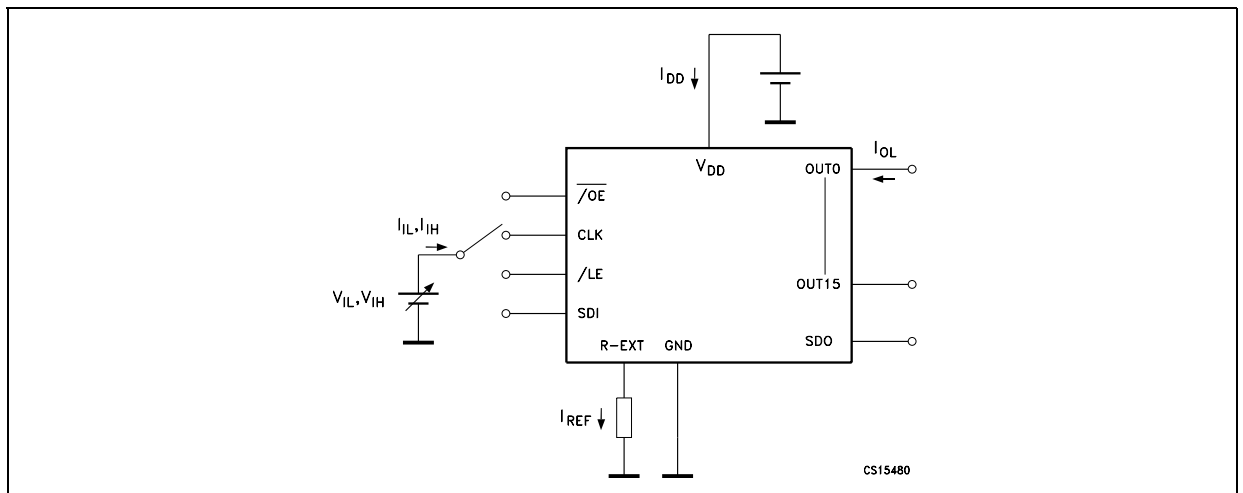


Figure 12: AC Characteristic

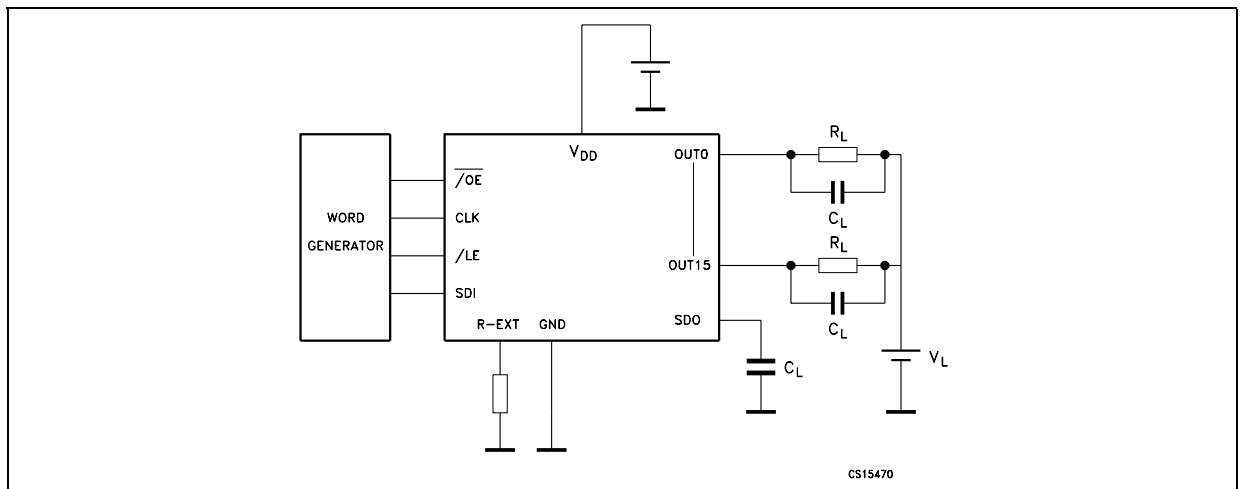


Figure 13: Output Current- R_{EXT} Resistor

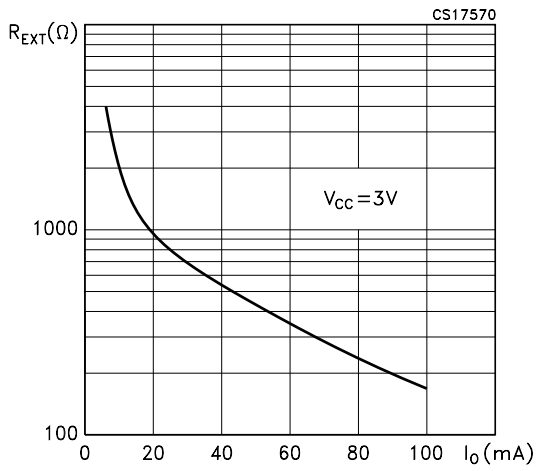
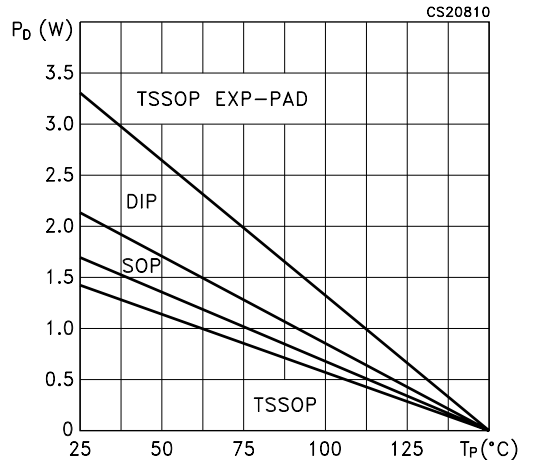
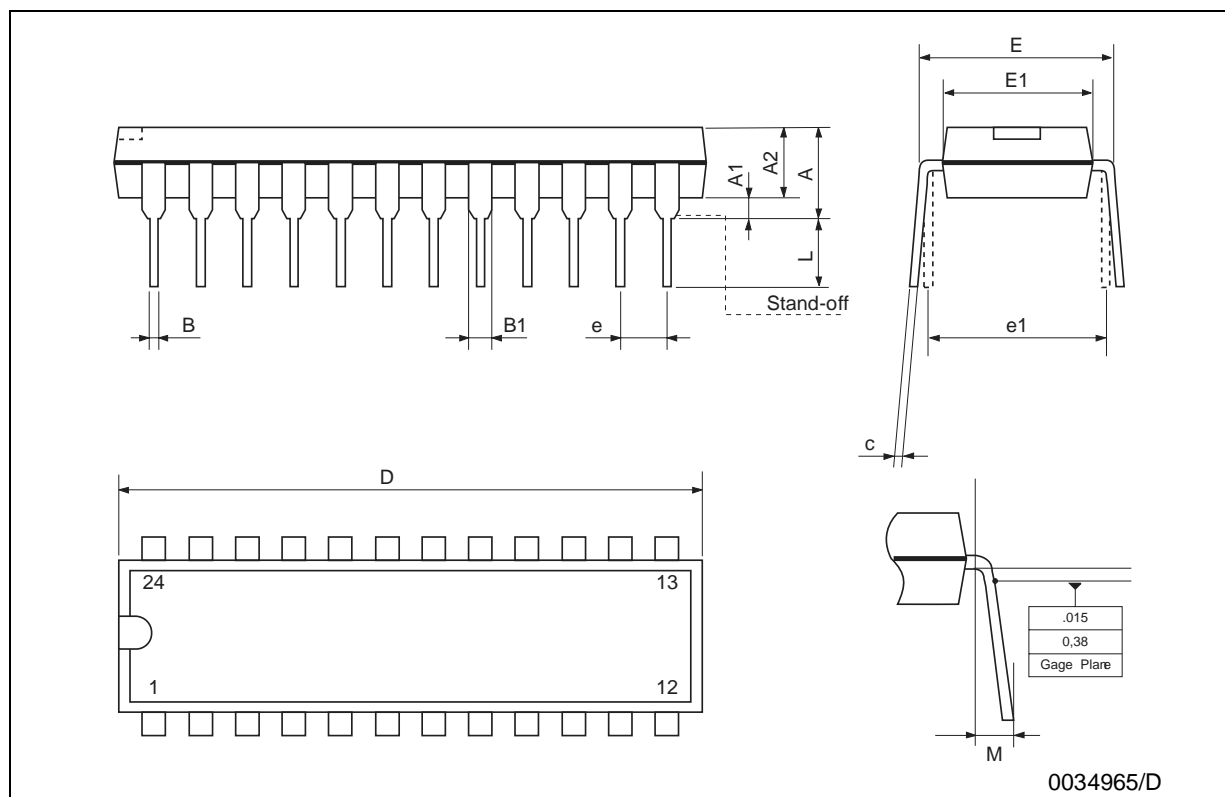


Figure 14: Power Dissipation vs Temperature Package



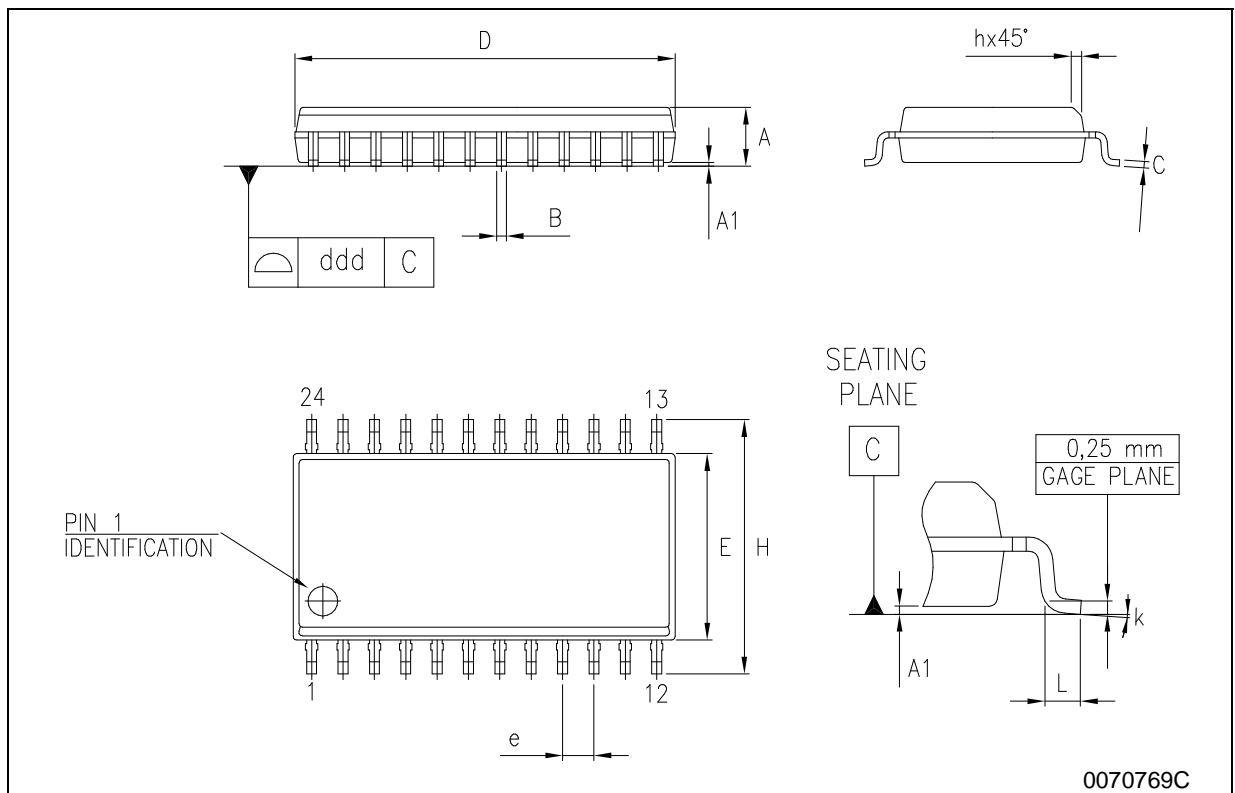
Plastic DIP-24 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.32			0.170
A1	0.38			0.015		
A2		3.3			0.130	
B	0.41	0.46	0.51	0.016	0.018	0.020
B1	1.40	1.52	1.65	0.055	0.060	0.065
c	0.20	0.25	0.30	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.62		8.26	0.300		0.325
E1	6.35	6.60	6.86	0.250	0.260	0.270
e		2.54			0.100	
E1		7.62			0.300	
L	3.18		3.43	0.125		0.135
M	0°		15°	0°		15°



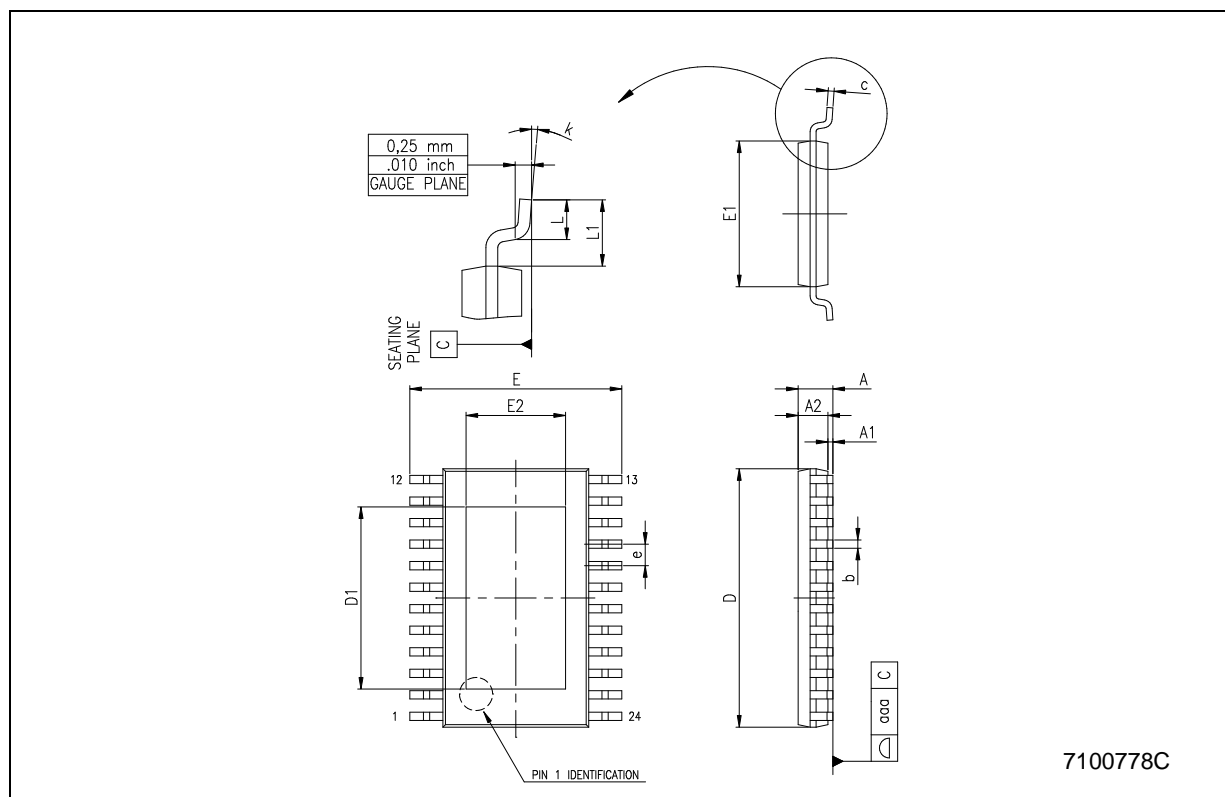
SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



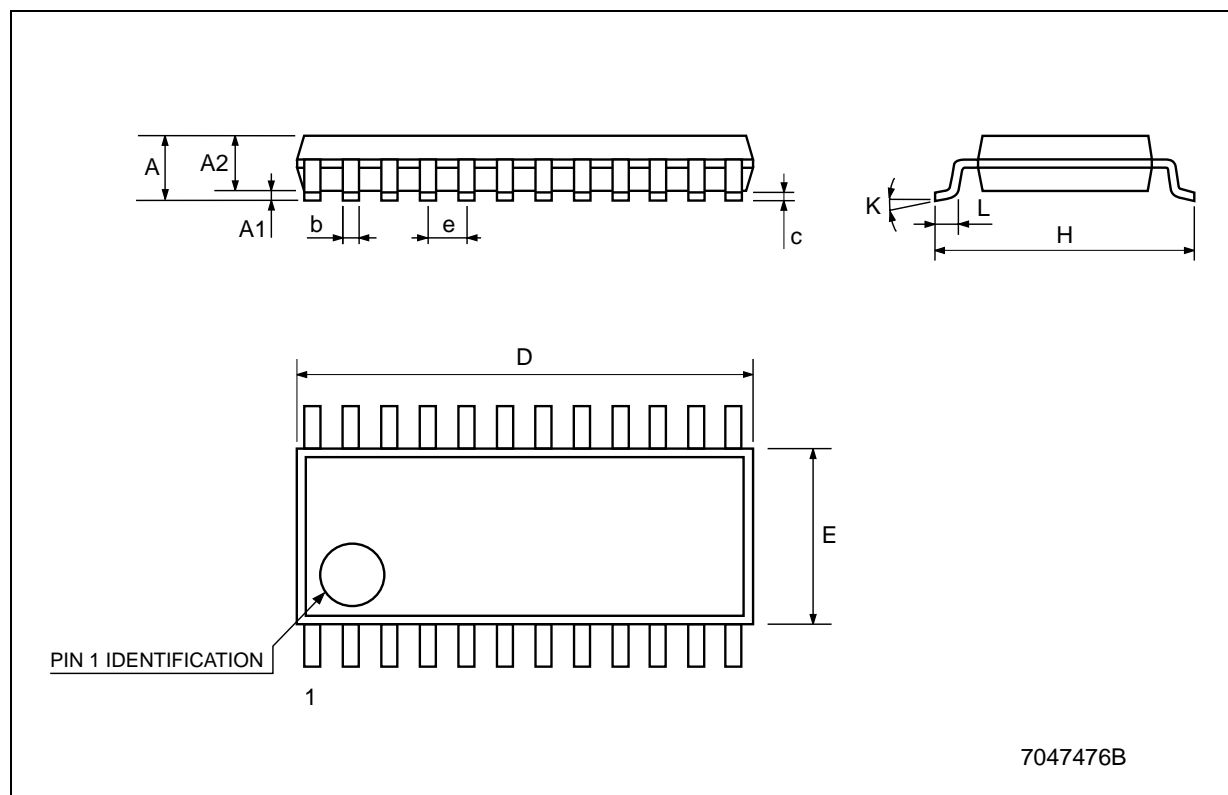
TSSOP24 EXPOSED PAD MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	2.7			0.106		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



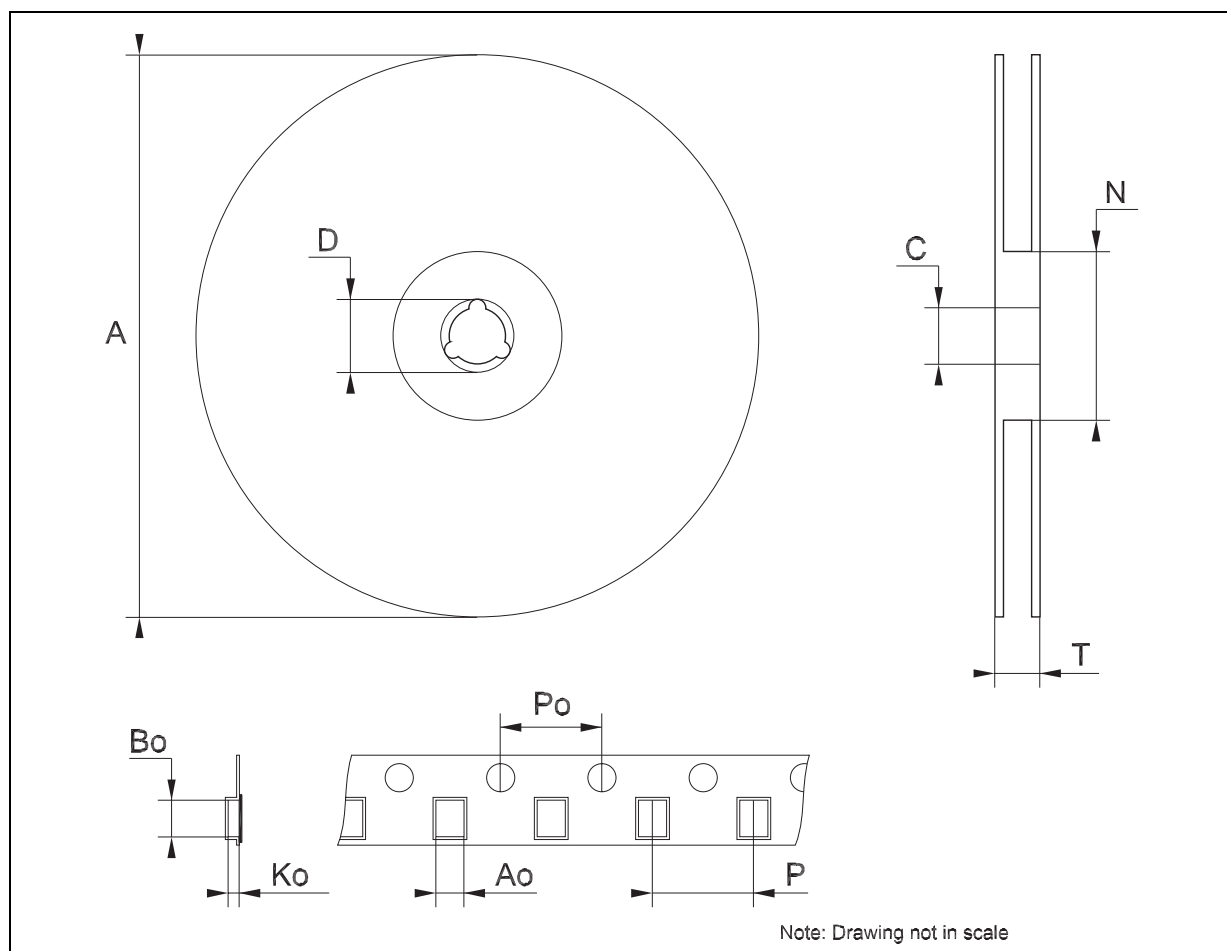
TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



Tape & Reel SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Tape & Reel TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

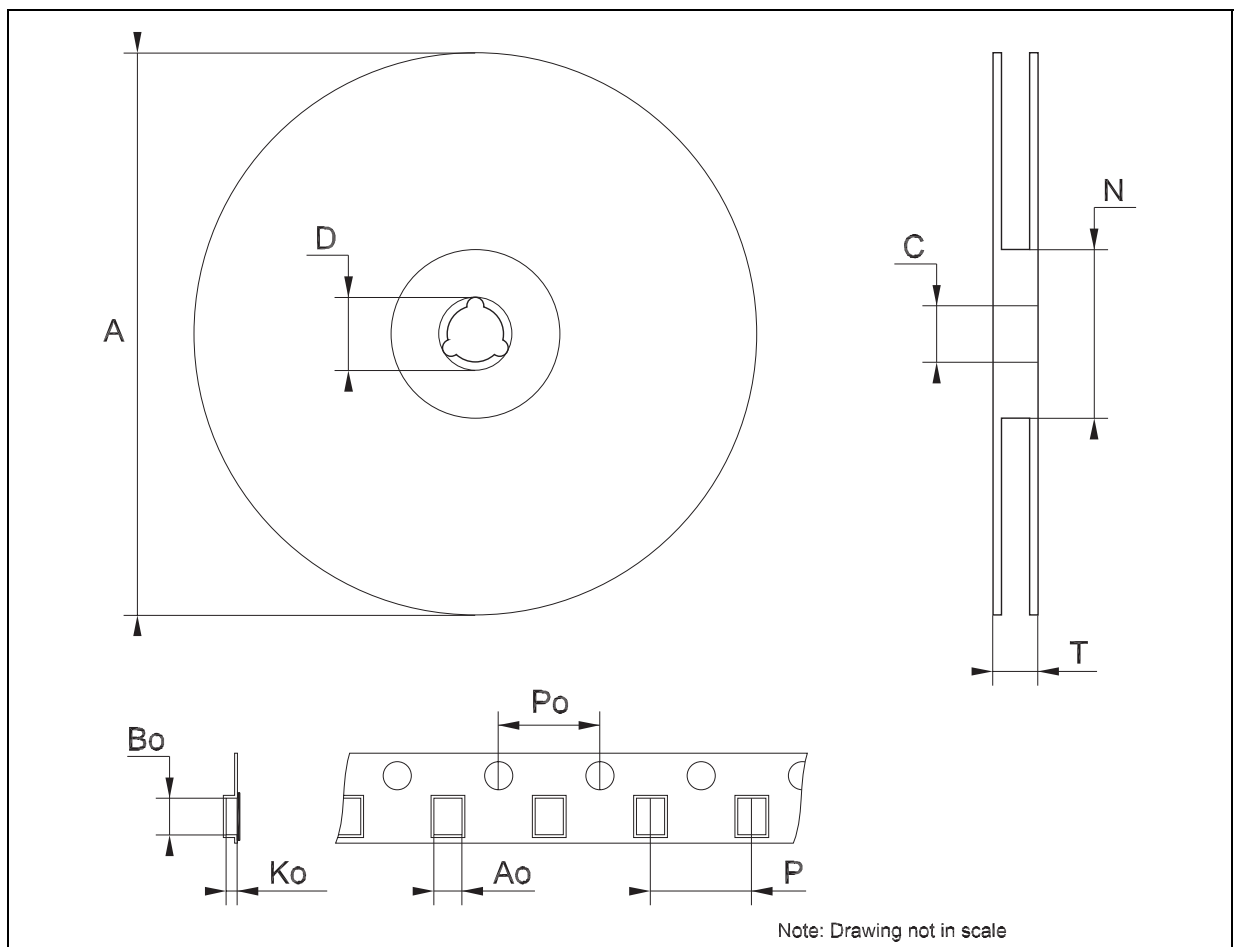


Table 10: Revision History

Date	Revision	Description of Changes
06-May-2004	4	Table 6 and Table 7 parameters changed
03-Aug-2004	5	Figure 14 - pag. 10 is changed.
31-Mar-2005	6	Mistake on Fig. 7.
02-May-2005	7	Typing Error on the description features.
22-Jul-2005	8	Add note on Fig. 1 and Table 5.

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