IRF640S

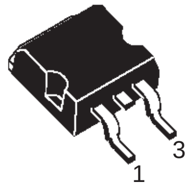
N - CHANNEL 200V - 0.150Ω - 18A TO-263
MESH OVERLAY™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF640S	200 V	< 0.18 Ω	18 A

- TYPICAL $R_{DS(on)}$ = 0.150 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

This power MOSFET is designed using he company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

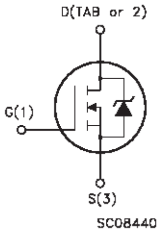


D^2PAK
TO-263
(suffix "T4")

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC COVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	18	A
I_D	Drain Current (continuous) at T_c = 100 °C	11	A
I_{DM}(•)	Drain Current (pulsed)	72	A
P_{tot}	Total Dissipation at T_c = 25 °C	125	W
	Derating Factor	1.0	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 18A$, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

THERMAL DATA

			3.12	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1.0		^{o}C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	62.5		oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink Typ	0.5		^{o}C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		^{o}C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	18	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 ^{o}C, $I_D = I_{AR}$, V_{DD} = 50 V)	280	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^{o}C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	μA
		V_{DS} = Max Rating T_c = 125 ^{o}C			10	μA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (∗)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 μA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 9 A		0.15	0.18	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	18			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (∗)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 9 A	3	4		S
C_{iss}	Input Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1200	1560	pF
C_{oss}	Output Capacitance			200	260	pF
C_{rss}	Reverse Transfer Capacitance			60	80	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	V_{DD} = 100 V I_D = 9 A		13	17	ns
t_r	Rise Time	R_G = 4.7 Ω V_{GS} = 10 V		27	35	ns
		(see test circuit, figure 3)				
Q_g	Total Gate Charge	V_{DD} = 160 V I_D = 18 A V_{GS} = 10V		55	72	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			21		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160 V I_D = 18 A		21	27	ns
t_f	Fall Time	R_G = 4.7 Ω V_{GS} = 10 V		25	32	ns
t_c	Cross-over Time	(see test circuit, figure 5)		50	65	ns

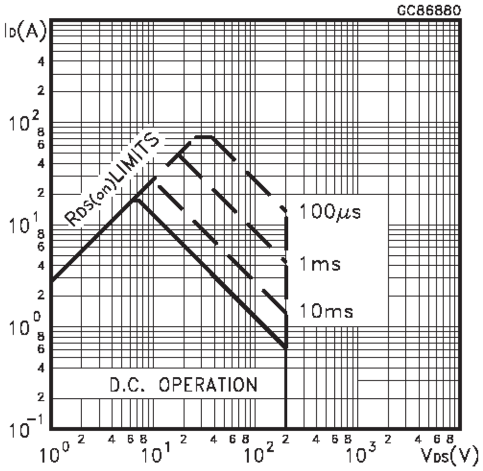
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				18	A
I_{SDM} (•)	Source-drain Current (pulsed)				72	A
V_{SD} (∗)	Forward On Voltage	I_{SD} = 18 A V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 18 A di/dt = 100 A/µs V_{DD} = 50 V T_j = 150 °C		240		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, figure 5)		1.8		µC
I_{RRM}	Reverse Recovery Current			15		A

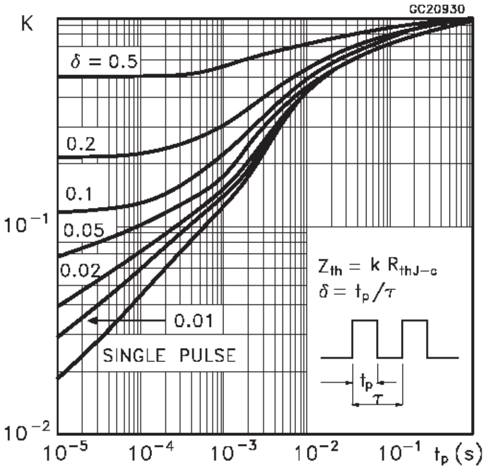
(∗) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

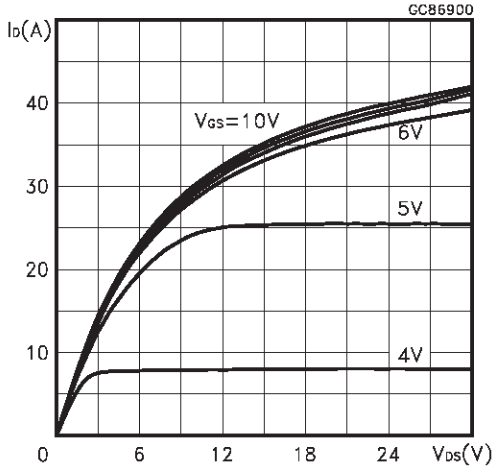
Safe Operating Area



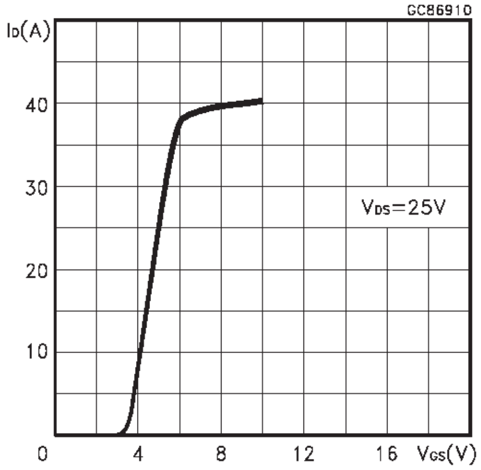
Thermal Impedance



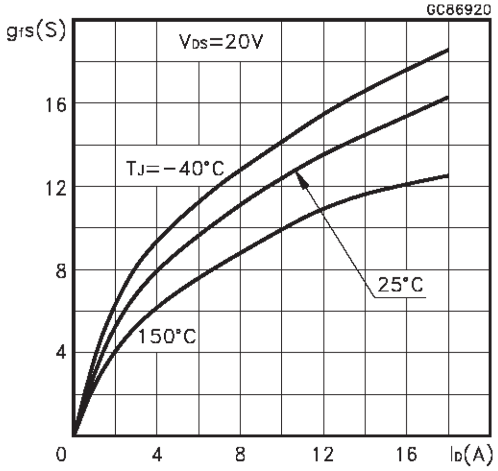
Output Characteristics



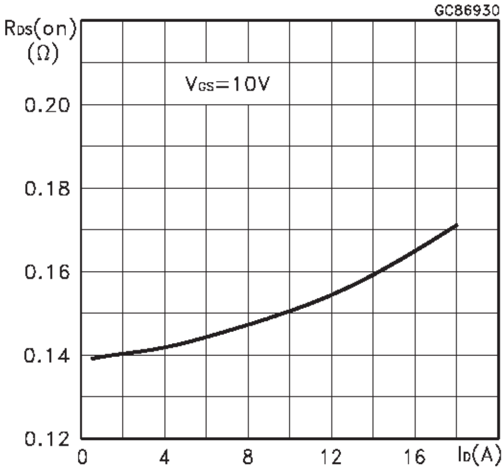
Transfer Characteristics



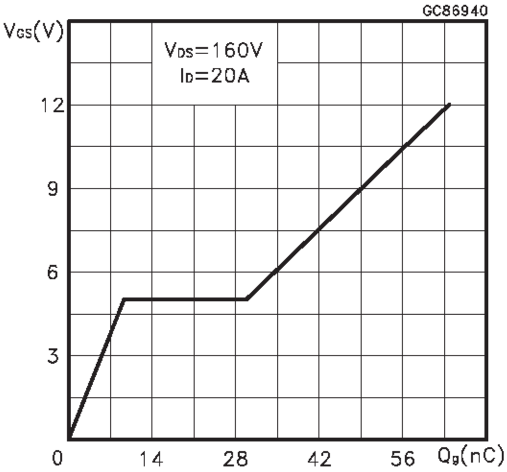
Transconductance



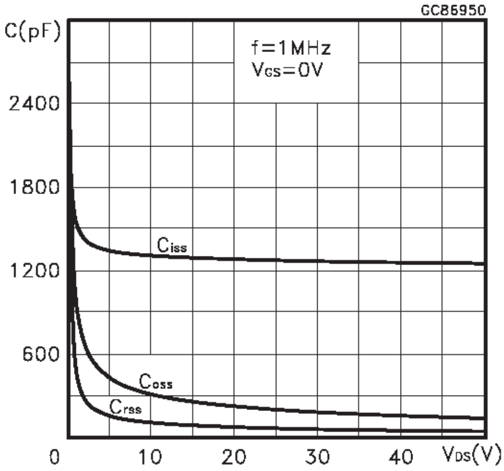
Static Drain-source On Resistance



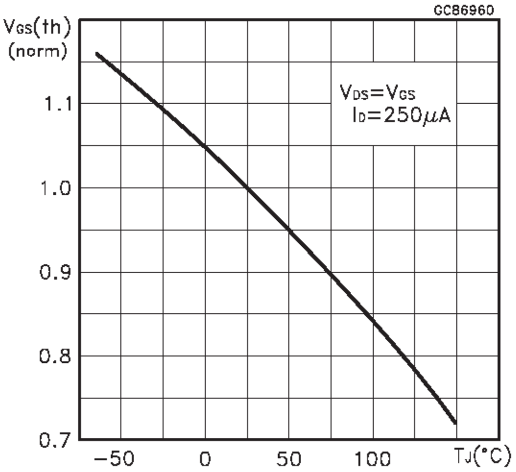
Gate Charge vs Gate-source Voltage



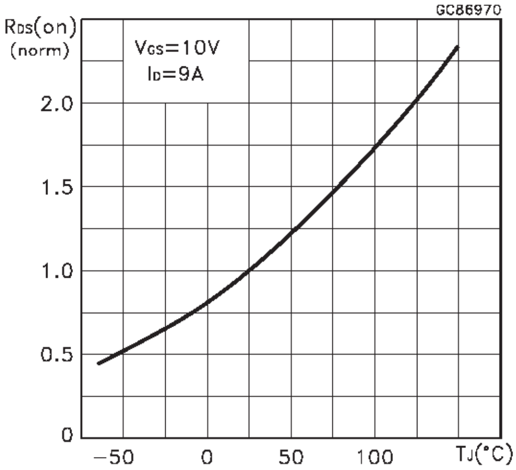
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

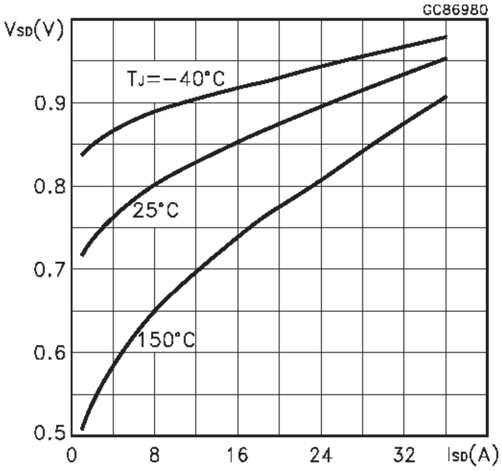


Fig. 1: Unclamped Inductive Load Test Circuit

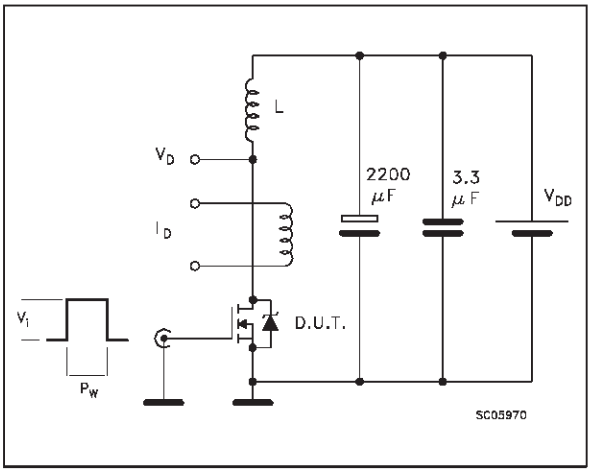


Fig. 1: Unclamped Inductive Waveform

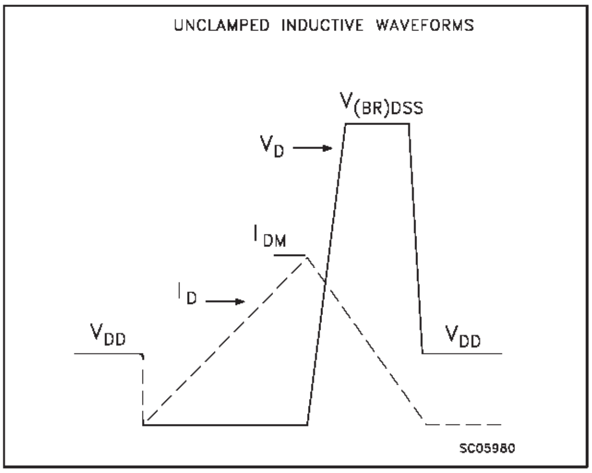


Fig. 3: Switching Times Test Circuits For Resistive Load

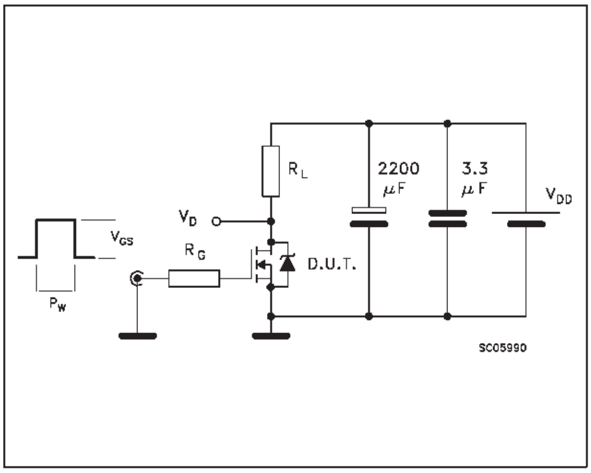


Fig. 4: Gate Charge test Circuit

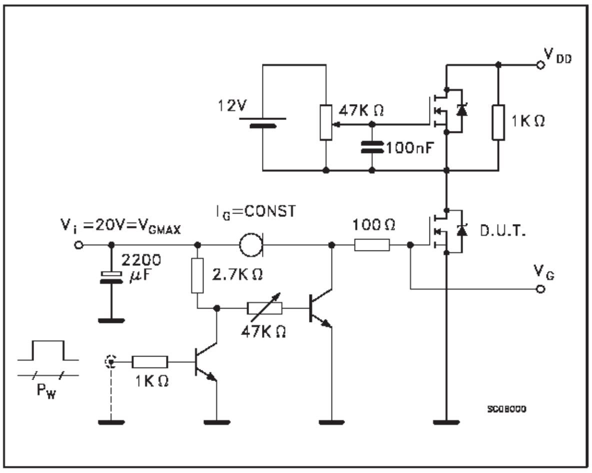
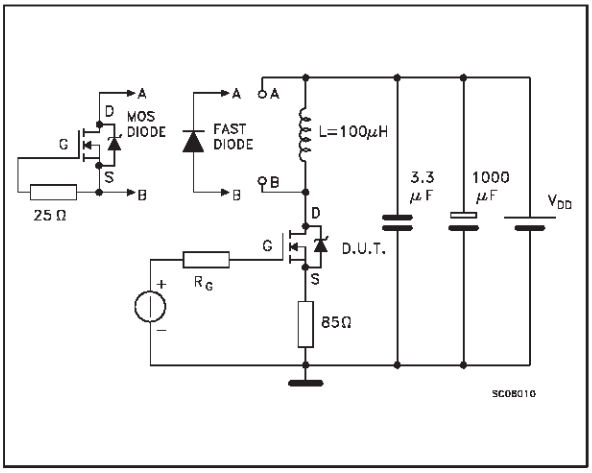
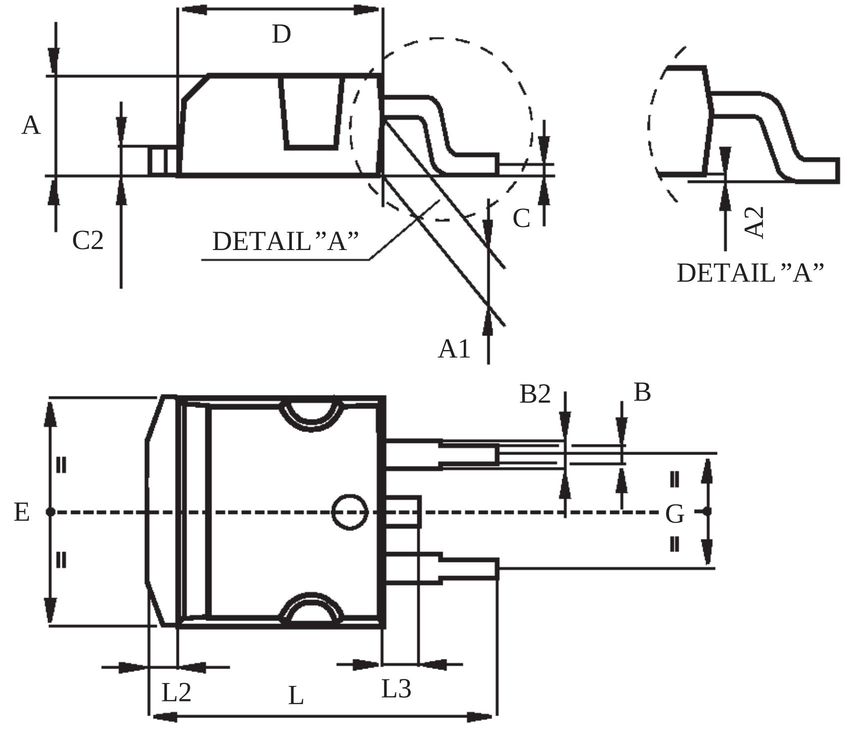


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D^2PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



P011P6/E

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com