DVIULC6-4SC6

Ultra low capacitance ESD protection

Main applications

- DVI ports up to 1.65 Gb/s
- HDMI ports up to 1.65 Gb/s
- IEEE 1394a and IEEE 1394b ports up to 1.6 Gb/s
- USB2.0 ports up to 480 Mb/s (high speed), backwards compatible with USB1.1 low and full speed
- Ethernet port: 10/100/1000 Mb/s
- SIM card protection
- Video line protection

Description

The **DVIULC6-4SC6** is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces, such as DVI, HDMI, IEEE 1394a and IEEE 1394b, USB2.0, Ethernet links and video lines.

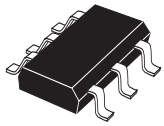
Its ultra low line capacitance secures a high level of signal integrity without compromising in protecting sensitive chips against the most stringent characterized ESD strikes.

Features

- 4 line ESD protection
- Protects V_{BUS} when applicable
- Ultra low capacitance: 0.6 pF at F = 825 MHz
- Fast response time
- SOT23-6L package
- RoHS compliant

Order code

Part Number	Marking
DVIULC6-4SC6	DL46



SOT23-6L
(JEDEC MO178AB)

Complies with these standards:

- IEC61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Benefits

- ESD standards compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of V_{BUS} when applicable. Allows ESD current flowing to Ground when ESD event occurs on data line
- Optimized rise and fall times for maximum data integrity
- Consistent D+ / D- signal balance:
  - Best capacitance matching tolerance I/O to GND = 0.015 pF for ultra low inter pair skew
  - Best capacitance matching tolerance I/O to I/O = 0.007 pF for ultra low intra pair skew
  - Matching high bit rate DVI, HDMI, and IEEE 1394 requirements
- Low PCB space consuming, 9mm² maximum foot print
- Low leakage current for longer operation of battery powered devices
- Higher reliability offered by monolithic integration

Figure 1. Functional Diagram

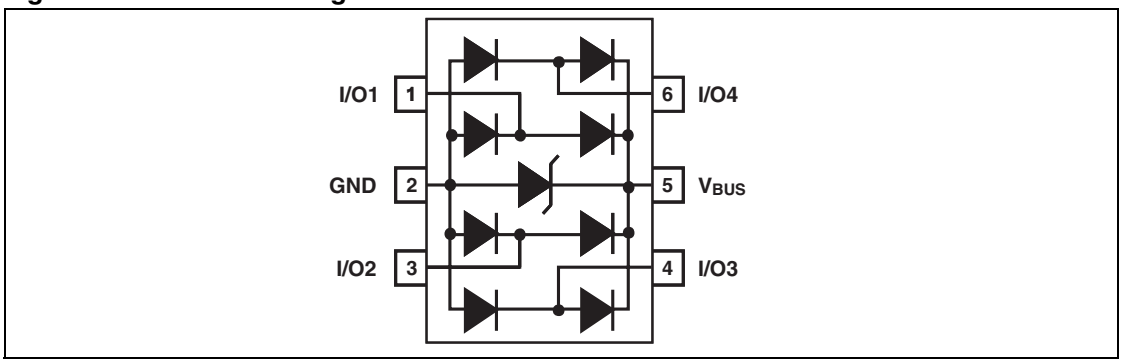


Table 1. Absolute Ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	At device level: IEC61000-4-2 air discharge IEC61000-4-2 contact discharge MIL STD883C-Method 3015-6	 ±15 ±15 ±25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max	
I_{RM}	Leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_{CL}	Clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 0 V, F= 1 MHz		0.85	1	pF
		V_R = 0 V, F= 825 MHz		0.6		
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND			0.015		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 0 V, F= 1 MHz		0.42	0.5	pF
		V_R = 0 V, F= 825 MHz		0.3		
$\Delta C_{i/o-i/o}$	Capacitance variation between I/O			0.007		

Figure 2. Line Capacitance versus line voltage (typical values)

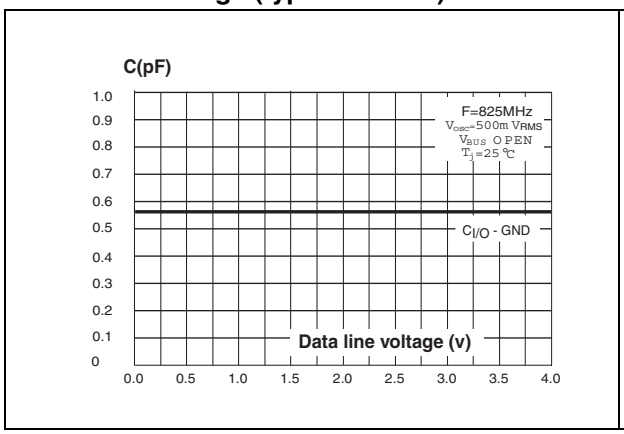


Figure 3. Line capacitance versus frequency (typical values)

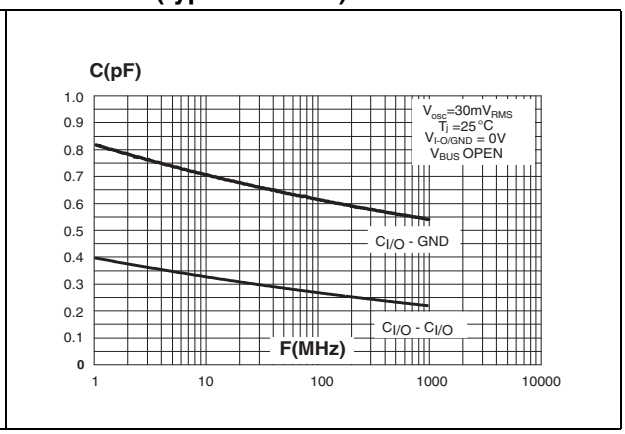


Figure 4. Relative variation of leakage current versus junction temperature (typical values)

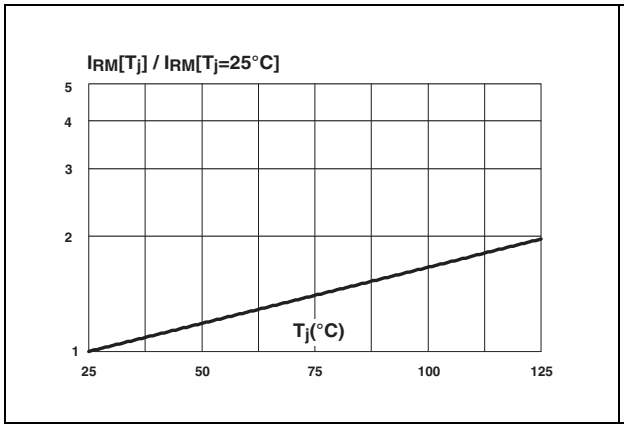
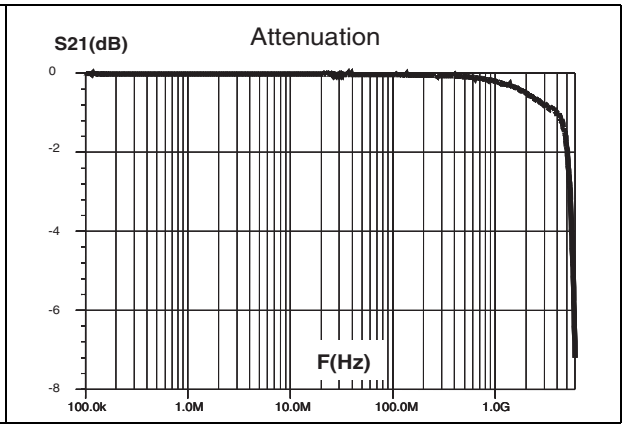


Figure 5. Frequency response



Technical information

1 Surge protection

The DVIULC6-4SC6 is particularly optimized to perform ESD surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follow:

$V_{CL}+ = V_{BUS} + V_F$ for positive surges

$V_{CL}- = - V_F$ for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F forward drop voltage) / (V_T forward drop threshold voltage)

We assume that the value of the dynamic resistance of the clamping diode is typically: R_d = 1.4 Ω and V_T = 1.2 V.

For an IEC61000-4-2 surge Level 4 (Contact Discharge: V_g=8 kV, R_g=330 Ω), V_{BUS} = +5 V, and if in first approximation, we assume that: $I_p = V_g / R_g$ = 24 A.

So, we find:

$V_{CL}+ = +39$ V

$V_{CL}- = -34$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC} and from GND to PCB GND are done by two tracks of 10mm long and 0.5 mm large; we assume that the parasitic inductances L_w of these tracks are about 6nH. So when an IEC61000-4-2 surge occurs, due to the rise time of this spike (tr=1 ns), the voltage V_{CL} has an extra value equal to Lw.dI/dt.

The dI/dt is calculated as: dI/dt = Ip/tr = 24 A/ns

The over voltage due to the parasitic inductances is: Lw.dI/dt = 6 x 24 = 144 V

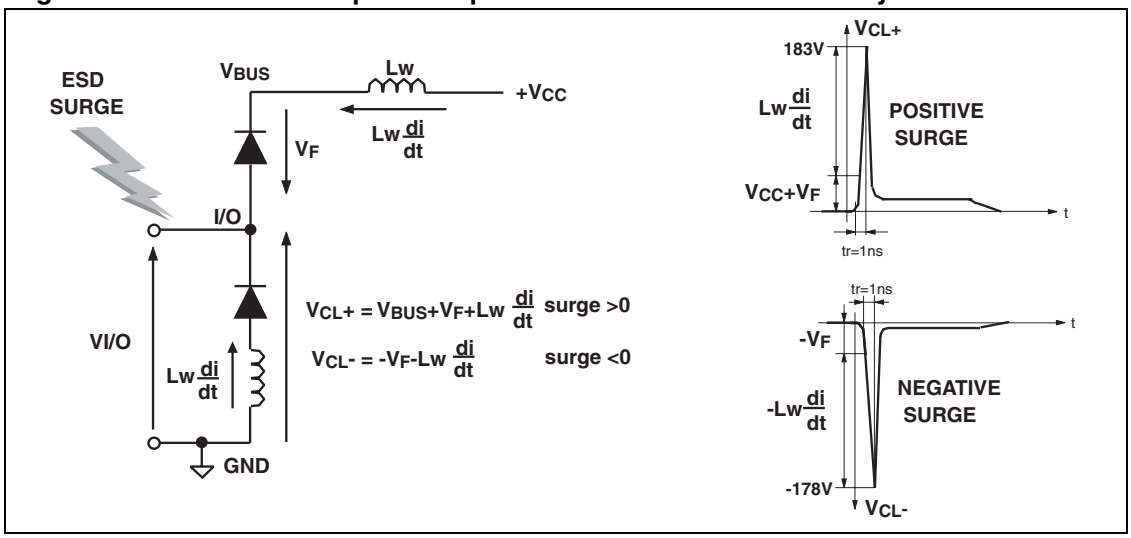
By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

$$V_{CL}+ = +39 + 144 = 183\ V$$
$$V_{CL}- = -34 - 144 = -178\ V$$

We can reduce as much as possible these phenomena with simple layout optimization.

It's the reason why some recommendations have to be followed (see *Section 3: How to ensure a good ESD protection*).

Figure 6. ESD behavior: parasitic phenomena due to unsuitable layout



3 How to ensure a good ESD protection

While the DVIULC6-4SC6 provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from the V_{BUS} pin to the power supply $+V_{CC}$ and from the V_{BUS} pin to GND must be as short as possible to avoid over voltages due to parasitic phenomena (see *Figure 6*).

It's often harder to connect the power supply near to the DVIULC6-4SC6 unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the DVIULC6-4SC6, between V_{BUS} and ground, a capacitance of 100nF to prevent from these kinds of overfatigue disturbances (see *Figure 7*).

The add of this capacitance will allow a better protection by providing during surge a constant voltage.

The *Figure 8*, *Figure 9*, and *Figure 10* show the improvement of the ESD protection according to the recommendations described above.

Figure 7. ESD behavior: optimized layout and add of a capacitance of 100nF

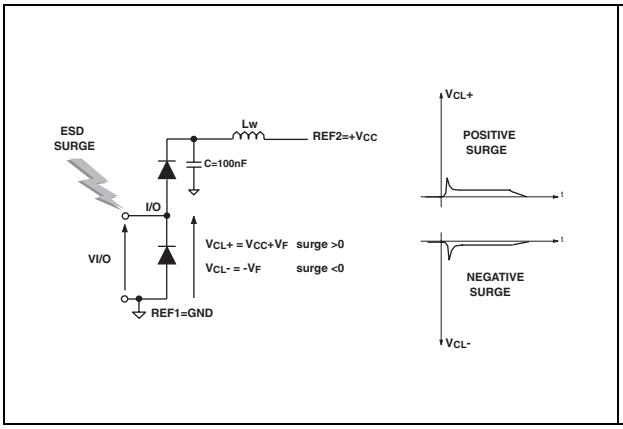


Figure 8. ESD behavior: measurements conditions (with coupling capacitance)

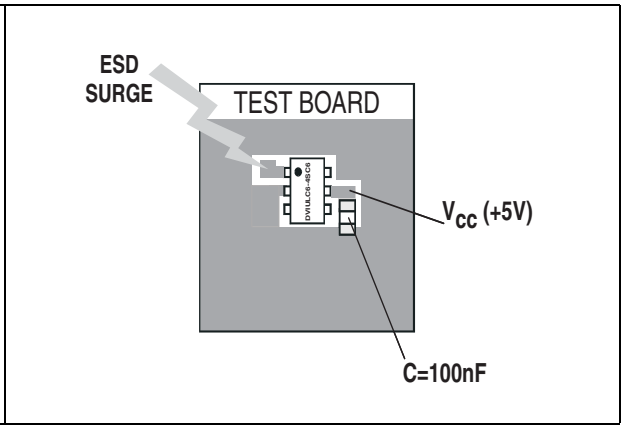


Figure 9. Remaining voltage after the DVIULC6-4SC6 during positive ESD surge

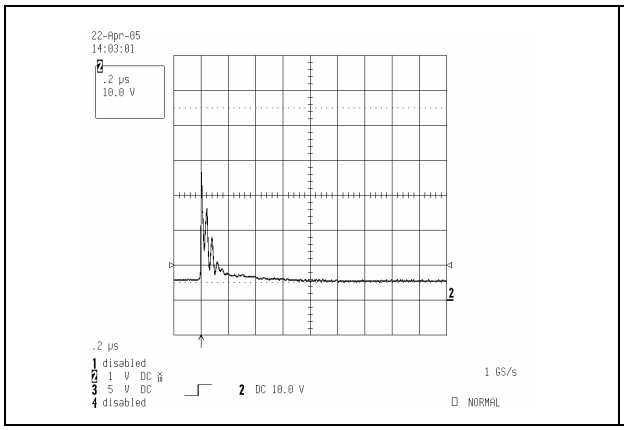
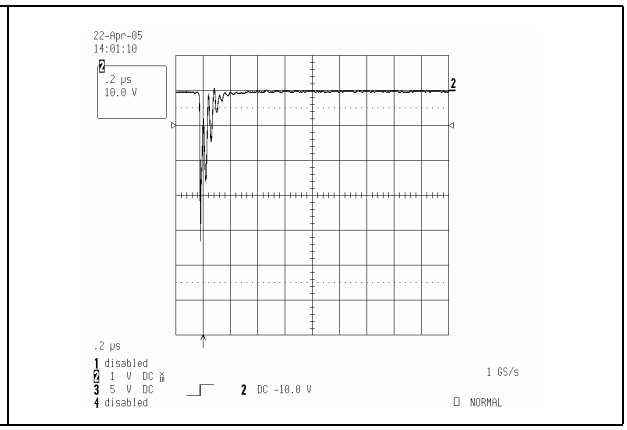


Figure 10. Remaining voltage after the DVIULC6-4SC6 during negative ESD surge



IMPORTANT:

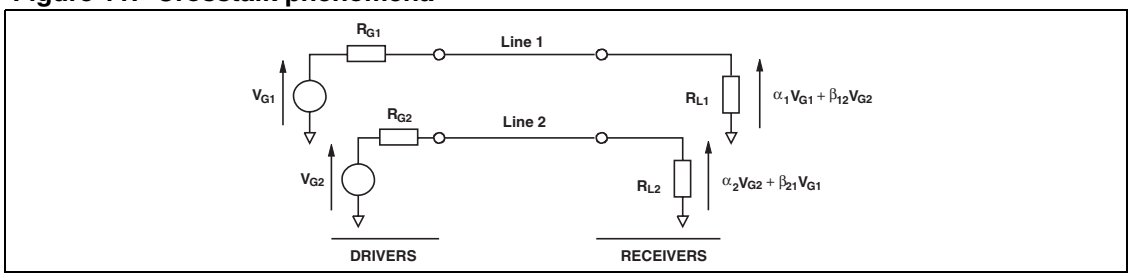
A main precaution to take is to put the protection device closer to the disturbance source (generally the connector).

Note: The measurements have been done with the DVIULC6-4SC6 in open circuit.

4 Crosstalk behavior

4.1 Crosstalk phenomena

Figure 11. Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when

the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 12. Analog crosstalk measurements

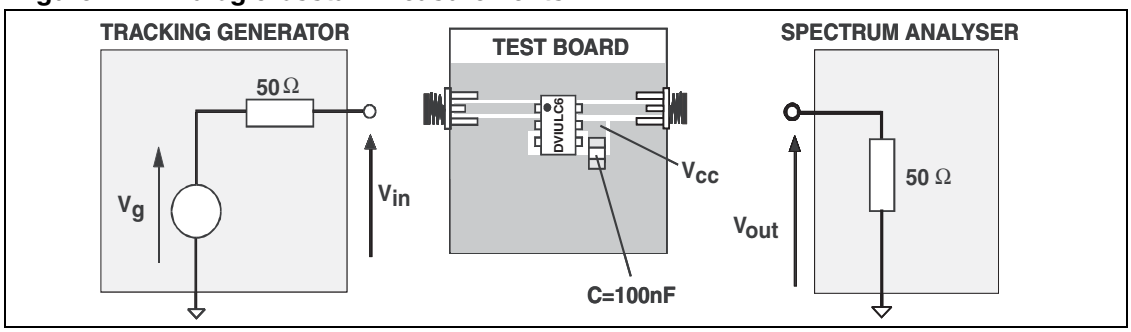
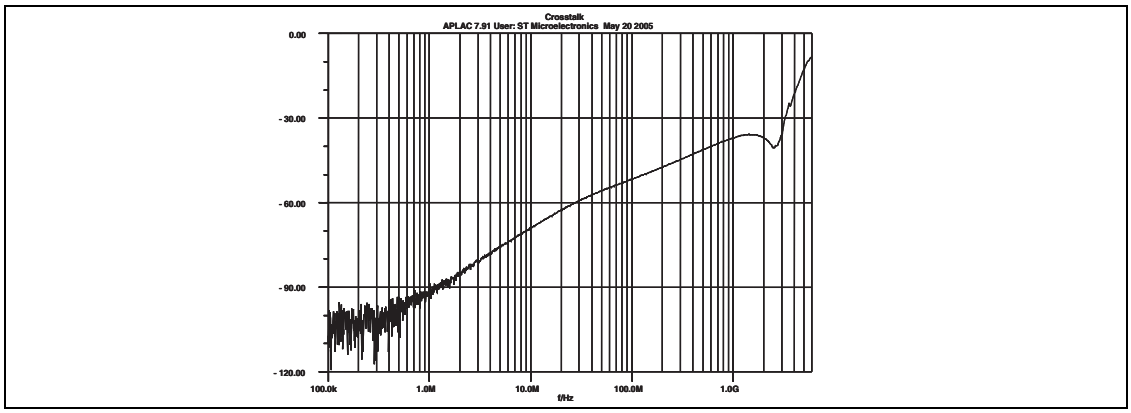


Figure 12 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -45 dB (see *Figure 13*).

Figure 13. Analog crosstalk results



As the DVIULC6-4SC6 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (figure 5) gives attenuation information and shows that the DVIULC6-4SC6 is well suitable for data line transmission up to 1.65 Gb/s.

5 Application examples

Figure 14. DVI/HDMI Digital single link application using DVIULC6-4SC6

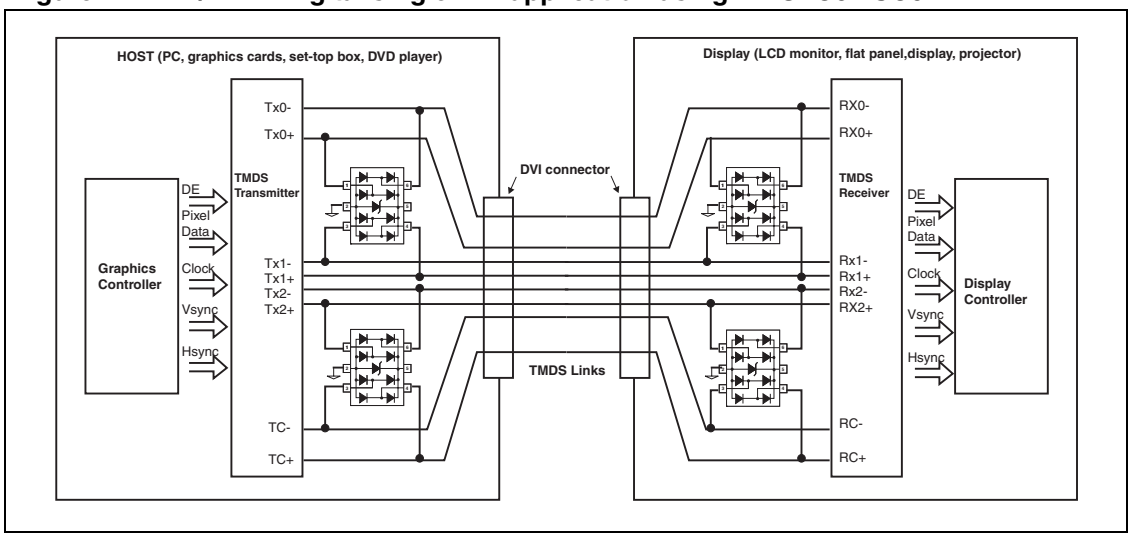
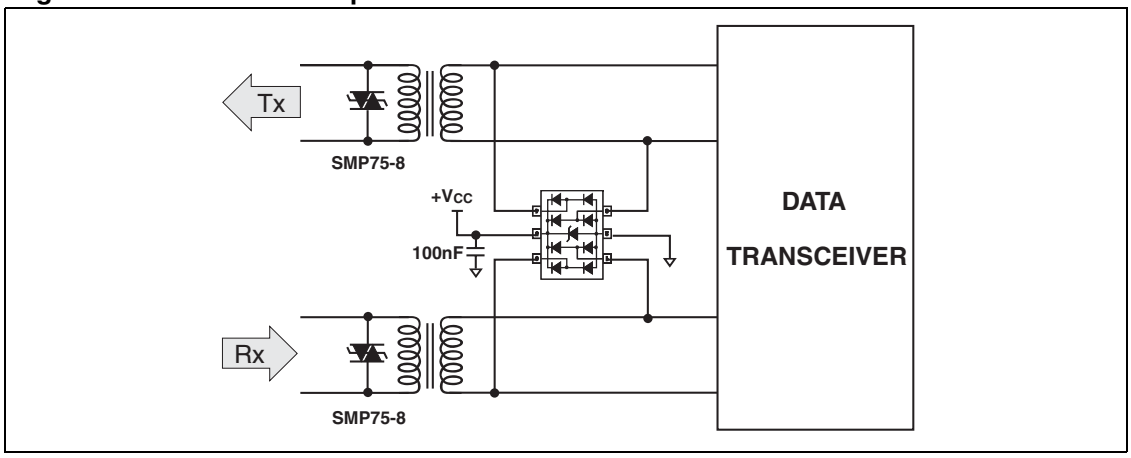


Figure 15. T1/E1/Ethernet protection



6 PCB layout considerations

Figure 16. DVIULC6-4SC6 PCB layout considerations (V_{CC} connection is application dependent)

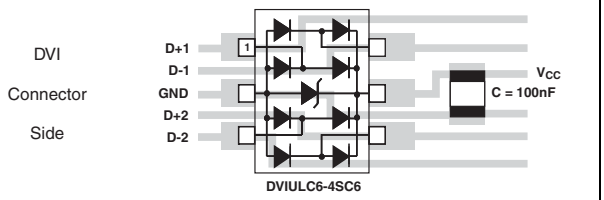


Figure 17. Foot Print Dimensions (in millimeters)

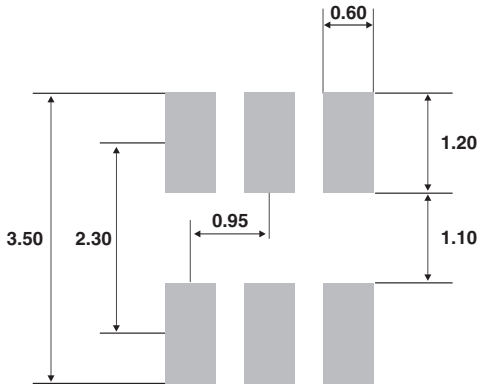
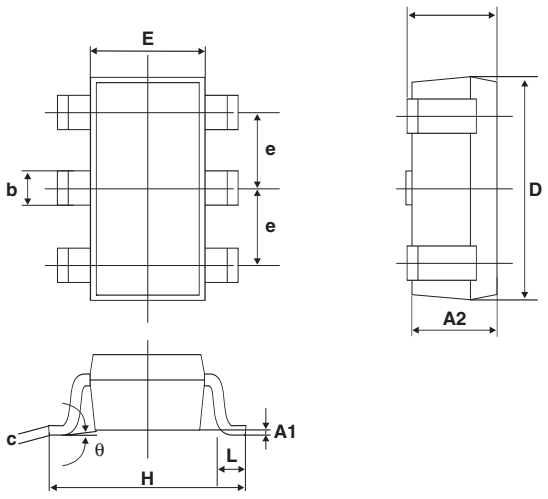


Figure 18. SOT23-6L Package Mechanical Data



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

7 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
DVIULC6-4SC6	DL46	SOT23-6L	16.7 mg	3000	Tape & reel

8 Revision history

Date	Revision	Description of Changes
24-Aug-2005	1	First Issue