AIC-43C97

Automated, High-performance, Integrated, SCSI Protocol Controller designed for SCSI-2/SCSI-3 embedded peripheral applications

DATA BRIEF

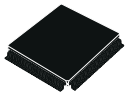
1 SCSI Host Interface Block

- Dual Mode Ultra-2 I/O supporting Low
- Voltage Differential (LVD) and Single
- Ended SCSI Interfaces
  - Ultra-2 (80 MB/s wide, 40 MB/s narrow) and slower with LVD
  - Ultra (40 MB/s wide, 20 MB/s narrow) and slower with Single Ended
- Supports Target and Initiator Modes
- Programmable SCSI Sequencer for Target Mode
  - Automatic Command receipt with messages
  - Automatic Disconnect and Reconnect
  - Automatic Message
  - Automatic Status
  - Automatic parsing of frequently used SCSI commands
  - Reduced Microprocessor Overhead
  - Auto Write & Auto Match operations
  - Two active contexts to support command execution pipelining or overlapping
- Two 16-byte SCSI Control FIFO's
- 128-byte SCSI Data FIFO
- Block or byte-based transfer counter
- Odd-byte transfer support in byte mode
- Stores configuration information for up to three SCSI devices
- Supports automatic SCAM selection and SCAM transfer cycles
- Selectable REQ/ACK noise Filtering

2 DMA Interface Block

- "ATA DMA Master/Slave" mode:
  - Supports 8/16-bit transfers with programmable speeds up to 40 MB/s in 16-bit mode
- "SCSI DMA" mode:
  - Supports 8/16-bit transfers with programmable speeds up to 100 MB/s in 16-bit asynchronous/synchronous mode
- "Generic" mode:
  - Supports 8/16-bit transfers with programmable speeds up to 40 MB/s in 16-bit mode

Figure 1. Package



TQFP144

Table 1. Order Codes

Part Number	Package
AIC-43C97M/C	TQFP144

3 Microcontroller Interface Block

- Selectable µP Style and Bus Mode
  - Multiplexed or non-multiplexed
  - Selectable strobing style (*RD & *WR, or E/*DS & R/*W)
  - 16-bit or 8-bit data (8-bit data only in non-multiplexed mode)
  - Programmable CS and INT polarities
- Supports wide variety of MPUs
  - Intel 80C196xx
  - Motorola 68HC11 & 68HC16
  - NEC V852
  - Hitachi SH-1 7034 & H8 3002
  - Intel 80C186

4 Buffer Manager and Buffer RAM

- 8KB RAM for buffering data and speed matching between and Host DMA ports
- Concurrent Buffer RAM access by Host and DMA ports
- MPU access of Buffer RAM when DMA port is disabled
- Parity protection on buffer data
- Block or Byte based data flow control between Host and DMA ports

5 Frequency Synthesizer

- 960 MHz PLL for high resolution on selections of HIFCLK and DIFCLK

This is preliminary information on a new product now in development. Details are subject to change without notice.

6 Other Features

- 144-pin TQFP package
- End-to-end parity protection on data path
- 5V Single-ended SCSI I/O support with dedicated 5V supply
- 5V tolerant 3.3V I/O on non-SCSI pins
- 0.35µ 3.3V CMOS

7 Introduction

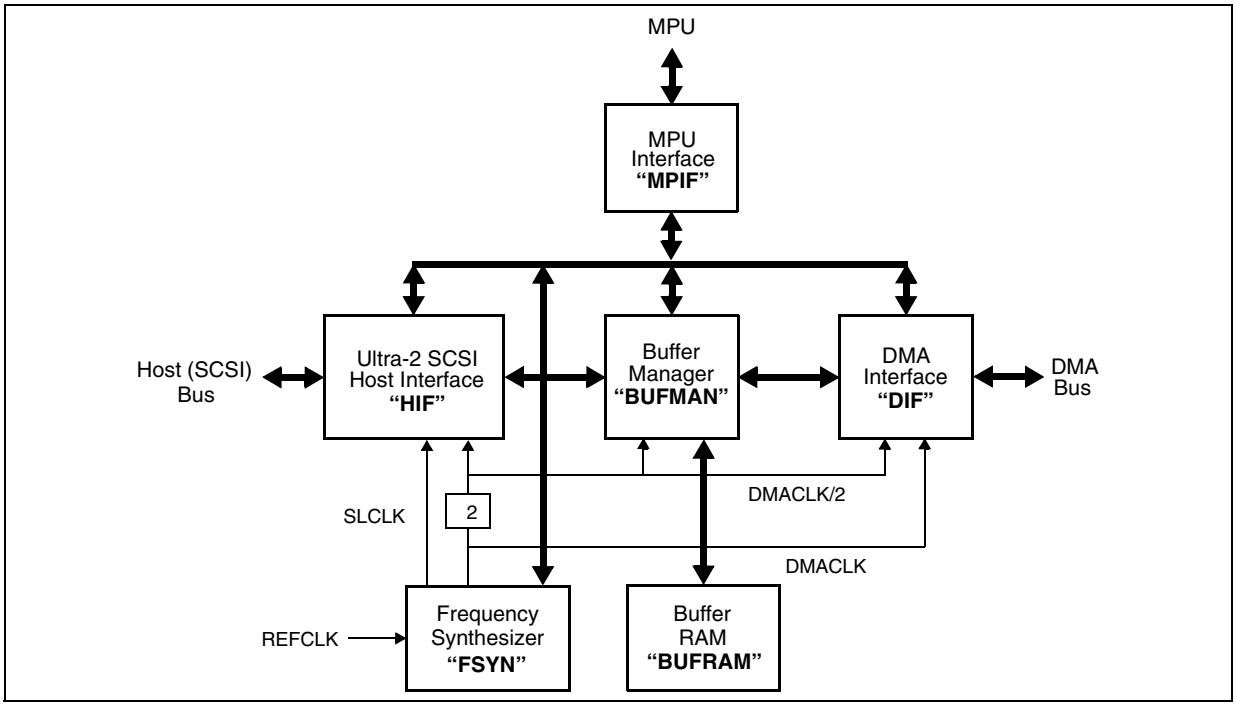
The AIC-43C97C is an automated, high-performance, integrated, SCSI protocol controller designed for SCSI-2/SCSI-3 embedded peripheral applications. The AIC-43C97C provides the necessary support for interfacing the SCSI bus to a peripheral using a DMA bus. It consists of three main blocks: SCSI Bus Interface, Buffer Controller and associated embedded 8 Kbyte FIFO RAM, and DMA Interface. Automation within this device enables a more efficient SCSI operation, thus minimizing microprocessor involvement.

The AIC-43C97C Ultra-2 SCSI Protocol chip supports the Low Voltage Differential (LVD) feature required to enable connectivity to the Ultra-2 80 MB/s bus. The AIC-43C97C also maintains backward compatibility to single-ended operation by detecting signal variance on the SCSI bus and automatically defaulting to the proper SCSI bus characteristic of single ended or Low Voltage Differential.
An embedded 960 MHz Phase Locked Loop Frequency Synthesizer provides high resolution on selection of SCLK and BCLK frequencies for the SCSI bus.

The AIC-43C97C supports both Initiator and Target modes. As a Target, the SCSI sequencer handles SCSI commands with as few as 0 interrupts to the microprocessor. In the case of Auto Matched Read or Write operation, 0 interrupts may be generated requiring no additional processing time. The sequencer can be custom programmed to handle most tasks to achieve maximum performance. The AIC-43C97C also has automated support for SCAM Level 1 and SCAM Level 2.

The AIC-43C97C has incorporated three DMA modes: an ATA mode which runs in Master and Slave Modes and sustains DMA transfers to 40 MB/s in 16-bit mode, a SCSI mode which runs in asynchronous and synchronous initiator modes up to 100 MB/s, and a Generic DMA mode that sustains DMA transfers up to 40 MB/s in 16-bit mode.

Figure 2. AIC-43C97C Block Diagram

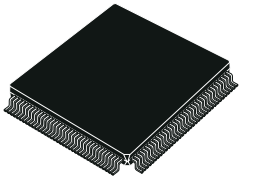


8 Package Information

Figure 3. TQFP144 Mechanical Data & Package Dimensions

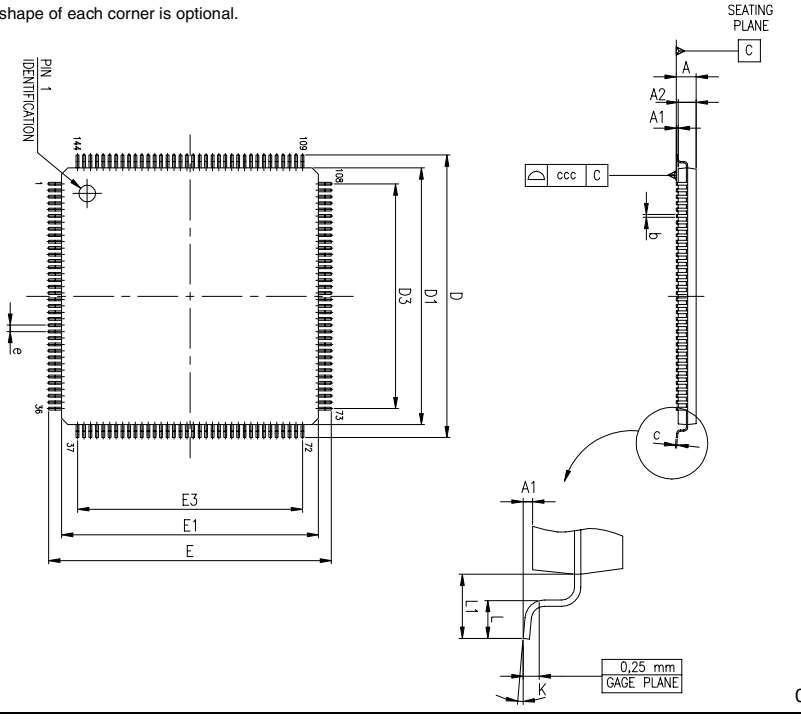
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		22.00			0.866	
D1		20.00			0.787	
D3		17.50			0.689	
e		0.50			0.020	
E		22.00			0.866	
E1		20.00			0.787	
E3		17.50			0.689	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5° (min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP144 (20x20x1.40mm)

Note 1: Exact shape of each corner is optional.



9 Revision History

Table 2. Revision History

Date	Revision	Description of Changes
December 2004	1	First Issue

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