SIEMENS

5-V Low-Drop Fixed Voltage Regulator   TLE 4270

Features

- Output voltage tolerance $\leq \pm 2\%$
- Low-drop voltage
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Adjustable reset time
- ESD protection > 4000 V

Type	Ordering Code	Package
TLE 4270	Q67000-A9209-A903	P-TO220-5-11
TLE 4270 S	Q67000-A9243-A904	P-TO220-5-12
TLE 4270 G	Q67006-A9201-A901	P-TO263-5-1
▼ TLE 4270	Q67000-A9209-A801	P-TO220-5-1
▼ TLE 4270 S	Q67000-A9243-A802	P-TO220-5-2
▼ TLE 4270 G	Q67006-A9201-A802	P-TO220-5-8
● TLE 4270 D	Q67006-A9360	P-TO252-5-1

▼ Not for new design   ● New type
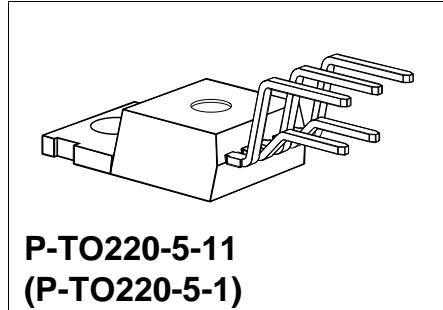
**P-TO220-5-11
(P-TO220-5-1)**
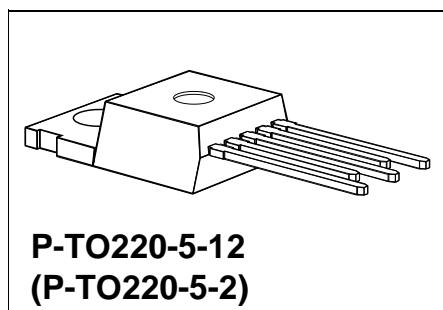
**P-TO220-5-12
(P-TO220-5-2)**
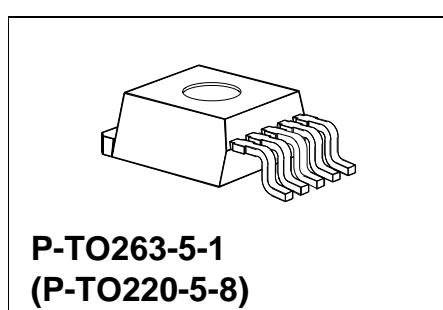
**P-TO263-5-1
(P-TO220-5-8)**

P-TO252-5-1 (D-PAK)

Functional Description

This device is a 5-V low-drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V, ≤ 400 ms). Up to an input voltage of 26 V and for an output current up to 550 mA it regulates the output voltage within a 2 % accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and temperature protection that disables the circuit at unpermissibly high temperatures.

Pin Configuration

(top view)
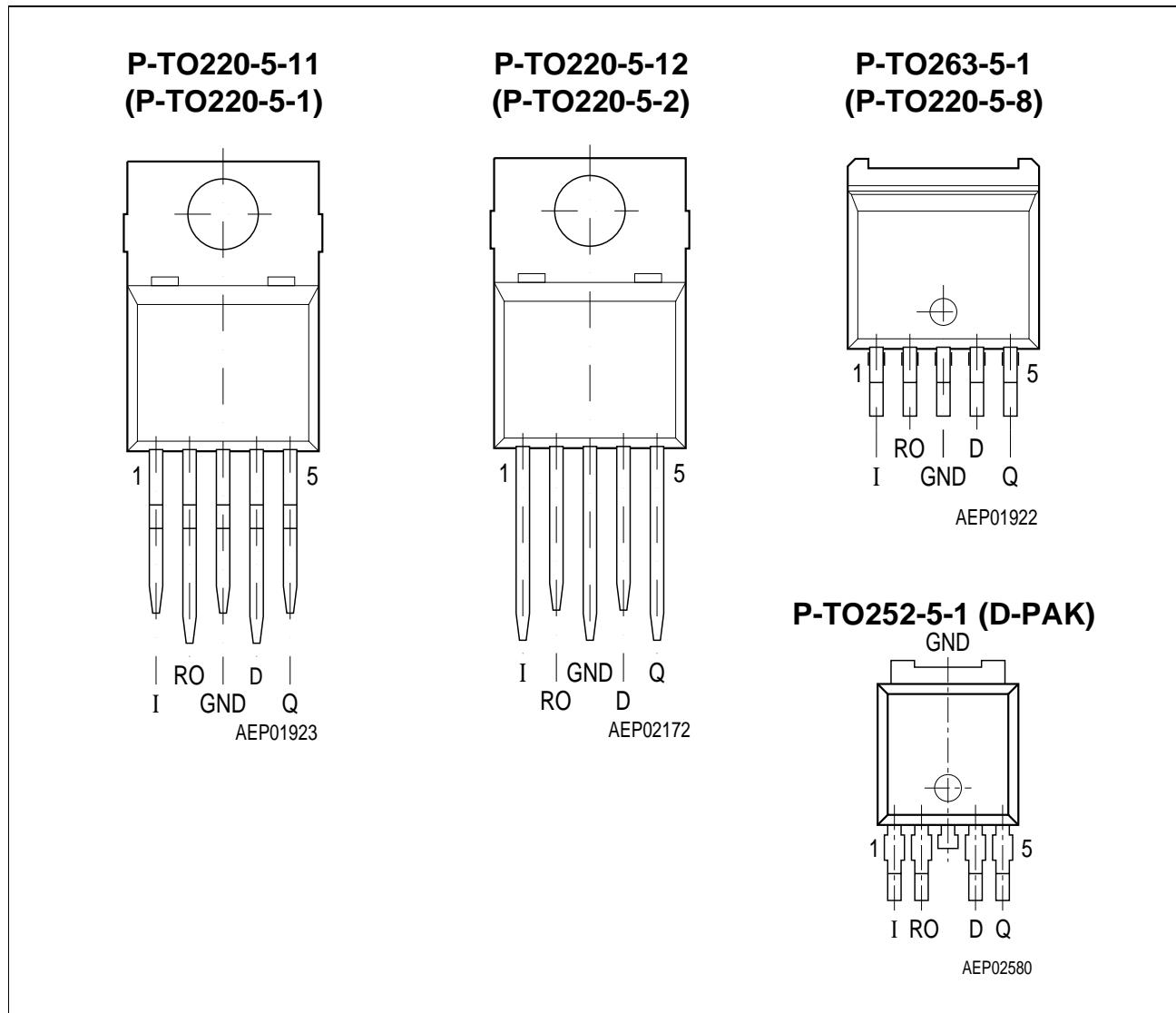
Figure 1

Pin Definitions and Functions

Pin	Symbol	Function
1	I	**Input**; block to ground directly on the IC with ceramic capacitor
2	RO	**Reset Output**; the open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.
3	GND	**Ground**; internally connected to heatsink.
4	D	**Reset Delay**; connect a capacitor to ground for delay time adjustment.
5	Q	**5-V Output**; block to ground with 22 μF capacitor, ESR $<$ 3 Ω.

Application Description

The IC regulates an input voltage in the range of 5.5 V $< V_I <$ 36 V to $V_{Qnom} =$ 5.0 V. Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. A reset signal is generated for an output voltage of $V_Q <$ 4.5 V. The delay for power-on reset can be set externally with a capacitor.

Design Notes for External Components

An input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. An output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of $C_Q \geq 22\ \mu F$ and an ESR of $< 3\ \Omega$.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

If the output voltage decreases below 4.5 V, an external capacitor C_D on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below V_{DRL}, a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above 4.5 V, C_D will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_D.

The IC also incorporates a number of internal circuits for protection against:

• Overload
• Overvoltage
• Overtemperature
• Reverse polarity

Temperature Sensor

Saturation Control and Protection Circuit

Input

1

5 Output

Control Amplifier

Adjustment

Bandgap Reference

+

−

Buffer

Reset Generator

2 Reset Output

4 Reset Delay

3
GND

AEB01924
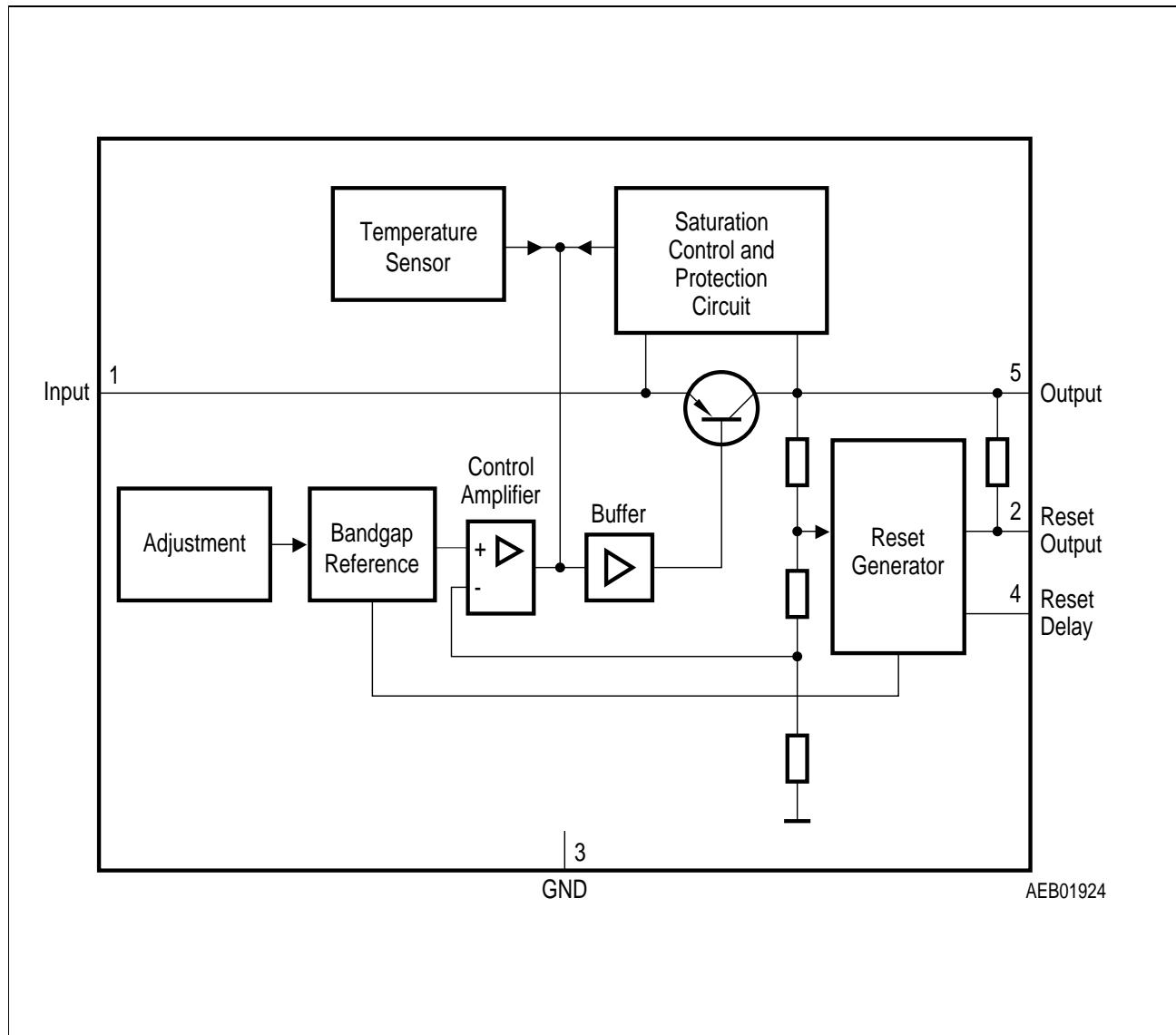
Figure 2
Block Diagram

Absolute Maximum Ratings

$T_j = -40$ to $150\ °C$

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		

Input

Voltage	V_I	-42	42	V	
Voltage	V_I		65	V	$t \leq 400$ ms
Current	I_I				internally limited

Reset Output

Voltage	V_R	-0.3	7	V	
Current	I_R				Internally limited

Reset Delay

Voltage	V_D	-0.3	7	V	
Current	I_D				Internally limited

Output

Voltage	V_Q	-1.0	16	V	
Current	I_Q				Internally limited

Ground

Current	I_{GND}	-0.5	–	A	–

Temperatures

Junction temperature	T_j		150	$°C$	–
Storage temperature	T_{stg}	-50	150	$°C$	

Optimum reliability and life time are guaranteed if the junction temperature does not exceed $125\ °C$ in operating mode. Operation at up to the maximum junction temperature of $150\ °C$ is possible in principle. Note, however, that operation at the maximum permitted ratings could affect the reliability of the device.

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage	V_I	6	42	V	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistance

Junction ambient	R_{thja}	–	65	K/W	
			70	K/W	TO263, TO252[1]
Junction case	R_{thjc}	–	3	K/W	$t < 1$ ms
	Z_{thjc}		2	K/W	(TO-220/263 Packages)

[1] Soldered in, min. footprint

Characteristics
V_I = 13.5 V; – 40 °C ≤ T_j = ≤ 125 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 550 mA; 6 V ≤ V_I ≤ 26 V
Output voltage	V_Q	4.90	5.00	5.10	V	26 V ≤ V_I ≤ 36 V; I_Q ≤ 300 mA
Output current limiting	I_{Qmax}	650	850	–	mA	$V_Q = 0$ V
Current consumption $I_q = I_I - I_Q$	I_q	–	1	1.5	mA	$I_Q = 5$ mA
Current consumption $I_q = I_I - I_Q$	I_q	–	55	75	mA	$I_Q = 550$ mA
Current consumption $I_q = I_I - I_Q$	I_q	–	70	90	mA	$I_Q = 550$ mA; $V_I = 5$ V
Drop voltage	V_{dr}	–	350	700	mV	$I_Q = 550$ mA[1]

Characteristics (cont'd)

V_I = 13.5 V; $-40\,°C \le T_j = \le 125\,°C$ (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Load regulation	ΔV_Q	–	25	50	mV	I_Q = 5 to 550 mA; V_I = 6 V
Supply voltage regulation	ΔV_Q	–	12	25	mV	V_I = 6 to 26 V I_Q = 5 mA
Power supply Ripple rejection	$PSRR$	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{SS}

Reset Generator

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Switching threshold	V_{RT}	4.5	4.65	4.8	V	–
Reset High voltage	V_{ROH}	4.5	–	–	V	–
Reset low voltage	V_{ROL}	–	60	–	mV	R_{intern} = 30 kΩ[2]; 1.0 V $\le V_Q \le$ 4.5 V
Reset low voltage	V_{ROL}	–	200	400	mV	I_R = 3 mA, V_Q = 4.4 V
Reset pull-up	R	18	30	46	kΩ	internally connected to Q
Lower reset timing threshold	V_{DRL}	0.2	0.45	0.8	V	$V_Q < V_{RT}$
Charge current	I_d	8	14	25	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.4	1.8	2.3	V	–
Delay time	t_d	–	13	–	ms	C_D = 100 nF
Reset reaction time	t_{RR}	–	–	3	µs	C_D = 100 nF

Overvoltage Protection

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Turn-Off voltage	$V_{I, ov}$	42	44	46	V	–

[1] Drop voltage = $V_I - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

[2] Reset peak is always lower than 1.0 V.
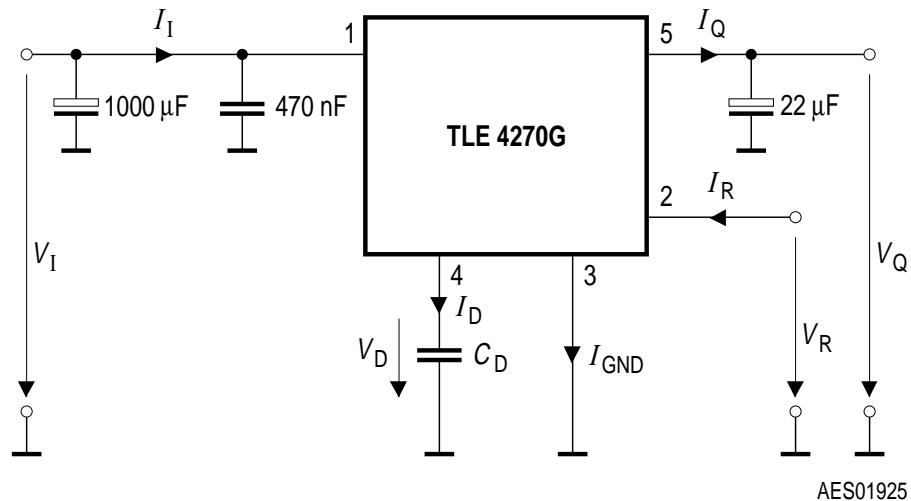
Figure 3
Test Circuit
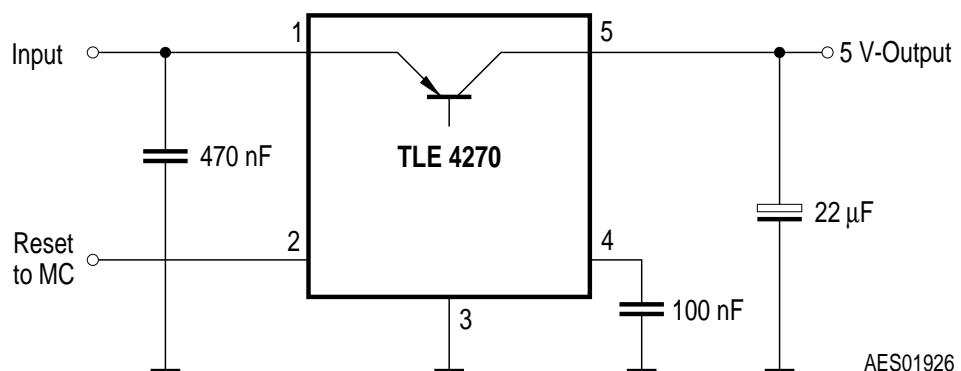

Figure 4
Application Circuit
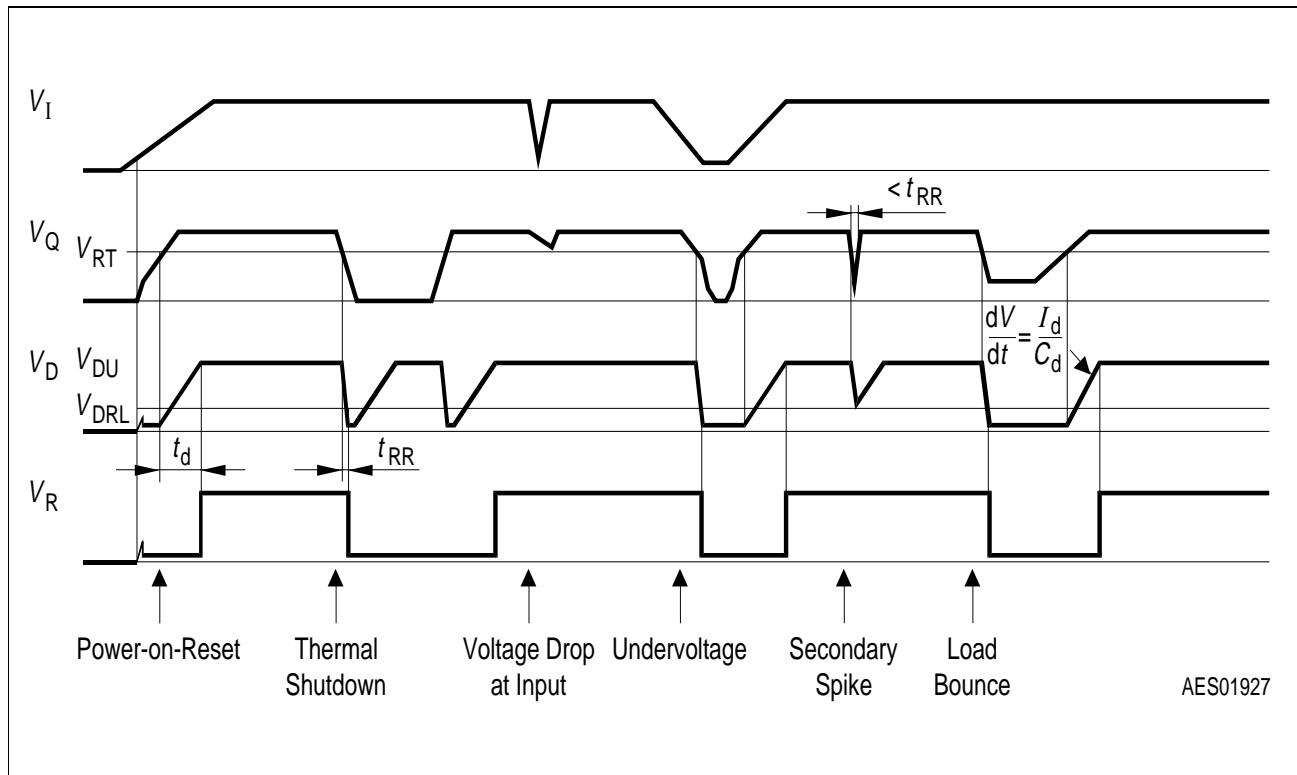
Figure 5
Time Response

Output Voltage V_Q versus Temperature T_j

AED01928

Graph: V_Q (V) vs T_j, y-axis from 4.60 to 5.20, x-axis from -40 to 160 °C. Curve labeled $V_I = 13.5$ V.
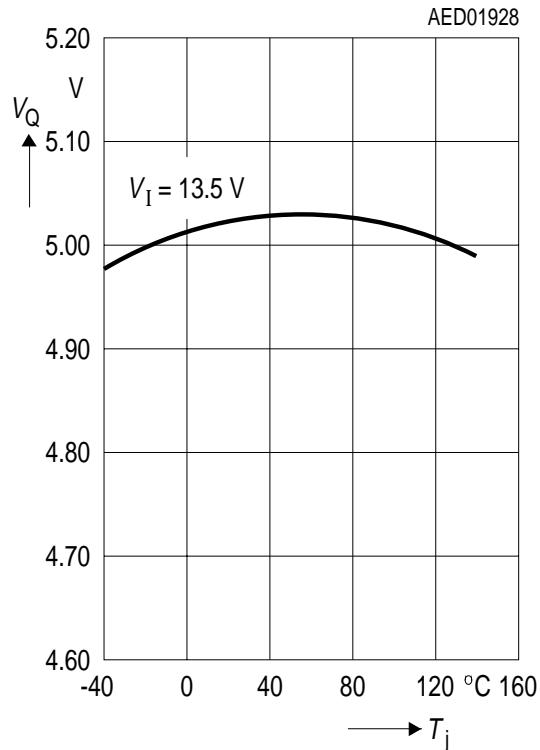
Output Voltage V_Q versus Input Voltage V_I

AED01929

Graph: V_Q (V) vs V_I, y-axis from 0 to 12, x-axis from 0 to 10 V. Curve labeled $R_L = 25\ \Omega$.
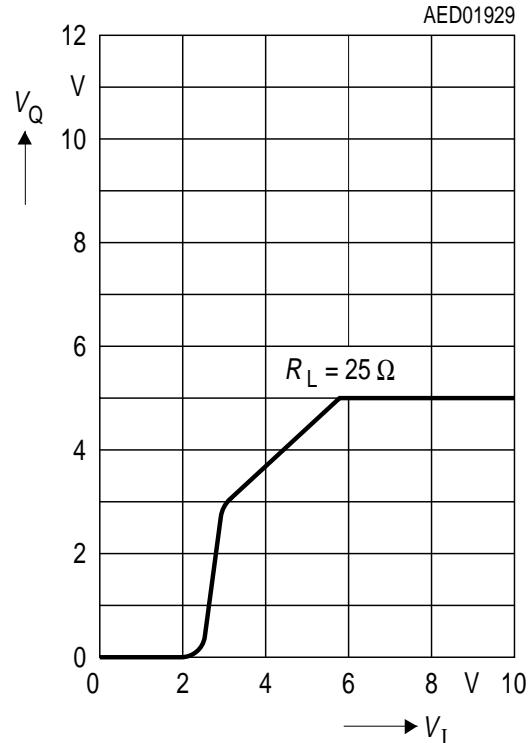
Output Current I_Q versus Temperature T_j

AED01930

Graph: I_Q (mA) vs T_j, y-axis from 0 to 1200 mA, x-axis from -40 to 160 °C.
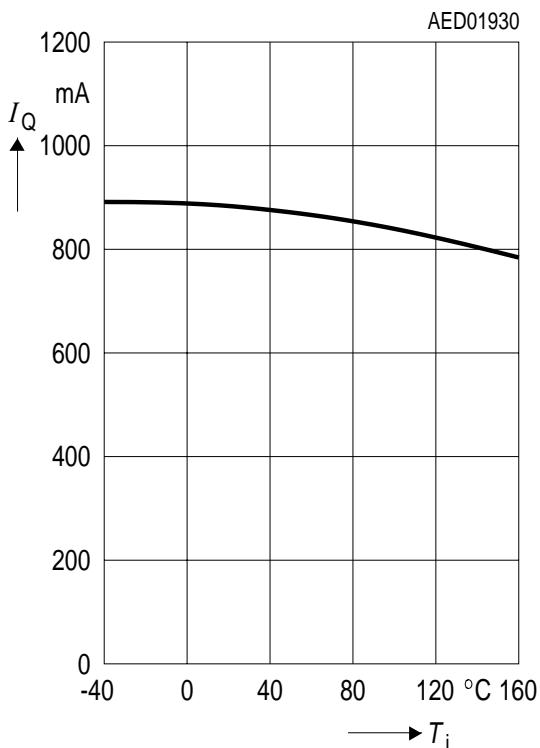
Output Current I_Q versus Input Voltage V_I
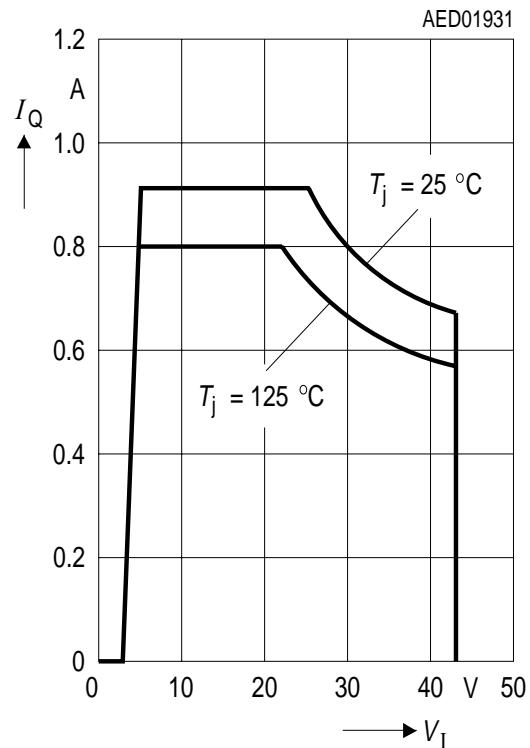
AED01931

Graph: I_Q (A) vs V_I, y-axis from 0 to 1.2 A, x-axis from 0 to 50 V. Curves labeled $T_j = 25\ ^\circ C$ and $T_j = 125\ ^\circ C$.

Current Consumption I_q versus Output Current I_Q

AED01932

$V_I = 13.5$ V

Current Consumption I_q versus Output Current I_Q

AED01933

$V_I = 13.5$ V
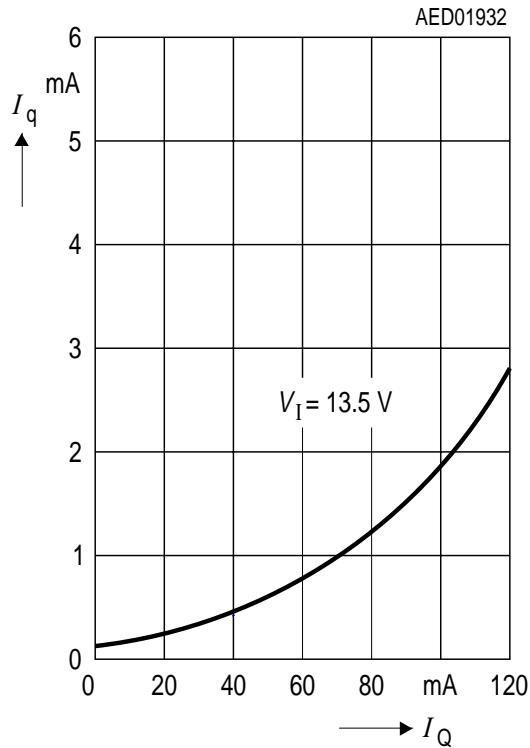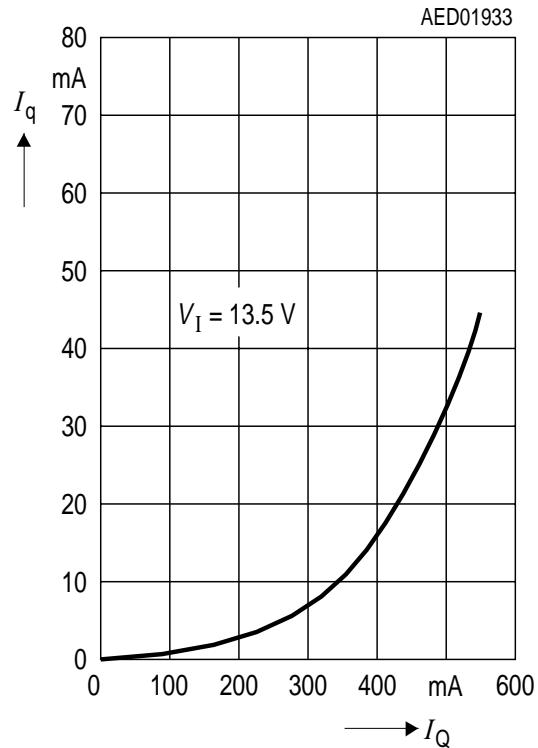
Current Consumption I_q versus Input Voltage V_I

AED01934

$R_L = 10$ Ω

$R_L = 20$ Ω $R_L = 50$ Ω
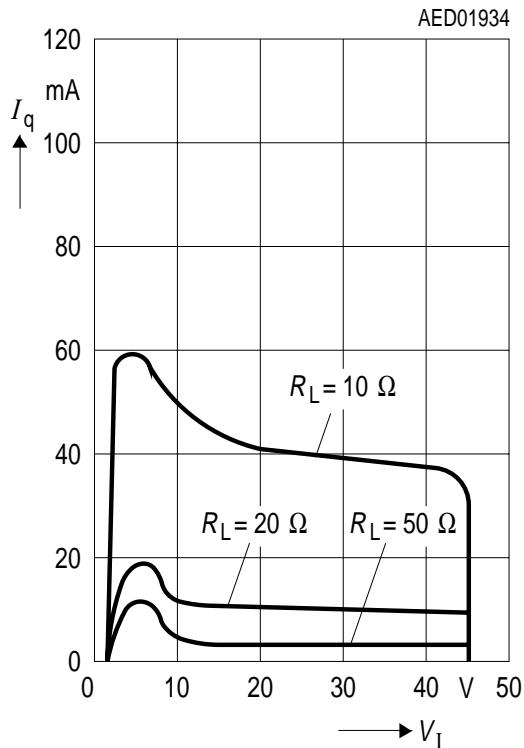
Drop Voltage V_{dr} versus Output Current I_Q

AED01935

$T_j = 125$ °C

$T_j = 25$ °C
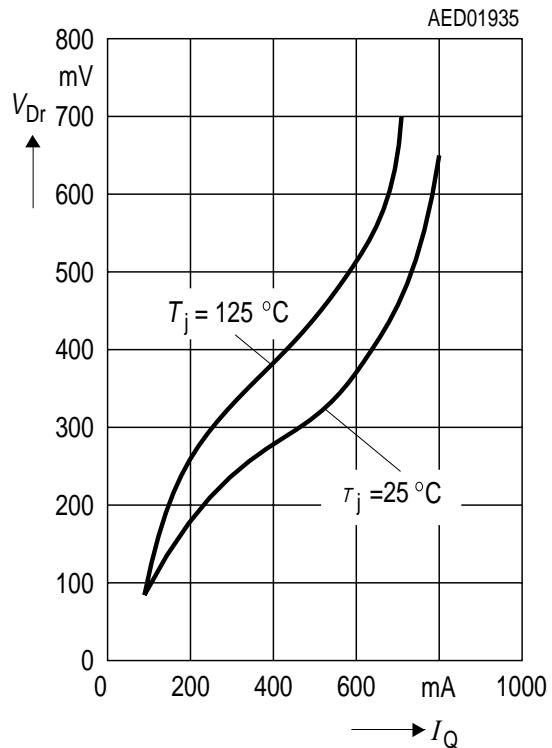
Charge Current I_d
versus Temperature T_j

AED01936
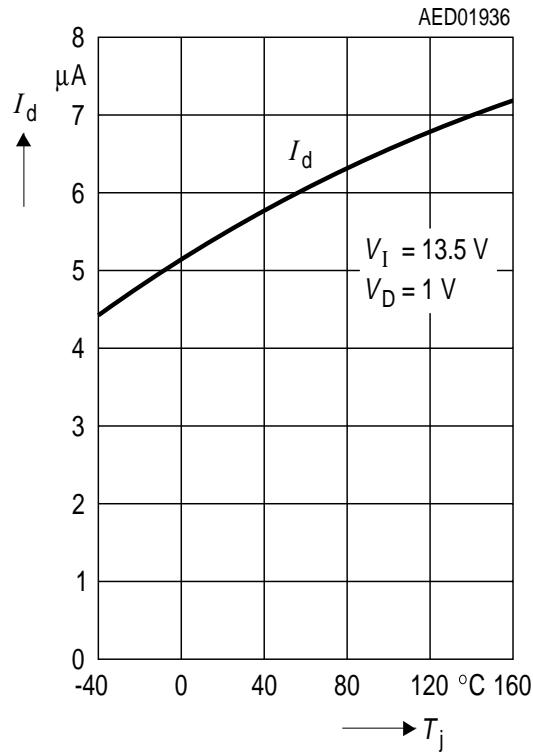
Delay Switching threshold V_{DU}
versus Temperature T_j

AED01937
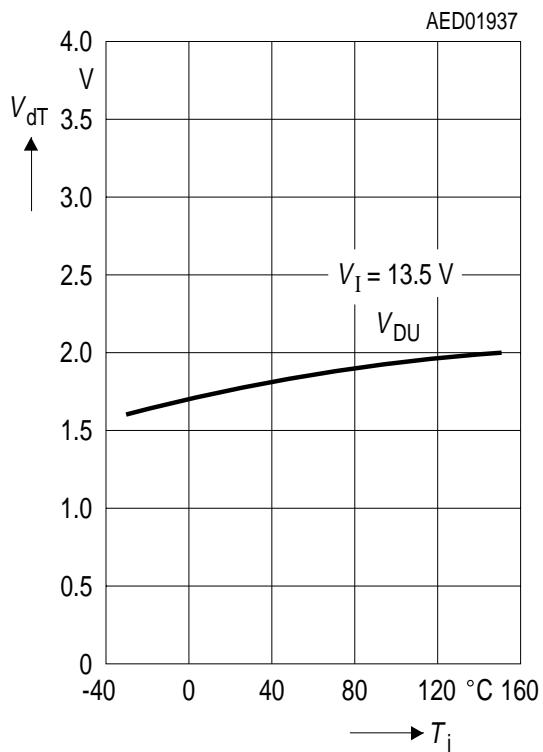
Package Outlines

P-TO220-5-1

(Plastic Transistor Single Outline)
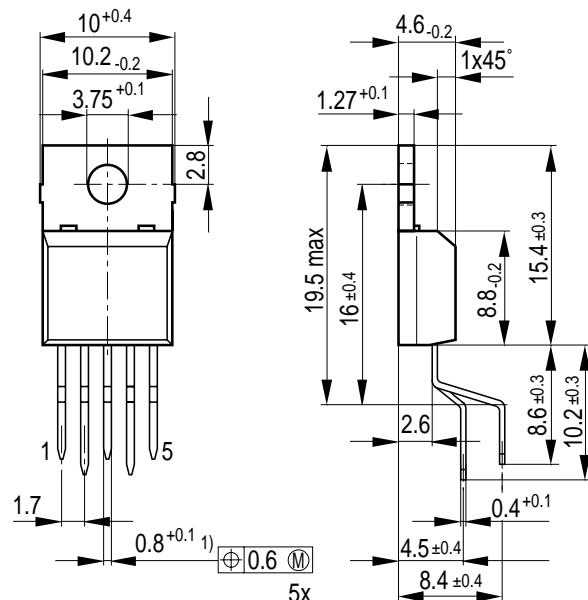
1) 1$_{-0.15}$ at dam bar (max 1.8 from body)

1) 1$_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

GPT05107

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

Dimensions in mm

P-TO220-5-2

(Plastic Transistor Single Outline)

$10^{+0.4}$
$10.2_{-0.2}$
$3.75^{+0.1}$
2.8
$4.6_{-0.2}$
$1 \times 45°$
$1.27^{+0.1}$
15.4 ± 0.3
$8.8_{-0.2}$
10.9 ± 0.2
12.9 ± 0.2
1
5
1.7
$0.8^{+0.1\ 1)}$
$\oplus$ 0.6 Ⓜ
5x
$0.4^{+0.1}$
2.6 ± 0.15
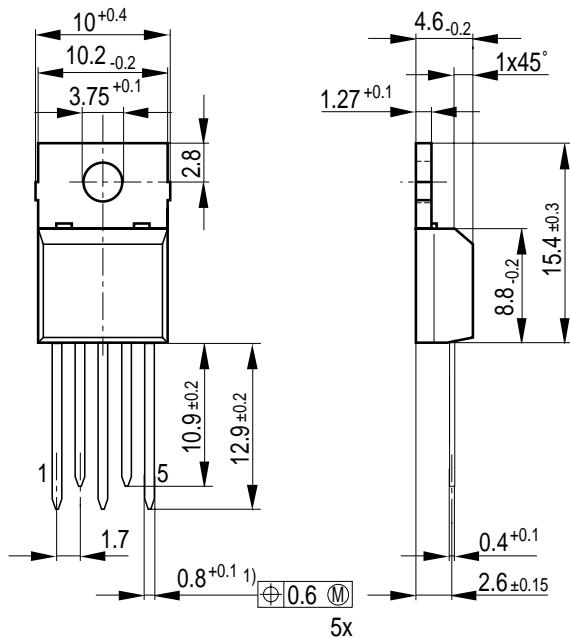
1) $1_{-0.15}$ at dam bar (max 1.8 from body)

1) $1_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

GPT05256

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

Dimensions in mm

P-TO220-5-11

(Plastic Transistor Single Outline)

10 ±0.2 $\boxed{A}$

9.8 ±0.15

8.5 [1]

3.7 -0.15

17 ±0.3

15.65 ±0.3

13.4 [1]

2.8 ±0.2

$\boxed{C}$

8.6 ±0.3

10.2 ±0.3

0...0.15

0.8 ±0.1

$\boxed{1.7}$

$\boxed{\oplus \; 0.25 \; \text{Ⓜ} \; A \; C}$

4.4

1.27 ±0.1

$\boxed{\square \; 0.05}$

9.25 ±0.2

3.7 ±0.3

0.5 ±0.1

$\boxed{2.4}$

3.9 ±0.4

8.4 ±0.4
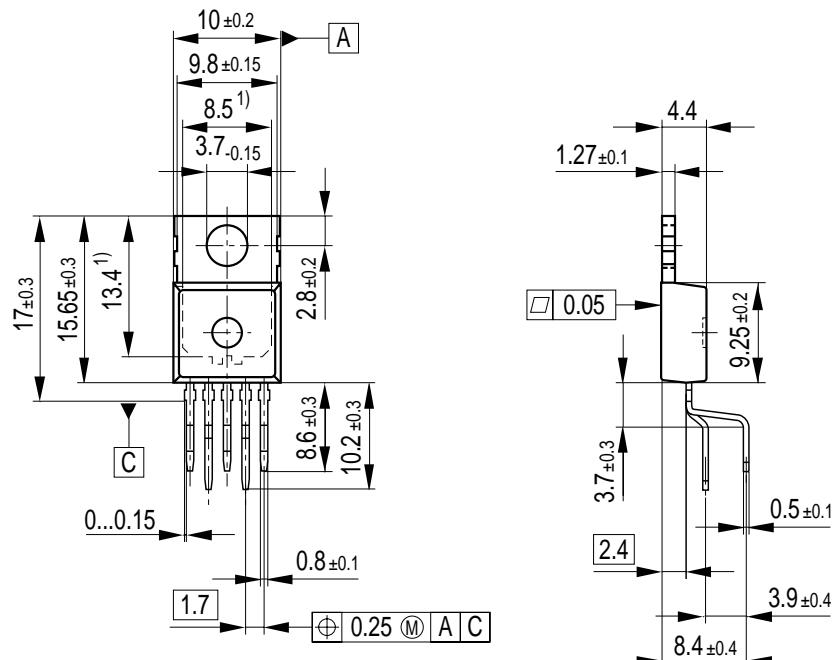
[1] Typical

All metal surfaces tin plated, except area of cut.

GPT09064

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

Dimensions in mm

P-TO220-5-12

(Plastic Transistor Single Outline)
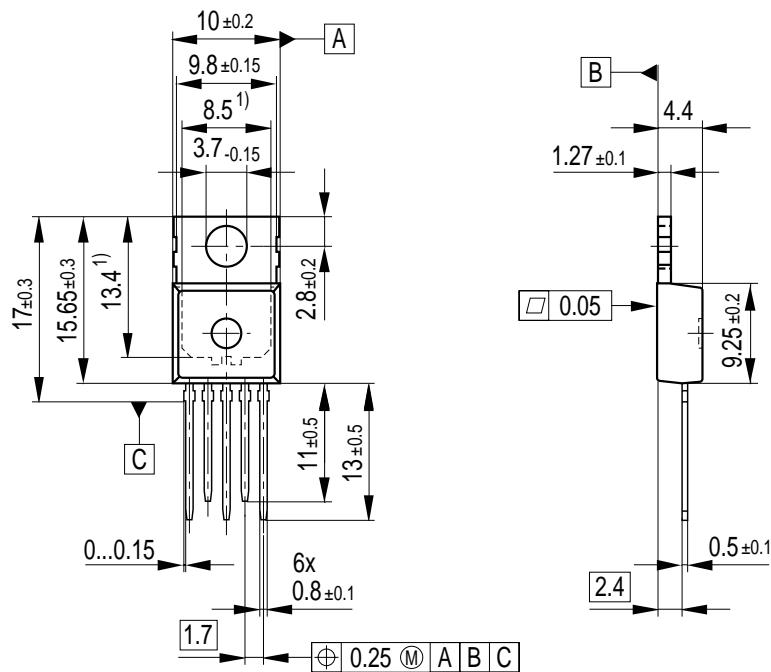
Typical

1) All metal surfaces tin plated, except area of cut.

GPT09065

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

Dimensions in mm

P-TO263-5-1
(Plastic Transistor Single Outline)

10 ±0.2
9.8 ±0.15
A
8.5 [1]
1 ±0.3
9.25 ±0.2
(15)
8 [1]
0...0.15
5x0.8 ±0.1
4x1.7
⊕ 0.25 Ⓜ A B

4.4
1.27 ±0.1
B
0.1
☐ 0.05
2.4
4.7 ±0.5
2.7 ±0.3
0.5 ±0.1
8° max.
△ 0.1

[1] Typical
All metal surfaces tin plated, except area of cut.
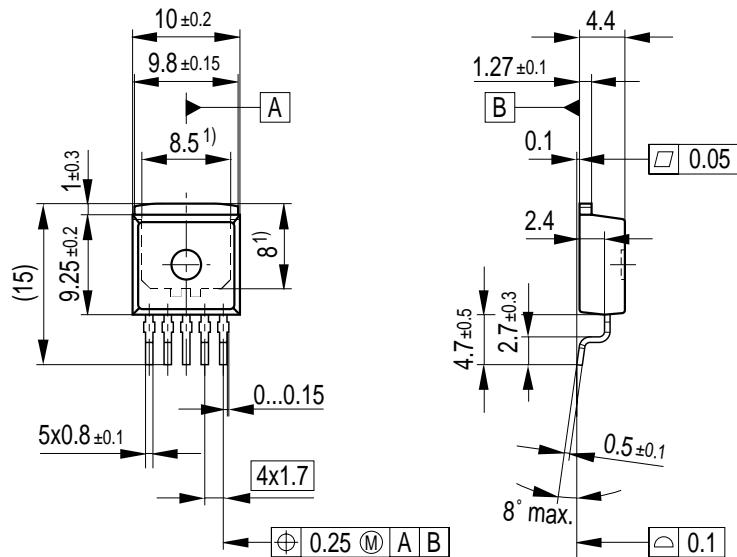
GPT09113

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

P-TO220-5-8

(Plastic Transistor Single Outline)

10.2

8.0

10.1

0.8

1.7

4 x 1.7 = 6.8

4.6

1.27

0.2

2.6

1)

8.8

3.5

1.5

0.4

GPT05873
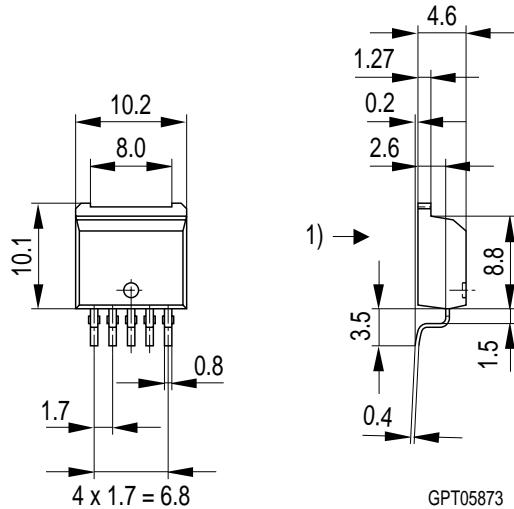
1) shear and punch direction burr free surface

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-TO252-5-1
(Plastic Transistor Single Outline)

All metal surfaces tin plated, except area of cut.

GPT09161

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm