

# DATA SHEET

## **TDA8505** SECAM encoder

Preliminary specification  
Supersedes data of May 1993  
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**Philips Semiconductors**



**PHILIPS**

# SECAM encoder

# TDA8505

## FEATURES

- Two input stages, R, G, B and Y,  $-(R-Y)$ ,  $-(B-Y)$  with multiplexing.
- Chrominance processing, highly integrated, includes vertical identification, low frequency pre-emphasis and high frequency pre-emphasis (anti-Cloche) and bandpass filter.
- Fully controlled FM modulator which produces a signal in accordance with the SECAM standard without adjustments.
- Two reference oscillators, one for D'R  $f_0$  (4.40625 MHz) and one for D'B  $f_0$  (4.250 MHz). These oscillators are tuned by PLL loop with the frequency of the line sync as reference. Crystal tuning, or tuning by external reference source, of the reference oscillators is possible.
- Output stages, CVBS and separated Y + SYNC and CHROMA. For CVBS output, signal amplitude 2 V (p-p) nominal, thus only an external emitter follower is required for 75  $\Omega$  driving.
- Sync separator circuit and pulse shaper, to generate the required pulses for the processing, line, frame, FH/2 and chrominance blanking.
- A 3-level sandcastle pulse is generated for PAL/NTSC to SECAM transcoding.
- FH/2 input for locking with another decoder.
- Colour killing on the internal colour difference signals.
- Internal bandgap reference.

## GENERAL DESCRIPTION

The TDA8505 is a highly integrated SECAM encoding IC that is designed for use in all applications that require transformation of R, G and B signals or Y, U and V signals to a standard SECAM signal.

The specification of the input signals is fully compatible with those of the TDA8501 PAL/NTSC encoder.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |              |          |          |
|-------------|---------|--------------|----------|----------|
|             | PINS    | PIN POSITION | MATERIAL | CODE     |
| TDA8505     | 32      | SDIP32       | plastic  | SOT232-1 |



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**PINNING**

D'R and D'B are the colour difference signals at the output of the multiplexer circuit;  $D'R = -1.9(R-Y)$  and  $D'B = +1.5(B-Y)$ , for an EBU bar of 75% the amplitudes are equal.

| SYMBOL             | PIN | DESCRIPTION  |
|--------------------|-----|--|
| $-(R-Y)$           | 1   | colour difference input signal, for EBU bar of 75% 1.05 V (peak-to-peak value)   |
| MCONTR             | 2   | multiplexer control; input HIGH = RGB, input LOW = $-(R-Y)$ , $-(B-Y)$ and Y   |
| $-(B-Y)$           | 3   | colour difference input signal, for EBU bar of 75% 1.33 V (peak-to-peak value)   |
| FH/2               | 4   | line pulse input divided-by-2 for synchronizing two or more encoders; when not used this pin is connected to ground  |
| Y                  | 5   | luminance input signal 1 V nominal without sync  |
| TEST               | 6   | test pin; must be connected to $V_{CC}$ (pin 8), or left open-circuit  |
| R                  | 7   | RED input signal for EBU bar of 75% 0.7 V (peak-to-peak value)   |
| $V_{DDA}$          | 8   | analog supply voltage for encoder part; 5 V nominal  |
| G                  | 9   | GREEN input signal for EBU bar of 75% 0.7 V (peak-to-peak value)   |
| $V_{SSA}$          | 10  | analog ground  |
| B                  | 11  | BLUE input signal for EBU bar of 75% 0.7 V (peak-to-peak value)  |
| Y/Y+SYNC           | 12  | when this control input is LOW, Y without sync is connected to pin 5, input blanking at pin 5 is active; when input is HIGH, Y+SYNC is connected to pin 5, input blanking at pin 5 is not active |
| LPFDR              | 13  | modulator control loop filter output; black level of D'R = 4.40625 MHz   |
| FADJ               | 14  | adjustment pin for 4.286 MHz of HF pre-emphasis filter   |
| LPFDB              | 15  | modulator control loop filter output; black level of D'B = 4.250 MHz   |
| FLT                | 16  | filter tuning loop capacitor output  |
| $V_{ref}$          | 17  | 2.5 V internal reference voltage output  |
| CHROMA             | 18  | chrominance output, amplitude corresponds with Y+SYNC at the output of the delay line  |
| $V_{ext}$          | 19  | external power supply for sandcastle generation; when not used this pin is connected to ground   |
| SAND               | 20  | 3-level sandcastle output pulse  |
| CVBS               | 21  | composite SECAM output 2 V (peak-to-peak value) nominal  |
| NOTCH              | 22  | Y+SYNC output after an internal resistor of 2 k $\Omega$ ; a notch filter can be connected   |
| Y+SYNC IN          | 23  | Y+SYNC input, connected to the output of the delay line  |
| LPF4.4             | 24  | loop filter output for 4.40625 MHz reference oscillator  |
| Y+SYNC OUT         | 25  | Y+SYNC output, 2 V (peak-to-peak value) nominal, connected to the input of the delay line  |
| XTAL/PLL<br>VIDENT | 26  | control pin; input HIGH = crystal tuning, input LOW = PLL tuning, both <b>without</b> vertical identification, 2.5 V = PLL tuning <b>with</b> vertical identification                            |
| VCO4.25            | 27  | when used for PLL tuning a capacitor is connected; when used for crystal tuning a crystal has to be connected (in series with a capacitor)   |
| COLKIL             | 28  | colour killing; input HIGH = active, internal colour difference signals are blanked  |
| CS                 | 29  | composite sync input, 0.3 V (peak-to-peak value) nominal   |

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| SYMBOL           | PIN | DESCRIPTION  |
|------------------|-----|--|
| V <sub>SSD</sub> | 30  | digital ground   |
| LPF4.25          | 31  | loop filter output for 4.25 MHz reference oscillator; connected to pin 17 (V <sub>ref</sub> ) when external tuning by crystal or signal source |
| V <sub>DDD</sub> | 32  | supply voltage for the digital part  |

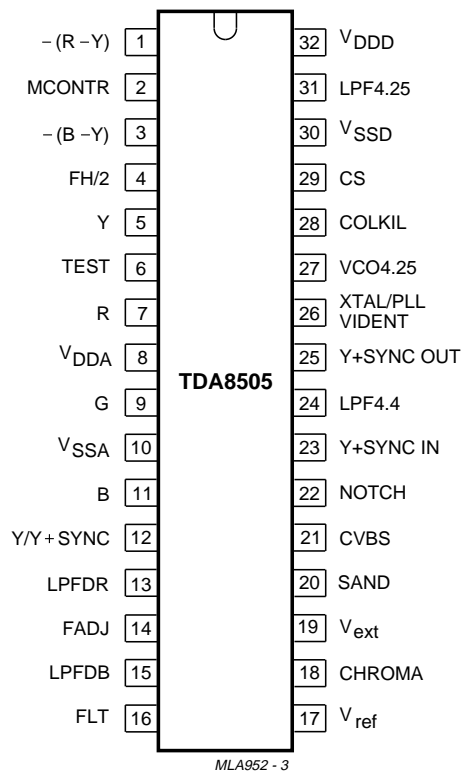


Fig.2 Pin configuration.

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### FUNCTIONAL DESCRIPTION

The following three important circuits are integrated:

- Encoder circuit
- Modulator control circuit
- Sync separator and pulse shaper.

#### Encoder circuit

##### INPUT STAGE

R, G and B inputs are connected to the matrix via a clamping and a blanking circuit.

For an EBU colour bar of 75% the amplitude of the signal must be 0.7 V (peak-to-peak value). The outputs of the matrix are Y, D'R and D'B.

The second part of the input stage contains inputs for colour difference signals and a luminance signal. The condition for 75% colour bar is  
 $-(R-Y) = 1.05\text{ V}$  (peak-to-peak value) at pin 1,  
 $-(B-Y) = 1.33\text{ V}$  (peak-to-peak value) at pin 3 and  
 $Y = 1\text{ V}$  (peak-to-peak value) without sync at pin 5. After clamping and blanking the amplitude and polarity are corrected such that the signals are equal to the signals of the matrix output. Signals are connected to a switch. Fast switching between the two input parts is possible by the multiplexer control pin (pin 2).

The Y output signal of the multiplexer is added to the sync pulse of the sync separator.

The Y input (pin 5) is different to the other 5 inputs. The timing of the internal clamping is after the sync period and there is no vertical blanking.

The input blanking of Y can be switched off by a HIGH at pin 12, and the internal sync separator signal is not added to the Y signal. In this way the Y+SYNC is allowed at pin 5 and after clamping internally connected directly to pin 25.

The colour difference signals are switched sequentially by H/2 and fed to the low frequency pre-emphasis circuit.

The colour-killing input signal at pin 28 can be used for completely blanking the internal colour difference signals at the input of the low frequency pre-emphasis filter.

##### LOW FREQUENCY PRE-EMPHASIS

This filter is fully integrated, Fig.3 illustrates the nominal response.

The transfer is guaranteed within the illustrated area for the whole ambient temperature range by a compensation circuit.

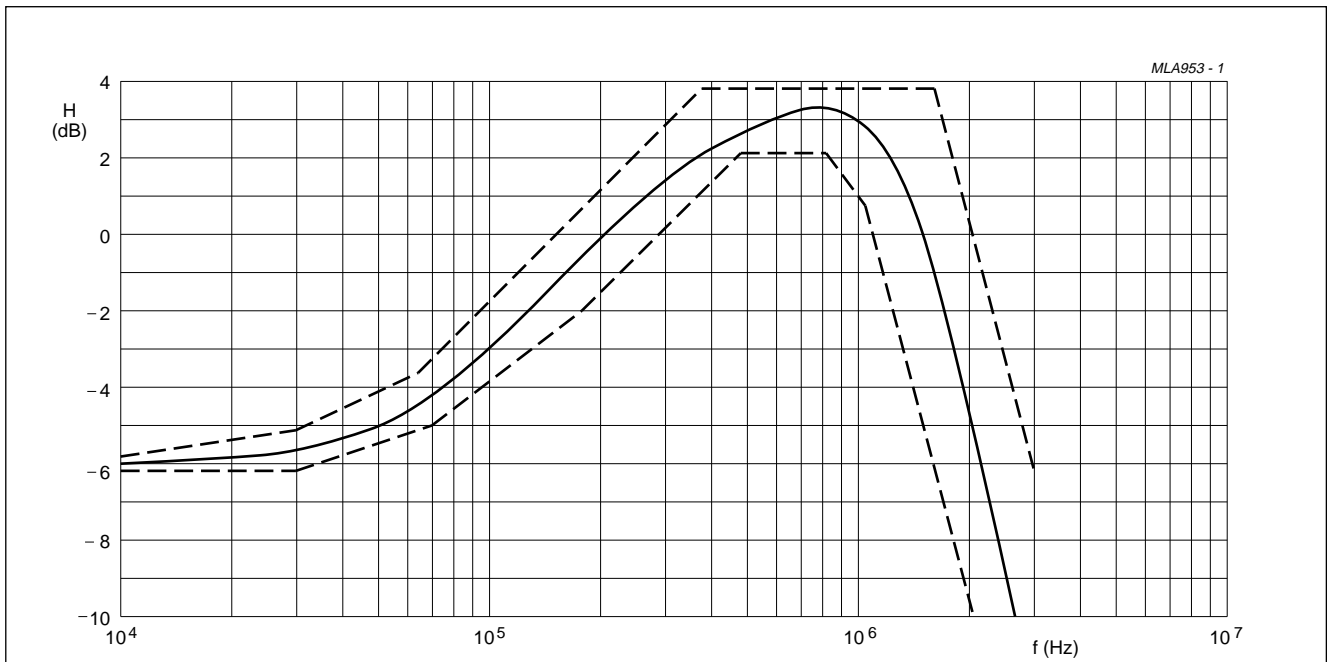


Fig.3 Nominal response for the low frequency pre-emphasis filter.

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### VERTICAL IDENTIFICATION

After the low frequency pre-emphasis the signal is clamped and, if desired the vertical identification sawtooth waveform can be added. The generation of the vertical identification is switched on/off by the logic level input at pin 26.

Figure 4 shows the sawtooth waveform at the input of the FM modulator with the corresponding frequency values after modulation.

**Vertical identification is only possible if PLL tuning is selected.**

### GAIN + LIMITER

The gain of this amplifier is sequentially switched, so that the amplitude of D'R is 280/230 times the amplitude of D'B (based on an EBU colour bar). The signal is limited at a lower and upper level to ensure that the FM modulator frequencies are always between 3.9 MHz and 4.756 MHz. A DC offset between D'R and D'B is added which corresponds with the limiter levels.

### FM MODULATOR

The signal of the gain + limiter stage is fed to the FM modulator.

The modulator control adjusts the DC level at pin 13 to set the frequency of the FM signal to 4.406 MHz at the black

level of D'R. The modulator control also sets the DC level at pin 15 to adjust the FM frequency to 4.250 MHz at the black level of D'B.

At the start of every line the FM modulator is stopped and is started again by a short duration pulse of the pulse shaper. These stop/start pulses are operating such that after two lines starting in the same phase, the start phase of the third line is shifted 180 degrees. This sequence is inverted during each vertical blanking.

The FM signal is fed to the internal HF pre-emphasis filter.

### HF PRE-EMPHASIS AND BANDPASS FILTER

An HF pre-emphasis filter combined with a bandpass filter is integrated.

Figures 5 and 6 illustrate the frequency response. Two resistors in series with a potentiometer at pin 14 adjusts the frequency to 4.286 MHz with a tolerance of  $\pm 20$  kHz.

A tuning circuit integrated with an external capacitor connected to pin 16 guarantees a stable frequency response for the whole temperature range.

The output of the bandpass filter is connected directly to the chrominance blanking circuit.

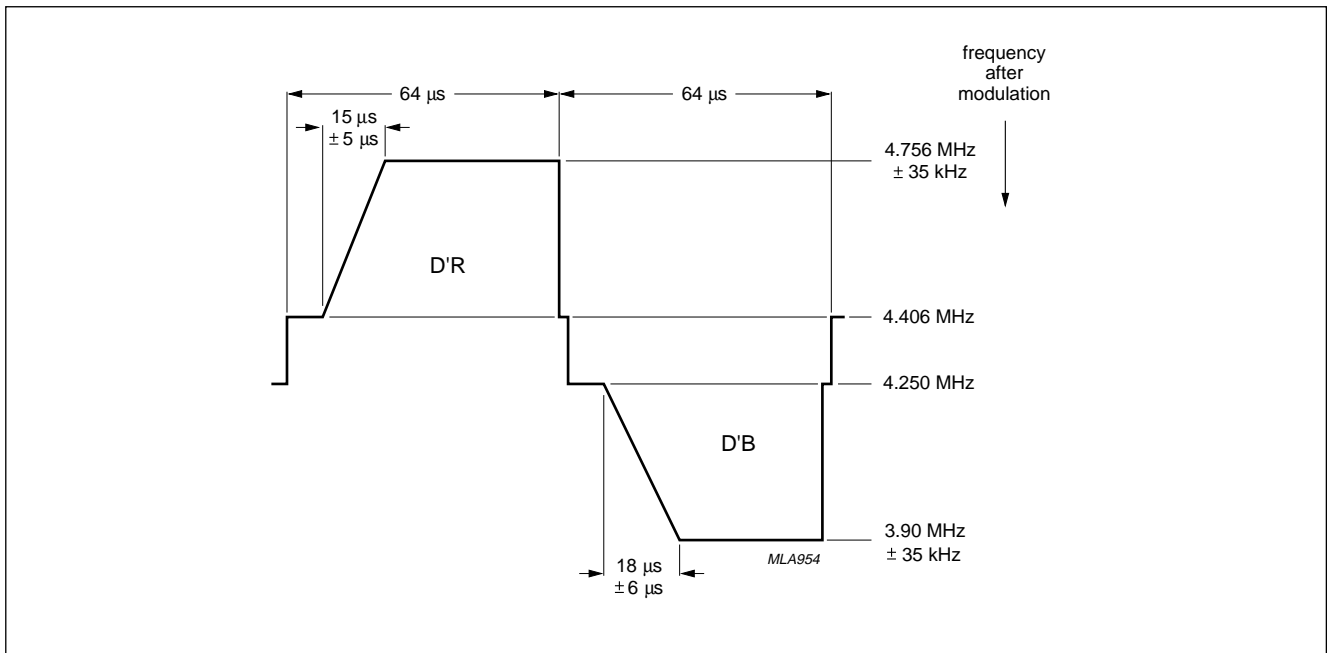


Fig.4 Vertical identification sawtooth waveform input.

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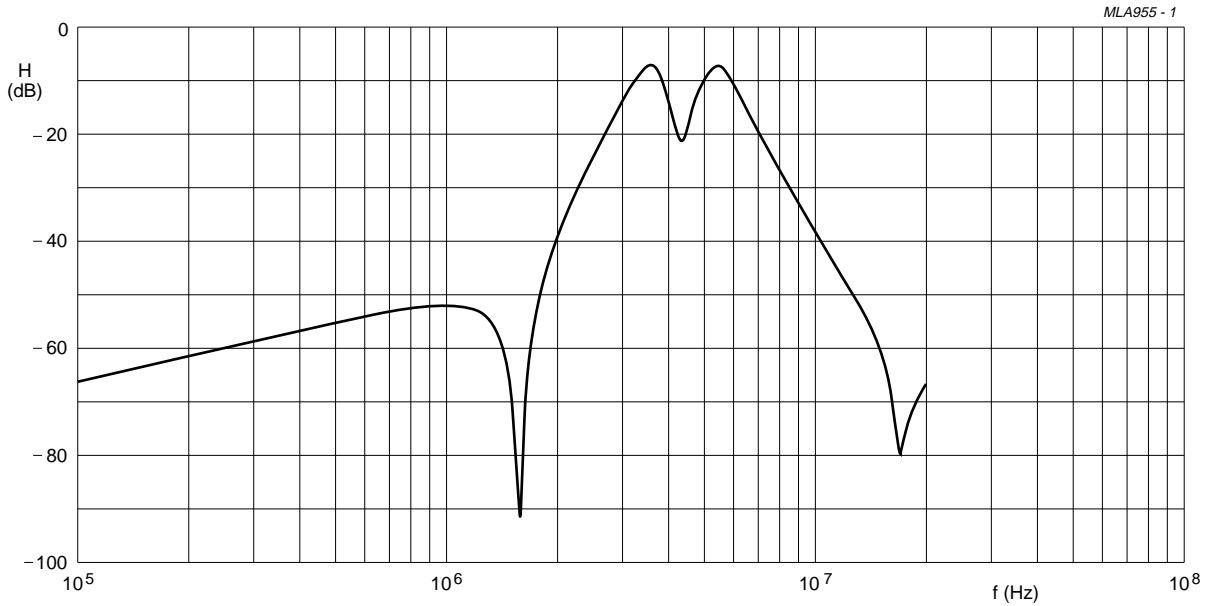


Fig.5 Frequency response of the HF pre-emphasis and bandpass filter; H as a function of frequency (1).

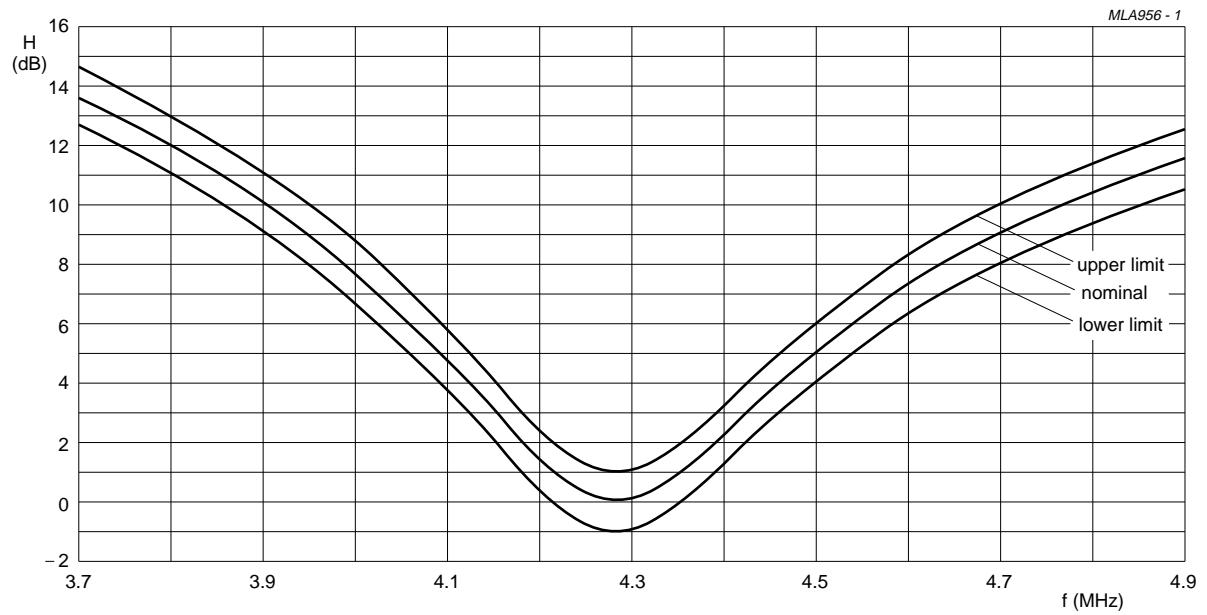


Fig.6 Frequency response of the HF pre-emphasis and bandpass filter; H as a function of frequency (2).



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CHROMINANCE BLANKING

The chrominance signal is blanked by the internally generated chrominance blanking pulse. The output of this blanking stage is connected to the chrominance and CVBS output circuits.

Y+SYNC, CVBS, AND CHROMA OUTPUTS

The Y output signal of the matrix is added to the composite sync signal of the sync separator. The output of this adder at pin 25 is connected to the input of an external delay line which is necessary for correct timing of the Y+SYNC signal corresponding with the chrominance signal. The signal amplitude at pin 25 is 2 V (peak-to-peak value) nominal, so at the output of the delay line Y+SYNC is 1 V (peak-to-peak value).

**The delay line has to be DC-coupled between pins 25 and 23 to ensure the required DC level at pin 23. The output resistor of the delay line has to be connected to pin 17 where ( $V_{ref} = 2.5 V$ ).**

The output of the delay line is connected to pin 23 which is the input of a buffer operational amplifier. The output of the buffer operational amplifier is connected to pin 22 and to the CVBS adder stage via an internal resistor of 2 kΩ. An external notch filter can be connected to pin 22. The CVBS signal amplitude output at pin 21 is 2 V (peak-to-peak value) nominal. An external emitter follower is used to provide a 75 Ω output load.

The amplitude of the chrominance output signal which is connected to pin 18 corresponds with the Y+SYNC signal at the output of the delay line.

**Modulator control circuit**

The modulator control circuit has two tuning modes which are controlled by the input at pin 26:

- Tuning by line frequency
- Tuning by crystal or external signal source.

TUNING BY LINE FREQUENCY

Two reference voltage controlled oscillators (VCOs) are integrated, the 4.4 MHz VCO with an internal capacitor and the 4.25 MHz VCO with an external capacitor at pin 27.

A PLL loop with divider circuits directly couples the frequencies of the two VCOs with the line frequency of the sync separator sync signal.

The loop filter for the 4.40625 MHz reference is at pin 24 and the loop filter for the 4.250 MHz reference is at pin 31.

The outputs of the 272 divider are also used for pulse shaping.

Within the vertical blanking period, another two Phase Locked Loops (PLLs) synchronizes the FM modulator during two lines with the 4.406 MHz reference VCO and during the following 2 lines with the 4.250 MHz reference VCO. The loop filters are connected to pins 13 and 15 respectively.

**It is necessary to use low-leakage capacitors for these loop filters.**

TUNING BY CRYSTAL OR EXTERNAL SIGNAL SOURCE

When the frequency of the sync pulse at pin 29 is not stable or is incorrect it is possible to tune the FM modulator using an external 4.250 MHz crystal connected to pin 27. The 4.25 MHz loop at pin 31 has to be connected to pin 17 ( $V_{ref}$ ). A stable line frequency reference is generated by the 272 divider circuit which is used for the 4.406 MHz reference loop.

An external signal source, instead of a crystal, can be connected at pin 27 via a capacitor in series with a resistor.

The minimum AC current of 50 μA is determined by the resistor values ( $R_{int} + R_{ext}$ ) and the output voltage of the signal source (see Fig.7).

**When crystal tuning is used no vertical identification is possible.**

Crystal tuning is recommended for VTR signals.

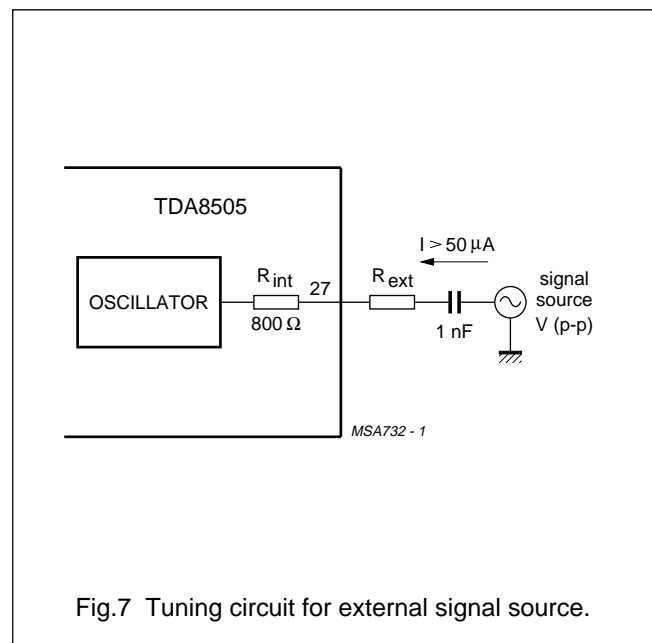


Fig.7 Tuning circuit for external signal source.

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**Sync separator and pulse shaper**

The composite sync input at pin 29 together with the outputs of the 272 divider of the 4.250 MHz reference loop are the sources for all pulses necessary for the processing.

The pulses are used for:

- Clamping
- Video blanking
- FH/2
- Chrominance blanking
- Stop/start of modulator
- Vertical identification
- Timing for the modulator control
- Sandcastle pulse shaping at pin 20.

External FH/2 at pin 4 is only necessary when two or more SECAM encoders have to be locked in the same phase. The phase of the internal FH/2 can be locked with an external FH/2 connected at pin 4. A reset of the internal FH/2 is possible by forcing pin 4 to a HIGH level. This HIGH level corresponds with D'R. Pin 4 is connected to ground when not used.

Figures 9 and 10 show the generated pulses during vertical blanking for PLL tuning or crystal tuning respectively. Figure 11 shows the pulses during line blanking.

**Transcoding application**

A sandcastle pulse is necessary for the PAL/NTSC demodulator (i.e. TDA4510) for transcoding PAL or NTSC to SECAM.

Most of the demodulator ICs use a sandcastle pulse with an amplitude of 12 V or 8 V. A 12 V or 8 V sandcastle is not possible with the TDA8505 because of the 5 V power supply.

To generate a 3-level sandcastle pulse at pin 20 (see Fig.8) an external supply voltage must be connected to pin 19.

The PAL or NTSC CVBS signal is connected to the composite sync input (pin 29) for PLL tuning and pulse shaping. As previously mentioned the Y input at pin 5 can be used as the Y+SYNC input for the filtered Y+SYNC PAL or NTSC signal, when pin 12 is at a HIGH level.

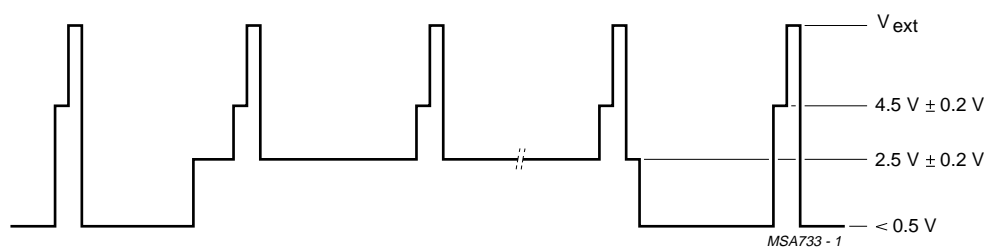


Fig.8 3-level sandcastle pulse.

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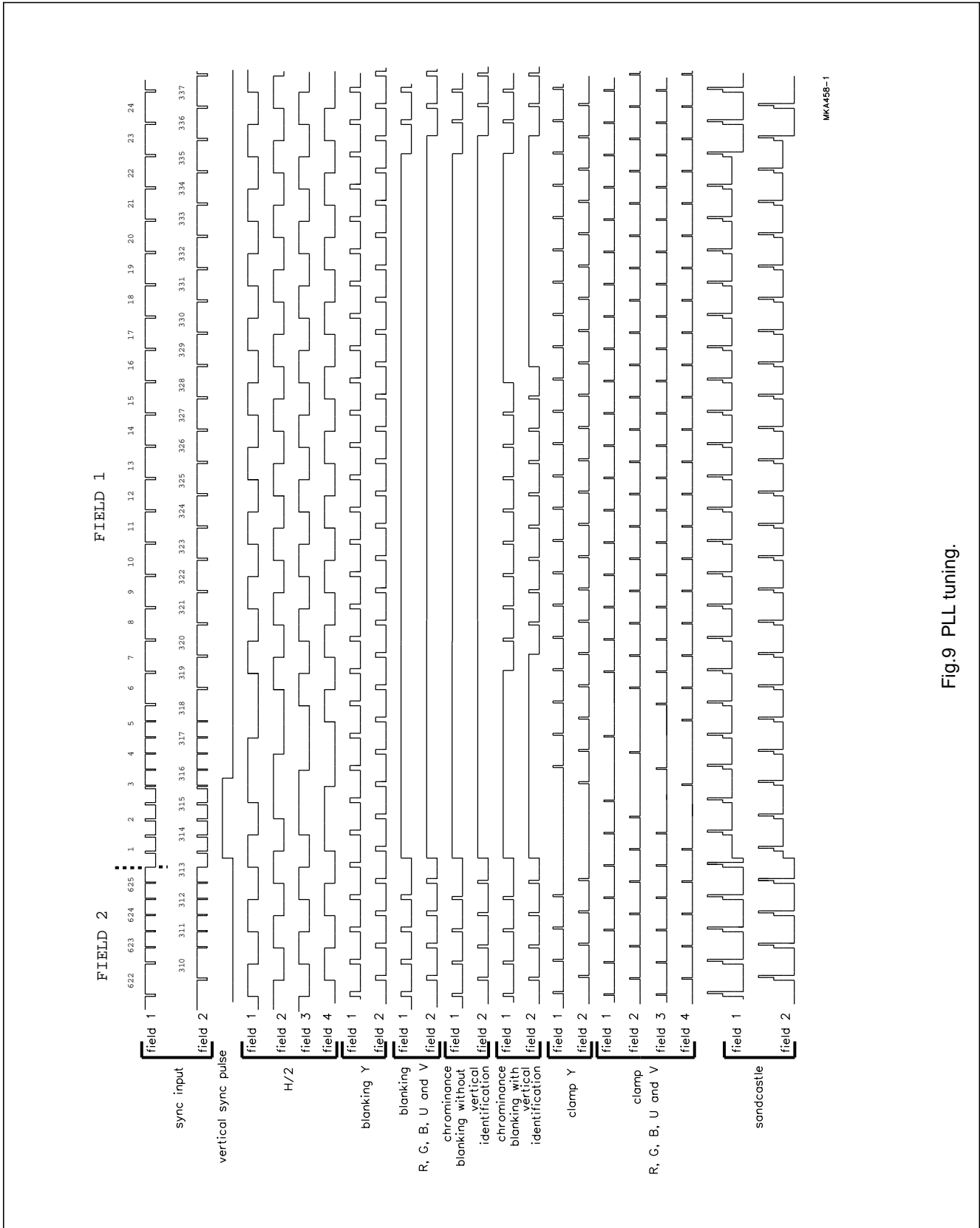


Fig.9 PLL tuning.

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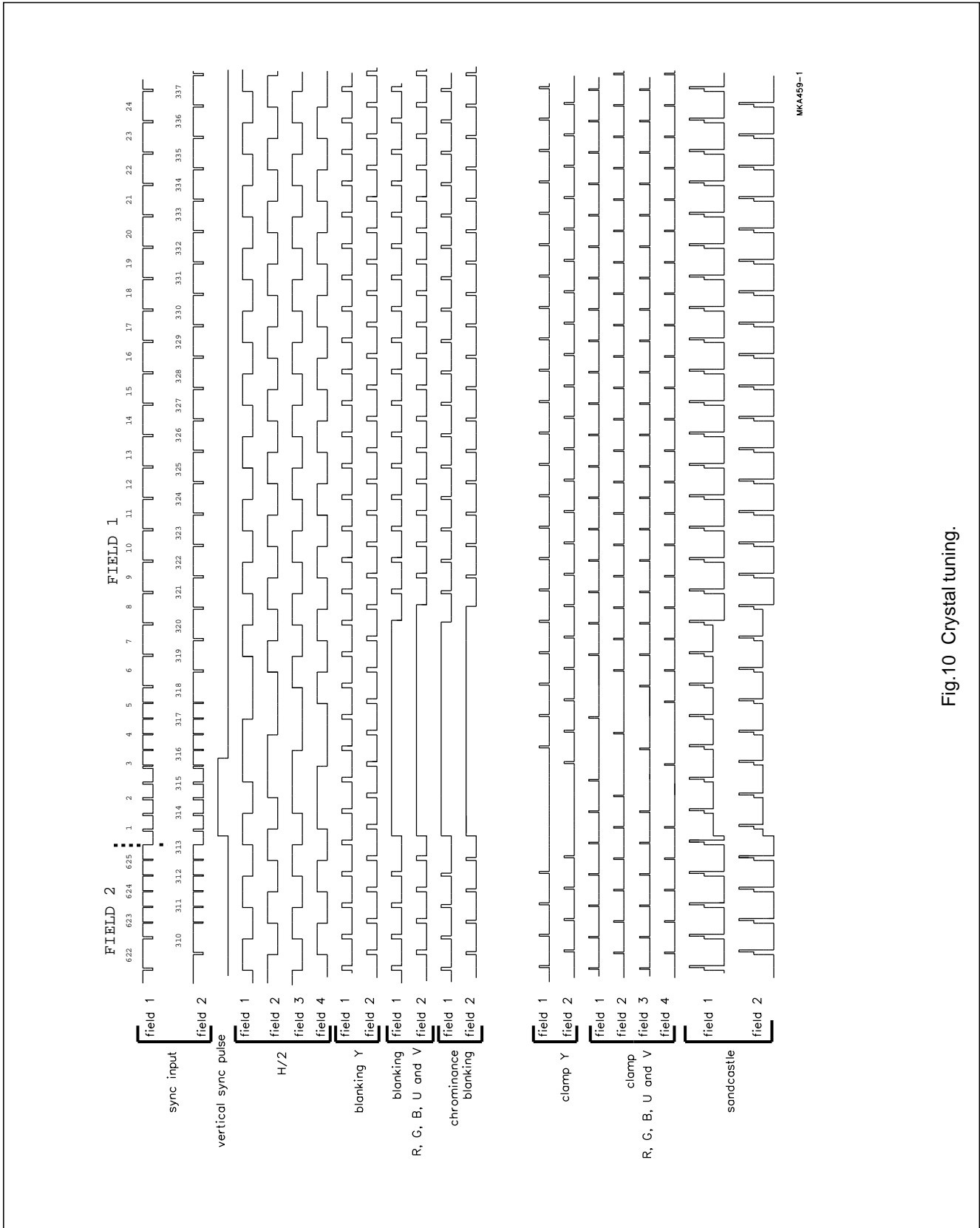
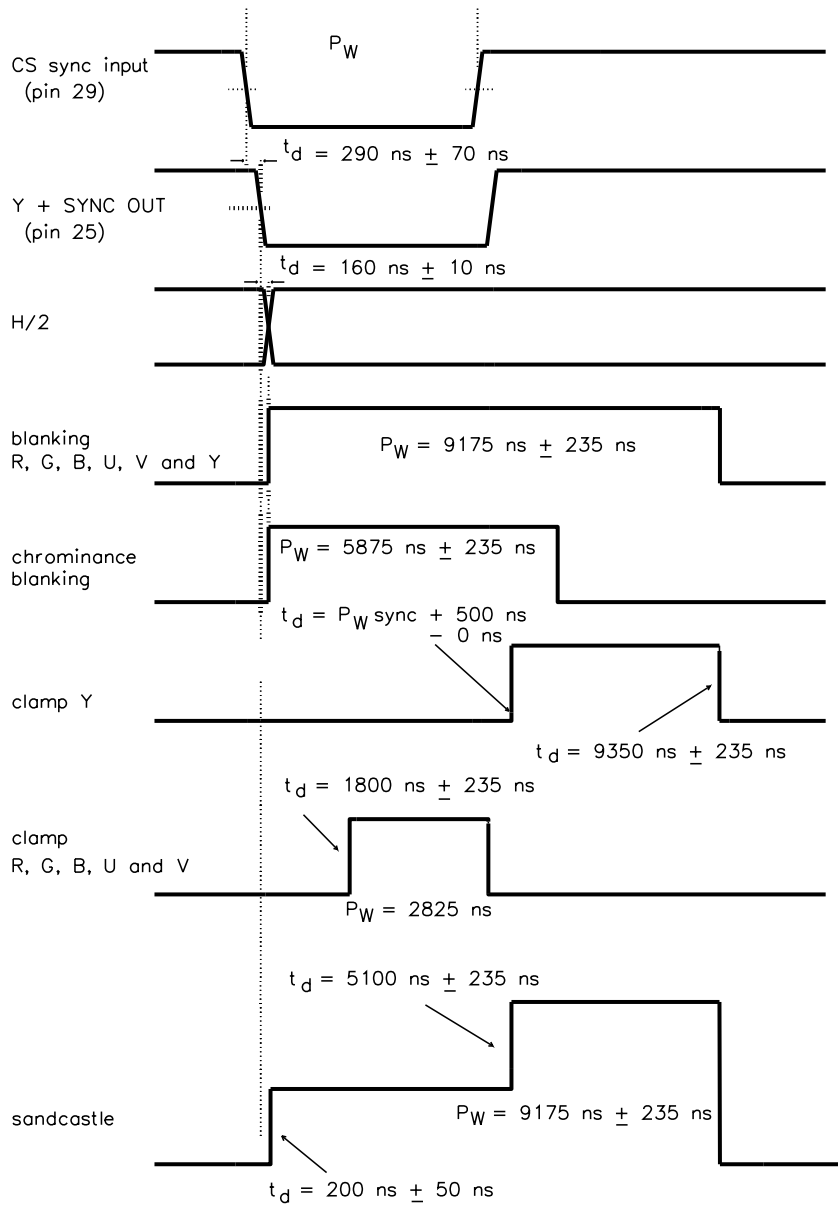


Fig.10 Crystal tuning.

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MKA460-1

Fig.11 Pulses during line blanking.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to  $V_{SSA}$  pin 10.

| SYMBOL    | PARAMETER   | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| $V_{DDA}$ | analog supply voltage for encoder part            | 0    | 5.5  | V    |
| $V_{DDD}$ | digital supply voltage                            | 0    | 5.5  | V    |
| $V_{ext}$ | external supply voltage for sandcastle generation | 0    | 13.2 | V    |
| $T_{stg}$ | storage temperature                               | -65  | +150 | °C   |
| $T_{amb}$ | operating ambient temperature                     | -25  | +70  | °C   |

**THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER   | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | 60    | K/W  |

**DC CHARACTERISTICS**

$V_{CC}$  and  $V_{DD} = 5$  V;  $T_{amb} = 25$  °C; all voltages referenced to pins 10 and 30; unless otherwise specified.

| SYMBOL    | PARAMETER   | MIN.  | TYP.    | MAX.  | UNIT |
|-----------|---|-------|---------|-------|------|
| $V_{DDA}$ | analog supply voltage for encoder part (pin 8)    | 4.5   | 5.0     | 5.5   | V    |
| $V_{DDD}$ | digital supply voltage (pin 32)                   | 4.5   | 5.0     | 5.5   | V    |
| $I_{DDA}$ | analog supply current                             | –     | 39      | –     | mA   |
| $I_{DDD}$ | digital supply current                            | –     | 4       | –     | mA   |
| $V_{ext}$ | external supply voltage for sandcastle generation | 0     | 8 to 12 | 13.2  | V    |
| $P_{tot}$ | total power dissipation                           | –     | 215     | –     | mW   |
| $V_{ref}$ | reference voltage output (pin 17)                 | 2.425 | 2.5     | 2.575 | V    |

**AC CHARACTERISTICS**

$V_{CC}$  and  $V_{DD} = 5$  V;  $T_{amb} = 25$  °C; composite sync signal connected to pin 29; unless otherwise specified.

| SYMBOL  | PARAMETER                         | CONDITIONS                          | MIN. | TYP.     | MAX. | UNIT |
|---|-----------------------------------|-------------------------------------|------|----------|------|------|
| <b>Encoder circuit: input stage (pins 1, 3, 5, 7, 9 and 11; black level = clamping level)</b> |                                   |                                     |      |          |      |      |
| $V_{n(max)}$  | voltage from black level positive |                                     | 1.2  | –        | –    | V    |
| $V_{n(min)}$  | voltage from black level negative | only pins 1, 3 and 5                | 0.9  | –        | –    | V    |
| $I_{bias(max)}$   | maximum input bias current        | $V_I = V_{17}$                      | –    | –        | 1    | μA   |
| $V_I$   | input voltage clamped             | input capacitor connected to ground | –    | $V_{17}$ | –    | V    |
| $Z_I$   | input clamping impedance          | $I_I = 1$ mA                        | –    | 80       | –    | Ω    |
|   |                                   | $I_O = 1$ mA                        | –    | 80       | –    | Ω    |

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| SYMBOL  | PARAMETER                                    | CONDITIONS  | MIN. | TYP.            | MAX. | UNIT   |
|---|--|---|------|-----------------|------|--------|
| <b>Multiplexer control (pin 2; note 1)</b>                                  |  |   |      |                 |      |        |
| V <sub>IL</sub>   | LOW level input voltage Y, -(R-Y) and -(B-Y) |   | 0    | –               | 0.4  | V      |
| V <sub>IH</sub>   | HIGH level input voltage R, G and B          |   | 1    | –               | 5    | V      |
| I <sub>I</sub>  | input current                                |   | –    | –               | –3   | μA     |
| t <sub>sw</sub>   | switching time                               |   | –    | 50              | –    | ns     |
| <b>Control input Y/Y+SYNC (pin 12)</b>                                      |  |   |      |                 |      |        |
| V <sub>IL</sub>   | LOW level input voltage                      | blanking pin 5 active; internal sync added to Y                               | 0    | –               | 1    | V      |
| V <sub>IH</sub>   | HIGH level input voltage                     | blanking pin 5 inactive; internal sync not added to Y                         | 4    | –               | 5    | V      |
| I <sub>I(max)</sub>   | maximum input current                        |   | –    | –               | 1    | μA     |
| <b>XTAL/PLL and VIDENT input (pin 26)</b>                                   |  |   |      |                 |      |        |
| V <sub>IL</sub>   | LOW level input voltage                      | PLL mode; vertical identification off   | 0    | –               | 1    | V      |
| V <sub>IH</sub>   | HIGH level input voltage                     | crystal tuning; vertical identification off                                   | 4    | –               | 5    | V      |
| V <sub>I</sub>  | input voltage                                | pin 26 connected to pin 17; PLL tuning; vertical identification on; see Fig.4 | –    | V <sub>17</sub> | –    | V      |
| I <sub>I</sub>  | input current                                |   | –    | –               | –6   | μA     |
| <b>COLKIL input (pin 28)</b>  |  |   |      |                 |      |        |
| V <sub>IL</sub>   | LOW level input voltage                      | inactive  | 0    | –               | 1    | V      |
| V <sub>IH</sub>   | HIGH level input voltage                     | active  | 4    | –               | 5    | V      |
| I <sub>I(max)</sub>   | maximum input current                        |   | –    | –               | 1    | μA     |
| <b>FH/2 input (pin 4)</b>   |  |   |      |                 |      |        |
| V <sub>IL</sub>   | LOW level input voltage                      | inactive  | 0    | –               | 1    | V      |
| V <sub>IH</sub>   | HIGH level input voltage                     | active  | 4    | –               | 5    | V      |
| I <sub>I(max)</sub>   | maximum input current                        |   | –    | –               | 1    | μA     |
| <b>LF pre-emphasis (see Fig.3)</b>  |  |   |      |                 |      |        |
| <b>HF pre-emphasis and bandpass (see Figs 5 and 6)</b>                      |  |   |      |                 |      |        |
| <b>FADJ input (pin 14) resistor value for correct adjustment; see Fig.1</b> |  |   |      |                 |      |        |
|   | input sensitivity                            |   | –    | 1.75            | –    | kHz/mV |
| I <sub>I(max)</sub>   | maximum input current                        |   | –    | –               | 100  | nA     |

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| SYMBOL                               | PARAMETER   | CONDITIONS  | MIN. | TYP.            | MAX. | UNIT     |
|--------------------------------------|---|---|------|-----------------|------|----------|
| <b>FLT output (pin 16)</b>           |   |   |      |                 |      |          |
| V <sub>DCL</sub>                     | limited DC LOW level output voltage                       | I <sub>O</sub> = 200 $\mu$ A                            | –    | 0.27            | –    | V        |
| V <sub>DCH</sub>                     | limited DC HIGH level output voltage                      | I <sub>I</sub> = 200 $\mu$ A                            | –    | 1.8             | –    | V        |
| V <sub>DC</sub>                      | DC level output voltage                                   |   | tbf  | 0.86            | tbf  | V        |
| <b>Y+SYNC output (pin 25)</b>        |   |   |      |                 |      |          |
| R <sub>O</sub>                       | output resistance   |   | –    | –               | 40   | $\Omega$ |
| I <sub>sink(max)</sub>               | maximum sink current                                      |   | 200  | –               | –    | $\mu$ A  |
| I <sub>source(max)</sub>             | maximum source current                                    |   | 1    | –               | –    | mA       |
| V <sub>BL</sub>                      | black level output voltage                                |   | –    | 1.6             | –    | V        |
| V <sub>SYNC</sub>                    | sync voltage amplitude                                    |   | 570  | 600             | 630  | mV       |
| V <sub>Y</sub>                       | Y voltage amplitude                                       |   | 1330 | 1400            | 1470 | mV       |
| B                                    | bandwidth frequency response                              | R <sub>L</sub> = 10 k $\Omega$ ; C <sub>L</sub> = 10 pF | 10   | –               | –    | MHz      |
| t <sub>d</sub>                       | group delay time tolerance                                | R <sub>L</sub> = 10 k $\Omega$ ; C <sub>L</sub> = 10 pF | –    | –               | 20   | ns       |
| t <sub>d</sub>                       | sync delay time from pin 29 to pin 25                     |   | 220  | 290             | 360  | ns       |
| t <sub>d</sub>                       | Y delay time from pin 5 to pin 25                         |   | –    | 10              | –    | ns       |
| <b>Y+SYNC input (pin 23; note 2)</b> |   |   |      |                 |      |          |
| I <sub>bias</sub>                    | input bias current  |   | –    | –               | 1    | $\mu$ A  |
| V <sub>I(max)</sub>                  | maximum Y voltage amplitude                               |   | –    | –               | 1    | V        |
| <b>NOTCH output (pin 22)</b>         |   |   |      |                 |      |          |
| R <sub>O</sub>                       | output resistance   |   | 1750 | 2000            | 2250 | $\Omega$ |
| V <sub>DC</sub>                      | DC output voltage level                                   |   | –    | V <sub>23</sub> | –    | V        |
| I <sub>sink(max)</sub>               | maximum sink current                                      |   | 300  | –               | –    | $\mu$ A  |
| <b>CHROMA output (pin 18)</b>        |   |   |      |                 |      |          |
| I <sub>sink(max)</sub>               | maximum sink current                                      |   | 200  | –               | –    | $\mu$ A  |
| I <sub>source(max)</sub>             | maximum source current                                    |   | 1    | –               | –    | mA       |
| V <sub>DC</sub>                      | DC voltage level  |   | –    | 2.5             | –    | V        |
| $\Delta$ V <sub>DC</sub>             | variation of DC voltage level                             | chrominance signal blanked                              | –    | 5               | –    | mV       |
|                                      |   | chrominance signal not blanked                          | –    | 5               | –    | mV       |
| R <sub>O</sub>                       | output resistance   |   | –    | 120             | –    | $\Omega$ |
| V <sub>O(p-p)</sub>                  | chrominance output voltage amplitude (peak-to-peak value) | f = 4.25 MHz  | –    | 165             | –    | mV       |
|                                      |   | f = 4.406 MHz   | –    | 205             | –    | mV       |



## SECAM encoder

## TDA8505

| SYMBOL  | PARAMETER  | CONDITIONS     | MIN. | TYP. | MAX. | UNIT     |
|---|--|----------------|------|------|------|----------|
| FREQUENCY OF CHROMINANCE SIGNAL (NOTE 3)                      |  |                |      |      |      |          |
| $f_{OR}$  | black level of D'R                                 |                | –    | 4406 | –    | kHz      |
| $f_{OB}$  | black level of D'B                                 |                | –    | 4250 | –    | kHz      |
| $f_{max}$   | maximum frequency                                  |                | 4721 | 4756 | 4791 | kHz      |
| $f_{min}$   | minimum frequency                                  |                | 3865 | 3900 | 3935 | kHz      |
| $\Delta D'R$  | deviation of D'R                                   | EBU bar of 75% | 252  | 280  | 308  | kHz      |
| $\Delta D'B$  | deviation of D'B                                   | EBU bar of 75% | 207  | 230  | 253  | kHz      |
| <b>CVBS output (pin 21)</b>                                   |  |                |      |      |      |          |
| $I_{sink(max)}$   | maximum sink current                               |                | 250  | –    | –    | $\mu$ A  |
| $I_{source(max)}$   | maximum source current                             |                | 1    | –    | –    | mA       |
| $V_{black}$   | black level voltage                                |                | –    | 1.6  | –    | V        |
| $G_Y$   | gain Y+SYNC (pin 23 to pin 21)                     |                | –    | 6    | –    | dB       |
| $G_{CHR}$   | gain CHROMA (pin 18 to pin 21)                     |                | –    | 6    | –    | dB       |
| $R_O$   | output resistance                                  |                | –    | 120  | –    | $\Omega$ |
| <b>LPFDR output (pin 13)</b>                                  |  |                |      |      |      |          |
| $V_O$   | DC control voltage level                           |                | tbf  | 2.4  | tbf  | V        |
|   | control sensitivity                                |                | –    | 0.2  | –    | kHz/mV   |
| $I_{LO}$  | output leakage current                             |                | –    | –    | 50   | nA       |
| <b>LPFDB output (pin 15)</b>                                  |  |                |      |      |      |          |
| $V_O$   | DC control voltage level                           |                | tbf  | 2.1  | tbf  | V        |
|   | control sensitivity                                |                | –    | 1.5  | –    | kHz/mV   |
| $I_{LO}$  | output leakage current                             |                | –    | –    | 50   | nA       |
| <b>LPF4.4 output (pin 24)</b>                                 |  |                |      |      |      |          |
| $V_O$   | DC control voltage level                           |                | tbf  | 2.3  | tbf  | V        |
|   | control sensitivity                                |                | –    | 1.5  | –    | kHz/mV   |
| $I_{LO}$  | output leakage current                             |                | –    | –    | 100  | nA       |
| <b>LPF4.25 output (pin 31; <math>C_{ext} = 270</math> pF)</b> |  |                |      |      |      |          |
| $V_O$   | DC control voltage level                           |                | tbf  | 2.3  | tbf  | V        |
|   | control sensitivity                                |                | –    | 5.3  | –    | kHz/mV   |
| $I_{LO}$  | output leakage current                             |                | –    | –    | 100  | nA       |
| <b>VCO4.25 (pin 27; note 4)</b>                               |  |                |      |      |      |          |
| <b>CS input (pin 29)</b>                                      |  |                |      |      |      |          |
| $V_{I(p-p)}$  | sync pulse input amplitude<br>(peak-to-peak value) |                | 75   | 300  | 600  | mV       |
|   | slicing level                                      |                | –    | 50   | –    | %        |
| $I_I$   | input current                                      |                | –    | 4    | –    | $\mu$ A  |
| $I_{O(max)}$  | maximum output current                             | during sync    | –    | 100  | –    | $\mu$ A  |

SECAM encoder

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| SYMBOL   | PARAMETER               | CONDITIONS              | MIN.                   | TYP. | MAX. | UNIT |
|--|-------------------------|-------------------------|------------------------|------|------|------|
| <b>V<sub>ext</sub> (pin 19)</b>                                  |                         |                         |                        |      |      |      |
| I <sub>ext</sub>   | external supply current |                         | –                      | –    | 1.5  | mA   |
| <b>SAND output (pin 20; V<sub>ext</sub> = 13.2 V); see Fig.8</b> |                         |                         |                        |      |      |      |
| I <sub>sink(max)</sub>   | maximum sink current    |                         | 100                    | –    | –    | μA   |
| I <sub>source(max)</sub>   | maximum source current  |                         | 100                    | –    | –    | μA   |
| V <sub>TL</sub>  | top voltage level       | V <sub>ext</sub> < 10 V | V <sub>ext</sub> - 0.1 | –    | –    | V    |
|  |                         | V <sub>ext</sub> > 10 V | 10                     | –    | –    | V    |

Notes

1. The threshold level of pin 2 is 700 ± 20 mV. The specification of the HIGH and LOW levels is in accordance with the scart fast blanking.
2. The black level of input signal must be 2 V; amplitude 1 V (peak-to-peak value) nominal (Y = 700 mV, SYNC = 300 mV).
3. The tolerances of f<sub>OR</sub> and f<sub>OB</sub> are with the printed-circuit board <±5 kHz. This value can be influenced by the print layout.
4. The oscillator operates in series-resonance. The resonance resistance of the crystal must be <60 Ω and parallel capacitance of the crystal <10 pF.

INTERNAL CIRCUITRY

| PIN | NAME   | CIRCUIT | DESCRIPTION  |
|-----|--------|---------|--|
| 1   | -(R-Y) |         | -(R-Y) input; connected via 47 nF capacitor; 1.05 V (peak-to-peak value) for EBU bar of 75%; see also pins 3, 5, 7, 9 and 11 |

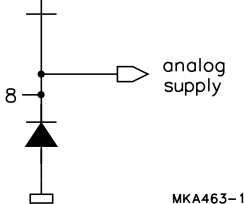
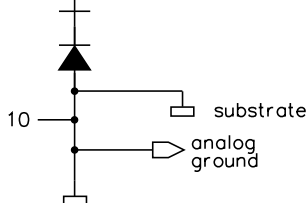
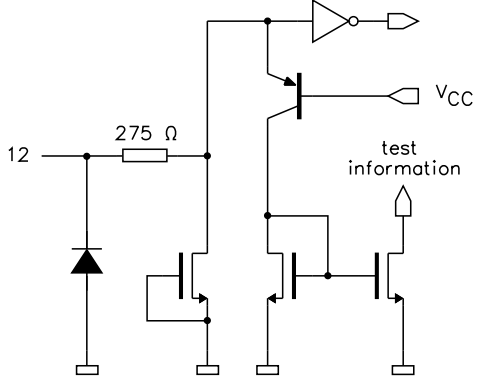
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| PIN | NAME   | CIRCUIT   | DESCRIPTION   |
|-----|--------|-----------|---|
| 2   | MCONTR |           | multiplexer control input:<br><0.4 V Y, U and V<br>>1 V R, G and B                          |
| 3   | -(B-Y) | see pin 1 | -(B-Y) input; connected via 47 nF capacitor; 1.33 V (peak-to-peak value) for EBU bar of 75% |
| 4   | FH/2   |           | FH/2 input; forcing possibility; when not used this pin is connected to ground              |
| 5   | Y      | see pin 1 | Y input; connected via 47 nF capacitor; 1 V (peak-to-peak value) for EBU bar of 75%         |
| 6   | TEST   |           | test pin; connected to V <sub>CC</sub> or left open-circuit                                 |

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| PIN | NAME             | CIRCUIT   | DESCRIPTION   |
|-----|------------------|---|---|
| 7   | R                | see pin 1   | RED input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75%   |
| 8   | V <sub>DDA</sub> |    | analog supply voltage for encoder part; 5 V nominal                                       |
| 9   | G                | see pin 1   | GREEN input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75% |
| 10  | V <sub>SSA</sub> |   | analog ground   |
| 11  | B                | see pin 1   | BLUE input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75%  |
| 12  | Y/Y+SYNC         |  | control pin:<br>0 V Y without sync supplied to pin 5<br>5 V Y with sync supplied to pin 5 |

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| PIN | NAME  | CIRCUIT    | DESCRIPTION   |
|-----|-------|------------|---|
| 13  | LPFDR |            | modulator control loop filter with low leakage capacitors   |
| 14  | FADJ  |            | adjustment pin for 4.286 MHz:<br>potentiometer in series with two resistors between ground and pin 17 |
| 15  | LPFDB | see pin 13 | modulator control loop filter with low leakage capacitors   |
| 16  | FLT   |            | filter control pin; 220 nF capacitor to ground  |

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| PIN | NAME      | CIRCUIT | DESCRIPTION  |
|-----|-----------|---------|--|
| 17  | $V_{ref}$ |         | 2.5 V reference voltage decoupling with 47 $\mu$ F and 22 nF capacitors  |
| 18  | CHROMA    |         | chrominance output   |
| 19  | $V_{ext}$ |         | pin for external power supply, for sandcastle pulse; $V_{ext} > 8$ V; if not used, the pin should be connected to ground |
| 20  | SAND      |         | sandcastle pulse   |

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| PIN | NAME      | CIRCUIT    | DESCRIPTION   |
|-----|-----------|------------|---|
| 21  | CVBS      |            | composite SECAM output  |
| 22  | NOTCH     |            | pin for external notch filter   |
| 23  | Y+SYNC IN |            | input of the delayed Y+SYNC signal of the delay line; black level must be 2 V |
| 24  | LPF4.4    | see pin 13 | loop filter for 4.40625 MHz reference oscillator                              |

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| PIN | NAME            | CIRCUIT | DESCRIPTION   |
|-----|-----------------|---------|---|
| 25  | Y+SYNC OUT      |         | <p>output of the delayed Y+SYNC signal, connected to the delay line via a resistor</p>  |
| 26  | XTAL/PLL VIDENT |         | <p>control pin:<br/> <b>without</b> vertical identification:<br/>         0 V PLL tuning<br/>         5 V crystal tuning<br/> <b>with</b> vertical identification:<br/>         2.5 V PLL tuning</p>  |
| 27  | VCO4.25         |         | <p>tuning of 4.25 MHz oscillator:<br/> <b>PLL tuning:</b><br/>         C = 270 pF to ground<br/> <b>crystal tuning:</b><br/>         crystal in series with a capacitor to ground<br/> <b>external tuning:</b><br/>         signal via 1 nF capacitor in series with a resistor</p> |



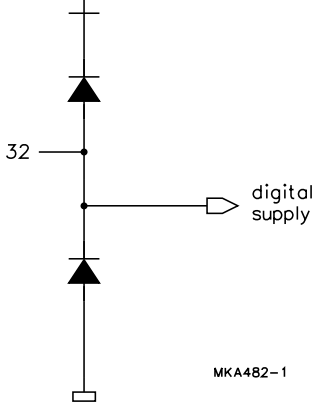
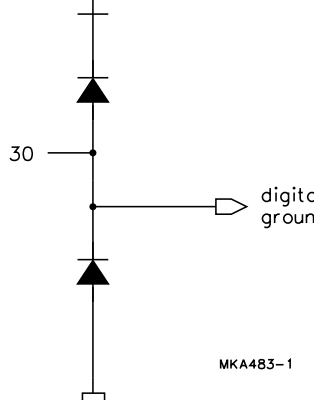
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| PIN | NAME   | CIRCUIT | DESCRIPTION  |
|-----|--------|---------|--|
| 28  | COLKIL |         | <p>colour killing input:<br/>                     0 V not active<br/>                     5 V active, internal D'R and D'B are blanked</p> |
| 29  | CS     |         | <p>composite sync signal input;<br/>                     amplitude &lt;600 mV<br/>                     (peak-to-peak value)</p>            |
| 30  | VSSD   |         | <p>digital ground</p>  |

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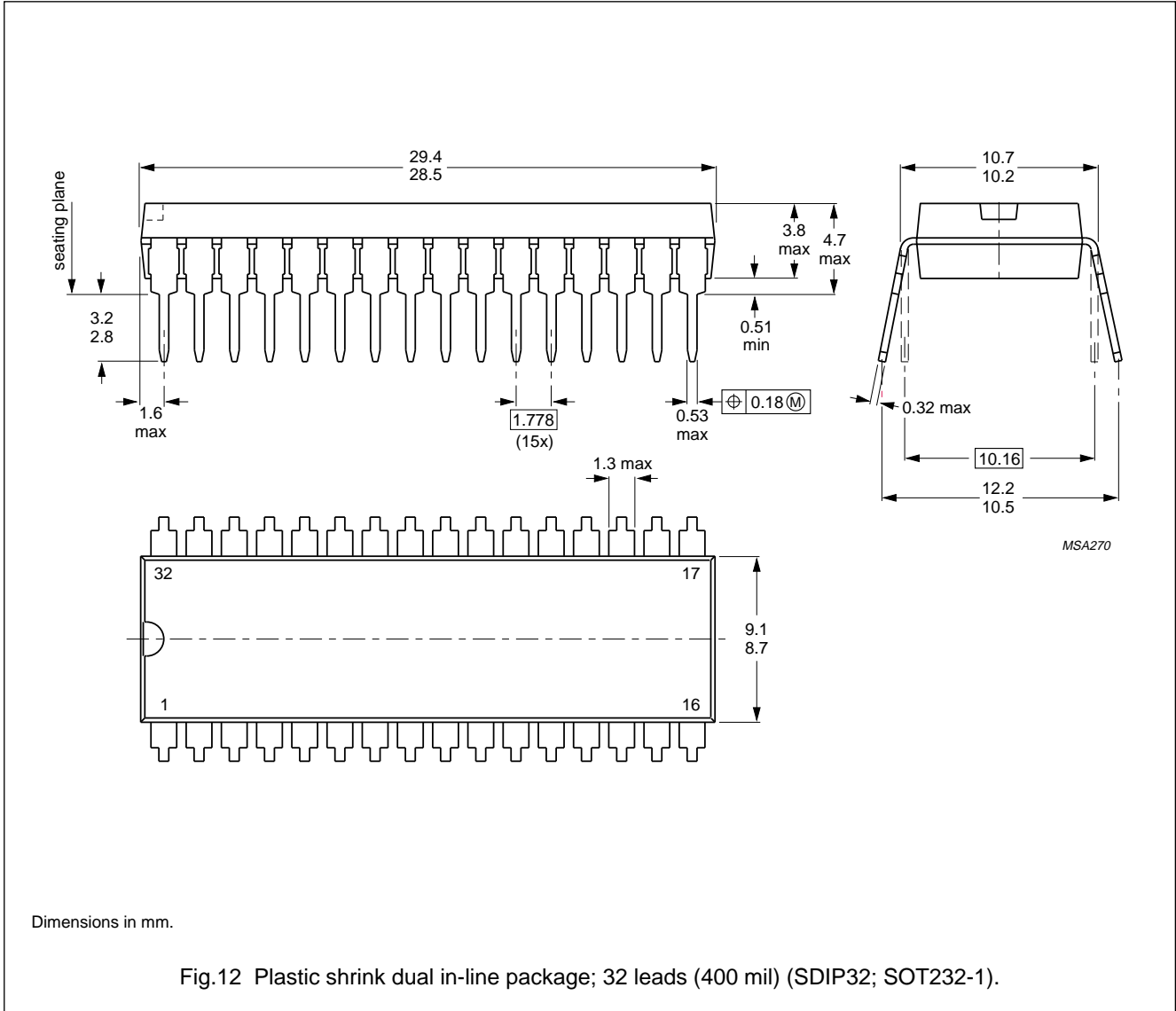
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| PIN | NAME             | CIRCUIT  | DESCRIPTION  |
|-----|------------------|--|--|
| 31  | LPF4.25          |   | loop filter for 4.25 MHz reference oscillator; connected to pin 17 if crystal or external tuning |
| 32  | V <sub>DDD</sub> |  | supply voltage digital part; 5 V nominal   |

SECAM encoder

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PACKAGE OUTLINE



## SECAM encoder

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**SOLDERING****Plastic dual in-line packages**

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the

specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**REPAIRING SOLDERED JOINTS**

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

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| <b>Data sheet status</b>  |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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**NOTES**

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**NOTES**

## Philips Semiconductors – a worldwide company

**Argentina:** IEROD, Av. Juramento 1992 - 14.b, (1428)  
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