DATA SHEET

TDA8050
QPSK transmitter

Product specification
Supersedes data of 1999 Jun 21
File under Integrated Circuits, IC02

1999 Dec 14

Philips
Semiconductors

PHILIPS

QPSK transmitter TDA8050

FEATURES

- Programmable gain
- PLL controlled carrier frequency
- 3-wire transmission bus
- 5 V supply voltage.

APPLICATIONS

- QPSK modulation.

GENERAL DESCRIPTION

The Quadrature Phase Shift Keying (QPSK) transmitter is a monolithic bipolar IC dedicated for quadrature modulation of the I and Q signals. It includes:

- Two double-balanced mixers
- Symmetrical Voltage Controlled Oscillator (VCO) with 0 to 90 degree signal generation for modulation
- Phase-Locked Loop (PLL) for IF frequency control
- Conversion mixer
- PLL for RF frequency control
- Gain controlled output amplifier
- 3-wire bus and an output buffer.

Two PLLs are incorporated, the first PLL includes:

- Fixed main divider
- Crystal oscillator and its programmable reference divider
- Phase/frequency detector combined with a fixed charge pump.

The second PLL includes:

- Divide-by-four preamplifier
- 12-bit programmable divider
- Crystal oscillator and its programmable reference divider
- Phase/frequency detector combined with a ‘clever’ charge pump which drives the tuning amplifier, including 9 V output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5.00	5.25	V
f_c	output centre frequency	5	–	40	MHz
$V_{o(max)}$	maximum output level	–	55	–	dBmV
f_{xtal}	crystal frequency	1	–	4	MHz
$f_{ref(MOD)}$	reference frequency for modulator synthesizer	–	250	–	kHz
f_{step}	frequency step size for convertor synthesizer	50	–	500	kHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8050T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

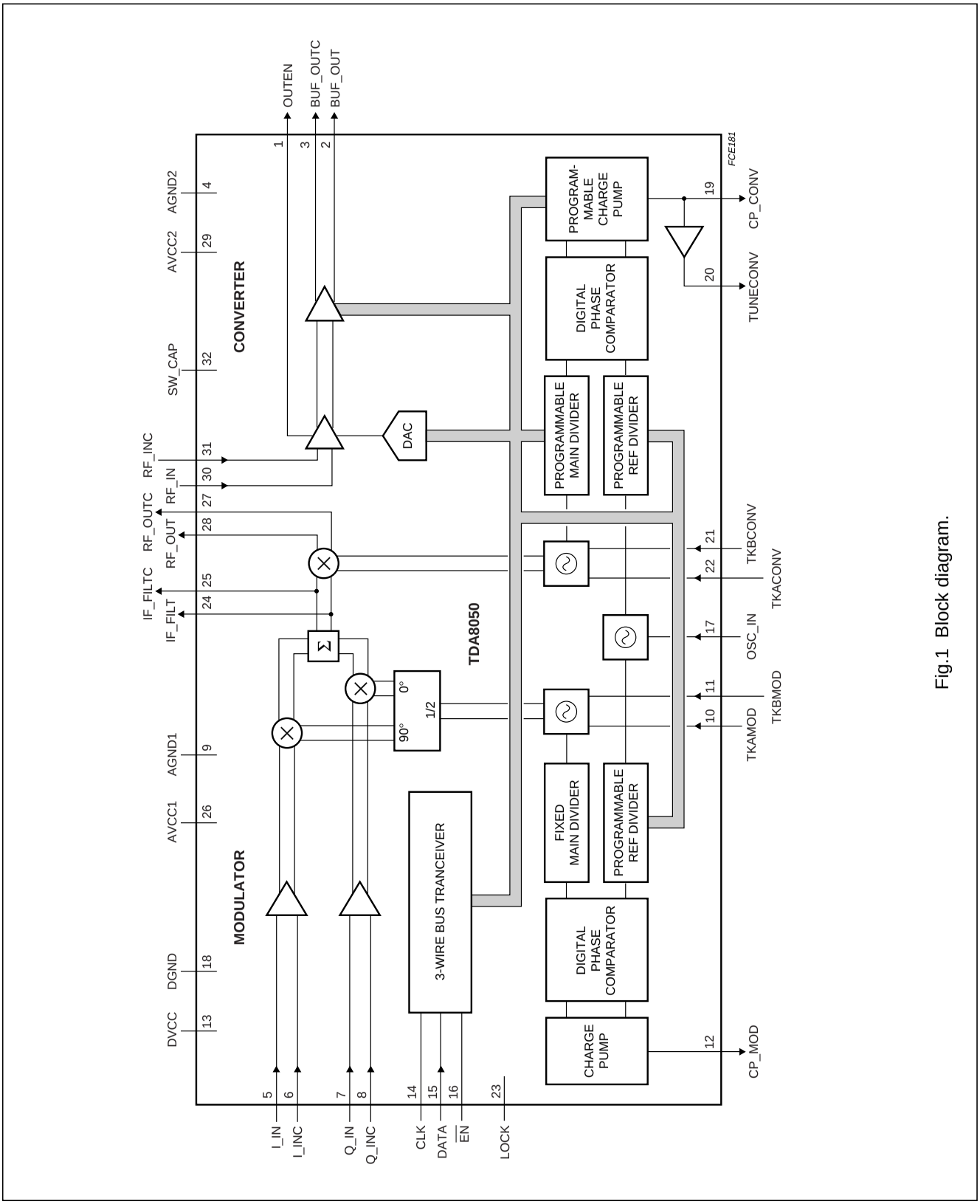


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTEN	1	output enable
BUF_OUT	2	output amplifier balanced output
BUF_OUTC	3	output amplifier balanced output
AGND2	4	converter analog ground 2
I_IN	5	I balanced input
I_INC	6	I balanced input
Q_IN	7	Q balanced input
Q_INC	8	Q balanced input
AGND1	9	modulator analog ground 1
TKAMOD	10	modulator VCO tank circuit input 2
TKBMOD	11	modulator VCO tank circuit input 1
CP_MOD	12	modulator charge pump output for PLL loop filter
DVCC	13	digital supply voltage
CLK	14	3-wire bus serial control clock
DATA	15	3-wire bus serial control data input
$\overline{EN}$	16	3-wire bus serial control enable
OSC_IN	17	crystal oscillator input
DGND	18	digital ground
CP_CONV	19	converter charge pump output for PLL loop filter
TUNECONV	20	tuning voltage output for converter VCO
TKBCONV	21	converter VCO tank circuit input 1
TKACONV	22	converter VCO tank circuit input 2
LOCK	23	lock detect signal
IF_FILT	24	IF balanced output to filter
IF_FILTC	25	IF balanced output to filter
AVCC1	26	modulator analog supply voltage
RF_OUTC	27	RF balanced output to filter
RF_OUT	28	RF balanced output to filter
AVCC2	29	converter analog supply voltage
RF_IN	30	RF balanced input to programmable amplifier
RF_INC	31	RF balanced input to programmable amplifier
SW_CAP	32	switch capacitor

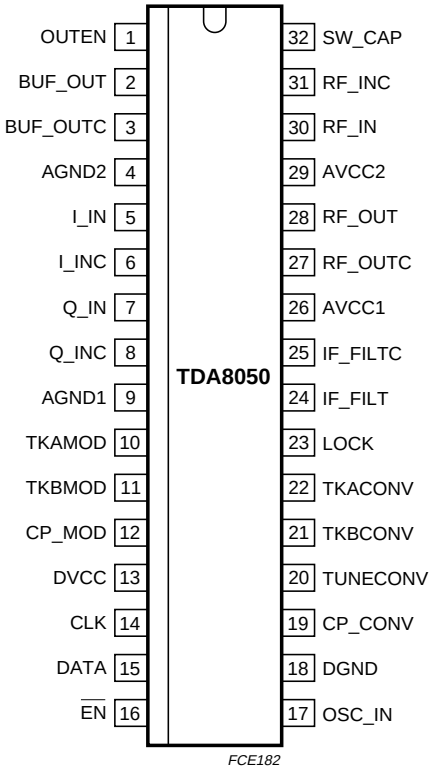


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The I and Q are balanced analog signals at a level of 400 mV (p-p). These are mixed by two double balanced mixers with the output signal generated by a first local oscillator providing the modulated signal.

The modulated signal is then filtered by an IF filter. This filtered signal together with a signal generated by a second local oscillator is converted by a balanced mixer to produce the QPSK signal.

The QPSK signal is amplified by a gain controlled amplifier to a level suitable for transmission. The gain of the controlled amplifier is bus controlled and this amplifier can be disabled when not transmitting to provide signal attenuation.

The amplified signal is applied to an on-chip amplifier having two balanced outputs (open collector) linked to two chip resistors (values 150 Ω), and 9 V. The balanced outputs are designed to drive a 2 : 1 transformer (Siemens V944) with a 75 Ω load giving an output level of 55 dBmV. The output frequency range of the transmitter is 5 to 40 MHz.

The frequency of the first local oscillator operates at twice the frequency (i.e. 280 MHz) fixed by a Phase-Locked Loop (PLL) implemented in the circuit.

The frequency of the second local oscillator operates in the bandwidth 145 to 180 MHz and programmable due to a PLL implemented in the circuit.

The VCO of both first and second local oscillators requires an external LC tank circuit with two varicap diodes.

The data to the PLL is loaded in bursts framed by the signal $\overline{EN}$. Programming rising clock edges and their appropriate data bits are ignored until $\overline{EN}$ goes active (LOW). The internal latches are updated with the latest programming data when $\overline{EN}$ returns inactive (HIGH). The last 14 bits are stored in the programming register.

No check is made on the number of clock pulses received during the time programming is enabled. **A wrong active clock edge will be generated causing a shift of data bits, if $\overline{EN}$ goes HIGH while CLK is still LOW.** At power up, $\overline{EN}$ should be HIGH. The lock detector output LOCK is HIGH when both PLLs are in lock.

The main divider ratio and the reference divider ratios are provided via the serial bus. A control register controls the Digital-to-Analog Converter (DAC), the output amplifier and the charge pump currents (Tables 1, 2 and 3).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
t_{sc}	short-circuit time (every pin to V_{CC} or GND)	–	10	s
V_{max}	voltage on all pins except BUF_OUT, BUF_OUTC and TUNECONV	–0.3	V_{CC}	V
$V_{o(tune)}$	output tuning voltage	–0.3	+30	V
$V_{o(buf)}$	output buffer voltage on pins BUF_OUT and BUF_OUTC	–	10	V
P_{tot}	maximum power dissipation	–	800	mW
T_{amb}	operating ambient temperature	0	70	°C
T_{stg}	storage temperature	–40	+150	°C
$T_{j(max)}$	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	63	K/W

HANDLING

Human Body Model (HBM): The IC pins withstand 2 kV except pins 27 and 28 (1750 V).

Machine Model (MM): The IC pins withstand 100 V.

CHARACTERISTICS

Measured in application circuit (see Fig.9) with the following conditions: V_{CC} = 5 V; T_{amb} = 25 °C; all AC units are RMS values; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{CCA(mod)}$	modulator analog supply voltage		4.75	5	5.25	V
$I_{CCA(mod)}$	modulator analog supply current		–	41	–	mA
$V_{CCA(conv)}$	converter analog supply voltage		4.75	5	5.25	V
$I_{CCA(conv)}$	converter analog supply current		–	48	–	mA
$I_{CC(buf)}$	buffer output supply current		–	44	–	mA
V_{CCD}	digital supply voltage		4.75	5	5.25	V
I_{CCD}	digital supply current		–	22	–	mA
$V_{CC(tune)}$	tuning supply voltage		–	–	9	V
Quadrature modulator I and Q inputs						
$V_{I(DC)}$	input DC level	over the complete range of temperature	–	$0.5V_{CC}$	–	V
$V_{i(p-p)}$	signal input level (balanced) (peak-to-peak value)	indicative	–	400	500	mV
$f_{i(max)}$	I and Q maximum input frequency	indicative	–	10	–	MHz
$Z_{i(dif)}$	differential input impedance		–	4.4	–	kΩ
$B_{(1dB)}$	1 dB amplifier bandwidth	indicative	–	10	–	MHz
MODULATOR						
f_c	output centre frequency		–	–	140	MHz
ΔA	amplitude imbalance	see Fig.3	–	–	±1	dB
$\Delta\Phi$	phase imbalance		–	–	±2	deg
$LO_{(sup)}$	LO suppression	see Fig.3	–	–28	–	dBc
$Z_{o(dif)}$	differential output impedance		–	1.8	–	kΩ
MODULATOR VOLTAGE CONTROLLED OSCILLATOR						
$f_{osc(mod)}$	oscillation frequency VCO		–	–	280	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Converter output						
V_o	output level	f_i = 30 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs	37.5	40	42.5	dBmV
ΔV_o	output flatness	f_i = 5 to 40 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs	–	–	2	dB
f_c	output centre frequency		5	–	40	MHz
$Z_{o(dif)}$	differential output impedance		–	150	–	Ω
IM3	3rd-order intermodulation distortion	see Fig.4	–	–	–35	dBc
H_2	2nd-order harmonic of 5 to 40 MHz signal	f_i = 10 to 80 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs	–	–	–45	dBc
H_3	3rd-order harmonic of 5 to 40 MHz signal	f_i = 15 to 120 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs	–	–	–45	dBc
S_o	mixer spurious outputs of 5 to 40 MHz signal	f_i = 5 to 40 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs	–	–	–50	dBc
Converter voltage controlled oscillator						
$f_{osc(min)}$	minimum oscillation frequency		–	–	145	MHz
$f_{osc(max)}$	maximum oscillation frequency		180	–	–	MHz
Programmable gain and output buffer; note 1						
$Z_{i(dif)}$	differential input impedance		–	5.6	–	kΩ
ΔG	output level step size		–	–	2	dB
ΔBuf_o	output level adjust range	V_i = 30 dBmV sine wave; 40 MHz at pin RF_IN and RF_INC; DAC = 0 to 31	32	–	–	dB
V_o	output level		–	55	–	dBmV
ΔV_o	output flatness	f_i = 5 to 40 MHz; V_i = 30 dBmV sine wave; DAC = 28	–	–	2	dB
$V_{O(ENL)}$	output controlled enable LOW	output buffer on	–	–	0.8	V
$V_{O(ENH)}$	output controlled enable HIGH	output buffer off	2.4	–	–	V
ISO	disable isolation	$V_{i(dif)}$ = 100 mV; V_o = 55 dBmV; DAC = 28; f_i = 40 MHz; OE = 0.5	–35	–	–	dBc
$G_{(max)}$	maximum gain	see Fig.5	–	22	–	dB
$V_{o(1dB)}$	1 dB compression point	see Fig.5	60	–	–	dBmV
H_2	2nd-order harmonic of 5 to 40 MHz signal	see Fig.6				
		f_i = 10 to 40 MHz	–	–	–45	dBc
		f_i= 54 to 120 MHz	–	–	–35	dBc

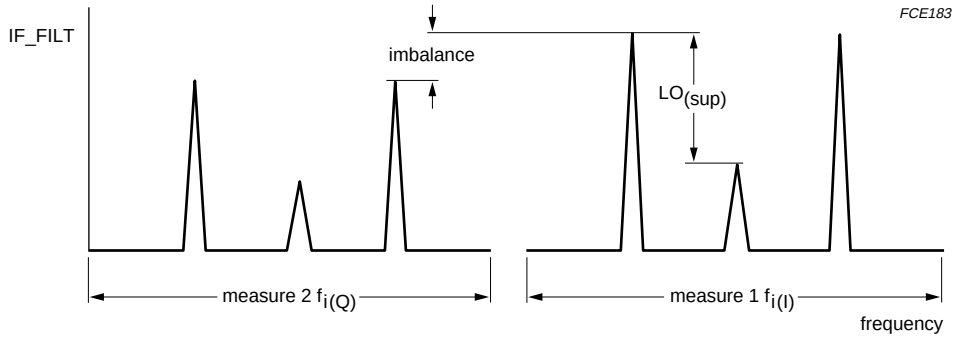
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H_3	3rd-order harmonic of 5 to 40 MHz signal	Fig.6				
		f_i = 15 to 40 MHz	–	–	–45	dBc
		f_i = 54 to 120 MHz	–	–	–35	dBc
Overall; note 1						
Φ_{osc}	phase noise	note 2;				
		at 10 kHz	–	–70	–	dBc/Hz
		at 100 kHz	–	–90	–	dBc/Hz
S_o	spurious signals of 5 to 40 MHz signal	f_i = 5 to 40 MHz; $V_{i(dif)}$ = 100 mV at I and Q inputs; V_o = 30 to 55 dBmV	–	–	–50	dBc
ISO_{tot}	total isolation at I/Q mid-range	see Fig.7	–	–	–65	dBc
C/N	carrier to noise ratio at final output at 2 MHz from carrier	$V_{i(dif)}$ = 100 mV V_o = 35 to 55 dBmV; f_i = 26.5 MHz	–	113	–	dBc/Hz
Crystal oscillator						
f_{xtal}	crystal frequency	note 3	1	–	4	MHz
Z_i	input impedance	f_{xtal} = 4 MHz	600	1200	–	Ω
$V_{I(DC)}$	DC input level		–	2.9	–	V
Modulator synthesizer						
$f_{ref(mod)}$	reference frequency		–	250	–	kHz
RDR1	reference divider ratio programmable		4	–	16	
ND1	fixed main divider ratio		–	1120	–	
I_{cp}	charge-pump current	fixed	–	0.30	–	mA
Converter synthesizer						
f_{step}	frequency step size		50	–	500	kHz
RD2	fixed reference divider ratio		–	2	–	
RDR2	reference divider ratio programmable	see Table 4	4	–	160	
ND2	fixed main divider ratio		–	4	–	
NDR2	programmable main divider ratio	see Table 4	290	–	3600	
Three wire bus						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.4	–	–	V
Lock detect pin						
$V_{o(lock)}$	output voltage (lock)		–	5	–	V
$V_{o(unlock)}$	output voltage (unlock)		–	0.02	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial control clock						
f_{clk}	clock frequency		–	330	–	kHz
t_{su}	input data to CLK set-up time	see Fig.3	–	2	–	µs
$t_{h(CLK)}$	input data to CLK hold time	see Fig.3	–	1	–	µs
$t_{d(strt)}$	delay to rising clock edge	see Fig.3	–	3	–	µs
$t_{d(stp)}$	delay from last clock edge	see Fig.3	–	3	–	µs

Notes

1. All specification points of the output section and the overall circuit are measured after the 2 : 1 transformer (siemens V944) connected with a load of 75 Ω.
2. Overall phase noise converter: I_{cp} = 0.36 mA; f_{ref} = 12.5 kHz; $V_{I(diff)}$ = 100 mV; $V_{O(diff)}$ = 100 mV; V_O = 55 dBmV; DAC = 28; f_i = 26.5 MHz.
3. Crystal oscillator; the crystal oscillator uses a 4, 2 or 1 MHz crystal in series with a capacitor. The crystal is serial resonant with load a capacitance of 18 to 20 pF. The connection to V_{CC} is preferred but can also be to GND.

Notes to the characteristics

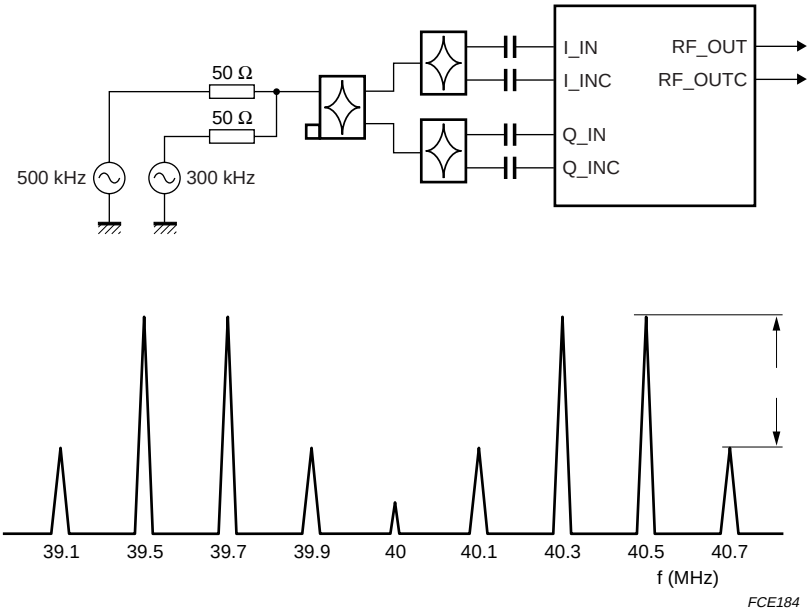


The amplitude imbalance and the LO suppression are measured in the spectrum of the signal measured at the output IF_FILT and are defined in the following conditions:

Measure 1: I input frequency = 500 kHz. I input level = 400 mV (p-p) sine wave. Unused input as 0 V differential.

Measure 2: Q input frequency = 500 kHz. Q input level = 400 mV (p-p) sine wave. Unused input as 0 V differential.

Fig.3 Imbalance and LO suppression.



3rd-order intermodulation distortion;
Two tones of 260 mV (p-p) at each I and Q input:

$$V_{(av)} = \frac{400}{2} \times 10^{\frac{-4}{20}} = 128\ mV(RMS)$$

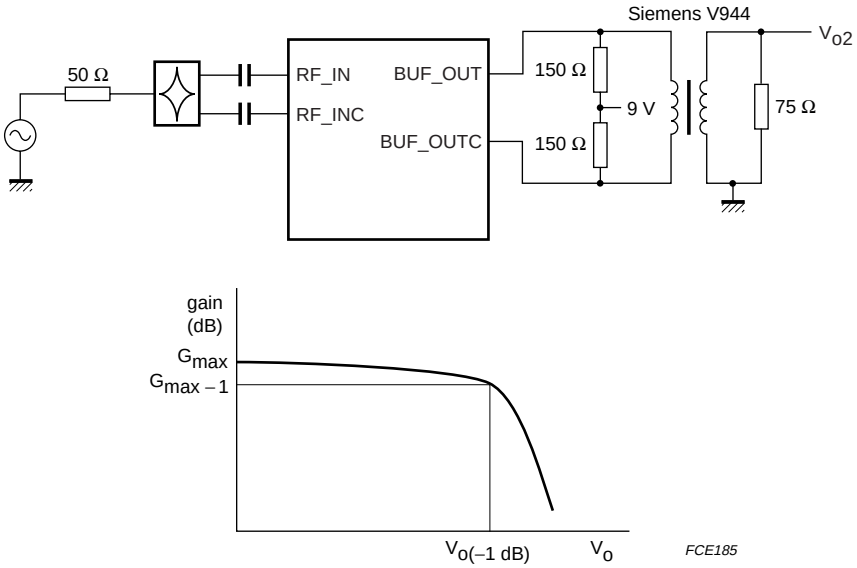
2 sine waves with a total RMS values of 128 mV give:

$$\sqrt{2 \times x^2} = 128$$

$x = \frac{128}{\sqrt{2}} =$ 90 mV (RMS) = 260 mV (p-p) and f_1 = 300 kHz,

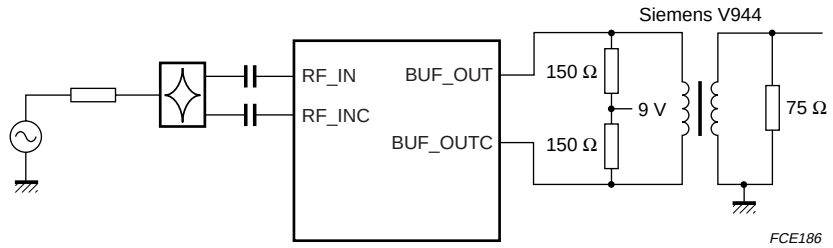
f_2 = 500 kHz and f_{RF} = 40 MHz.

Fig.4 3rd-order intermodulation distortion in I and Q channels (IM3).



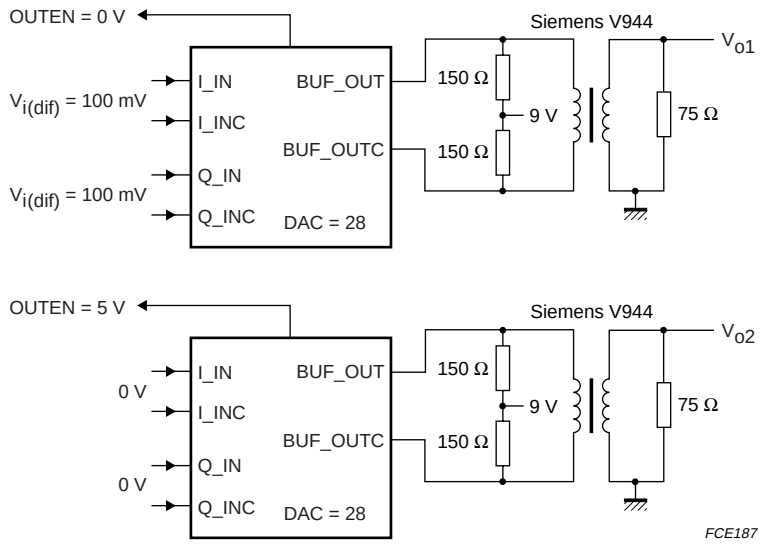
DAC = 31.
f = 26.5 MHz.
V_i is variable to have a variable output voltage.

Fig.5 Maximum gain and compression point.



DAC = 28.
f_i = 5 to 40 MHz.
V_i = 200 mV sine wave.
V_o = 55 dBmV (RMS value).

Fig.6 Harmonics of output section H2 and H3.



$ISO_{tot} = V_{o1}$ (dB) − V_{o2} (dB).

Fig.7 Isolation total.

APPLICATION INFORMATION

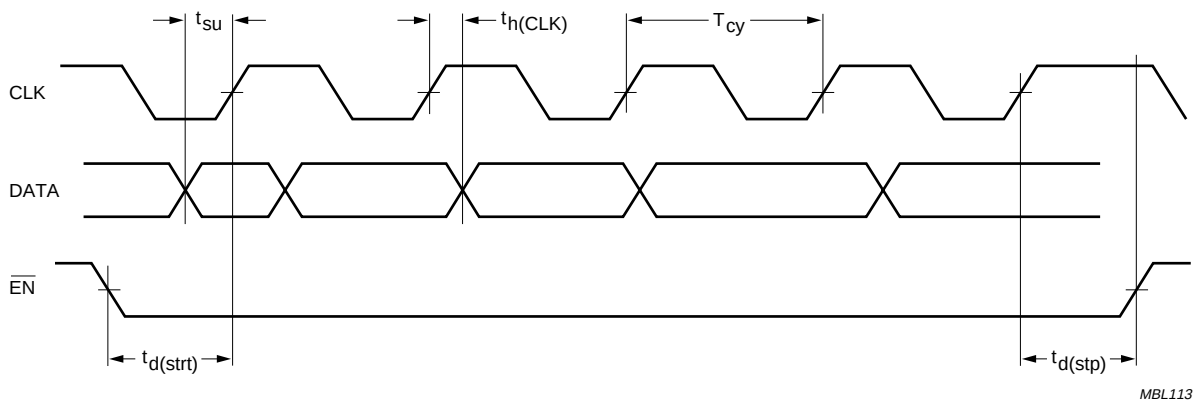


Fig.8 3-wire bus timing.

Table 1 Data format; note 1

DATA												ADDRESS	
D11 first in	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	AD1	AD0 last in
Modulator reference divider ratio				**Converter reference divider ratio**									
X	X	MP1(2)	MP0(2)	R7	R6	R5	R4	R3	R2	R1	R0	0	1
Control register													
X	X	X	OEN(3)	CR2(4)	CR1	CR0(4)	DAC4(5)	DAC3	DAC2	DAC1	DAC0	1	0
Main divider ratio													
P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	1	1

Notes

1. X = don't care.
2. MP1 and MP0: modulator reference divider ratio (see Table 2).
3. When OEN (output enable) is at logic 0, output is disabled, at logic 1 output is enabled.
4. CR2 to CR0: converter synthesizer charge pump current (see Table 3).
5. When DAC4 to DAC0 is at logic 0 minimum gain is programmed, at logic 1 maximum gain is programmed.

Table 2 Modulator reference divider ratio

MP1	MP0	PROGRAMMED RATIO
1	1	4
1	0	8
0	1	16

Table 3 Converter synthesizer charge pump current

CR2	CR1	CR0	LOCK_CONV(1)	I_{cp} (mA)
0	0	0	0	1.2
0	0	0	1	0.36
0	0	1	0	0.36
0	0	1	1	0.1
0	1	0	–	0.1
0	1	1	–	0.36
1	0	0	–	1.2

Note

1. LOCK_CONV is an internal signal.
   When at logic 0 converter PLL is out-of-lock. When at logic 1 converter PLL is in-lock.

Table 4 Converter synthesizer: $f_{comp} = f_{osc}/RD$

f_{osc}\f_{comp}	12.5 kHz	25 kHz	50 kHz	125 kHz
1 MHz	80	40	20	8
4 MHz	320	160	80	32

Table 5 Converter synthesizer; ND = 4; $f_{lo} = ND \times NDR \times f_{comp} = NDR \times step$

f_{lo}\step	50 kHz	100 kHz	200 kHz	500 kHz
145 MHz	2900	1450	725	290
180 MHz	3600	1800	900	360

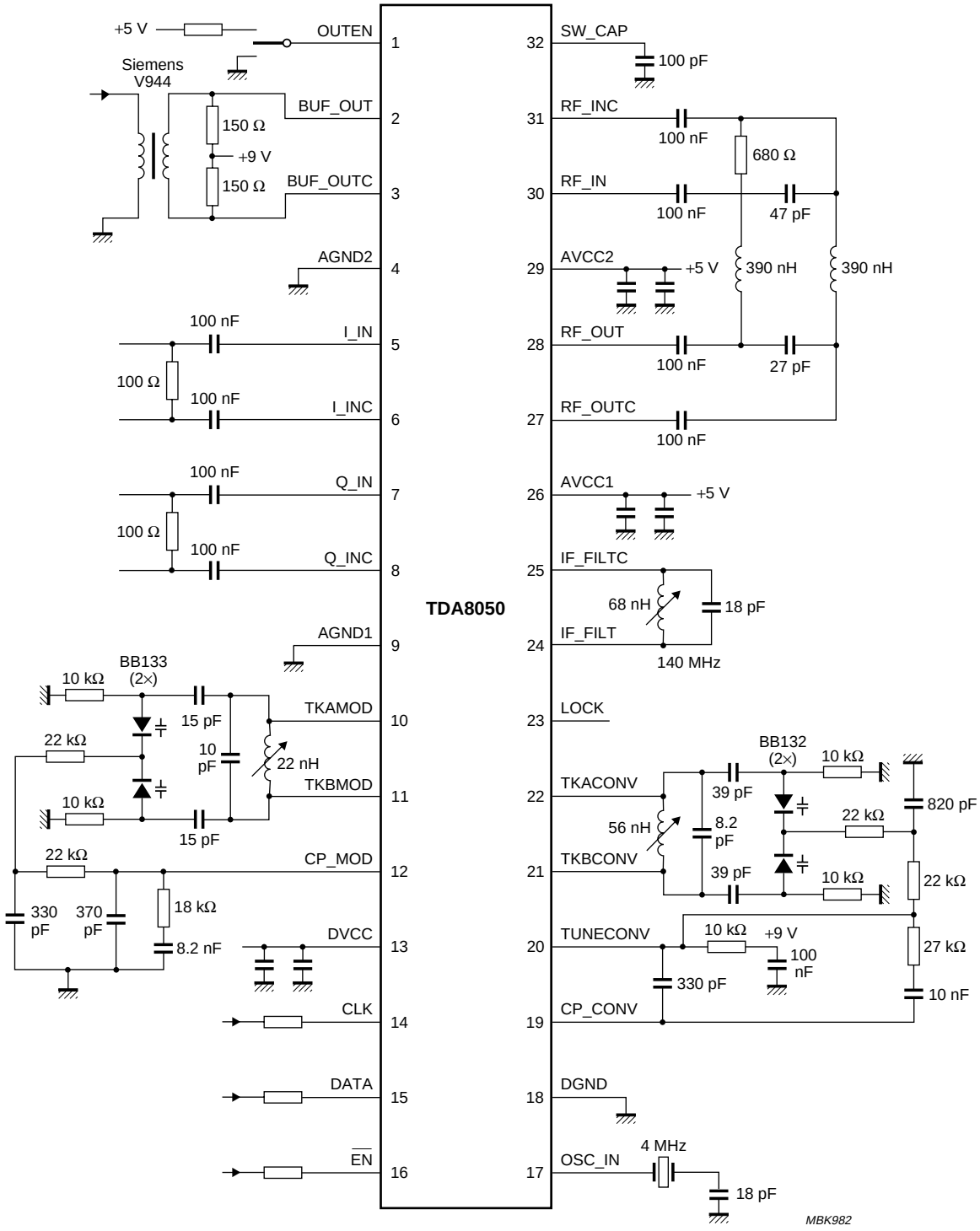
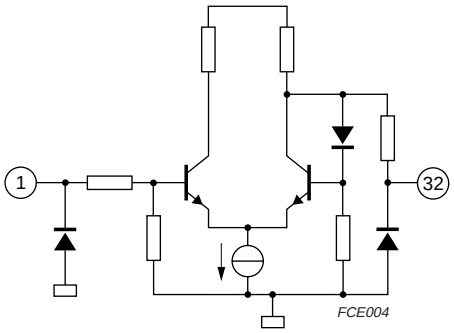
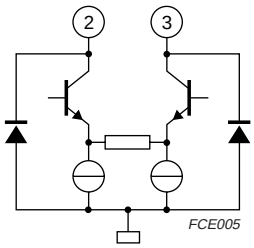
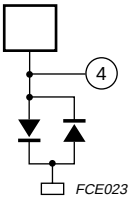
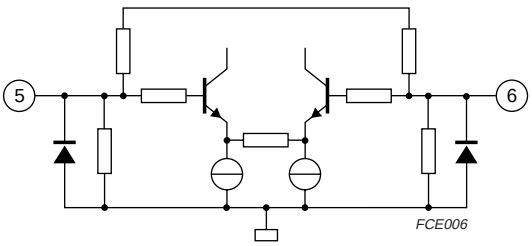
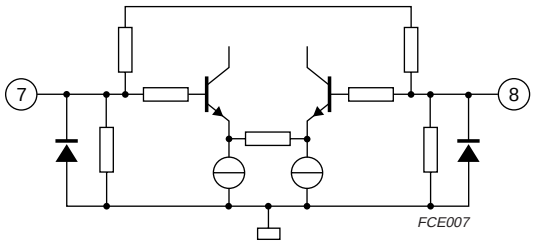
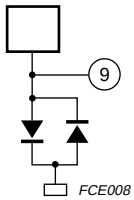
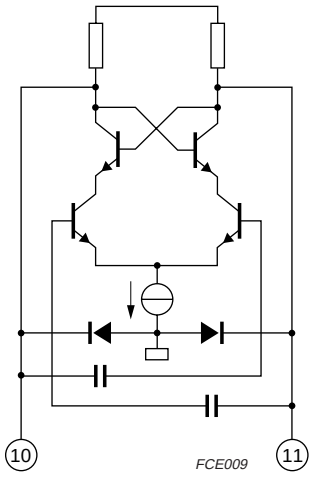
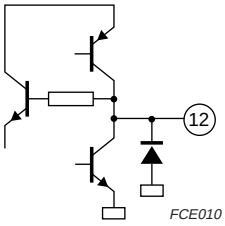
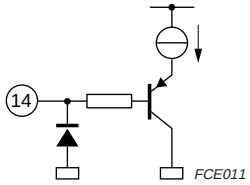
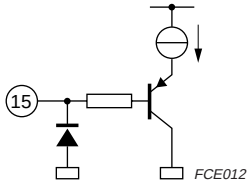
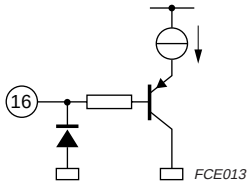
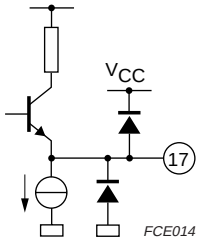
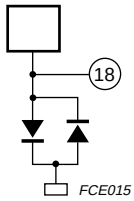


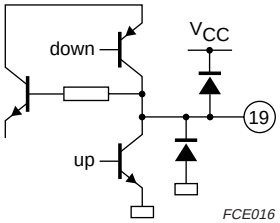
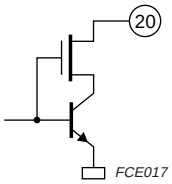
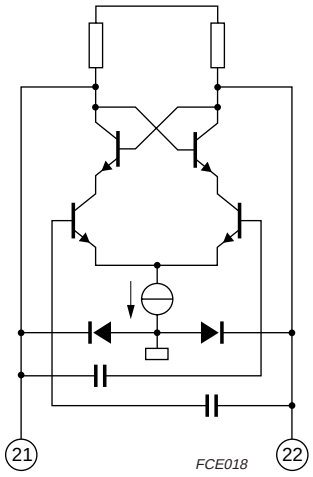
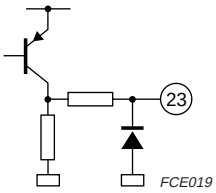
Fig.9 Application diagram.

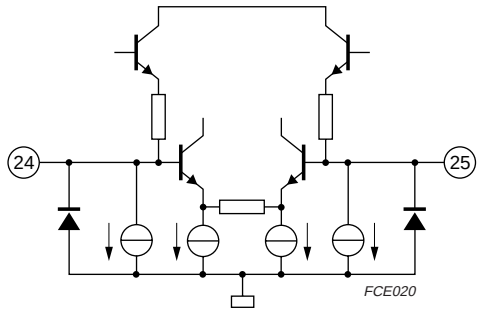
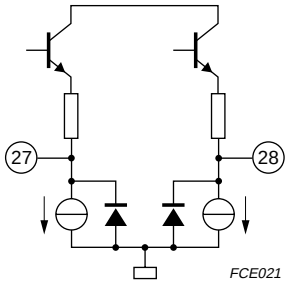
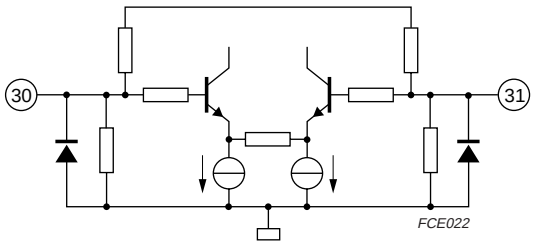
INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
OUTEN	1		–
SW_CAP	32		1.7 V
BUF_OUT	2		5.8 V
BUF_OUTC	3		5.8 V
AGND2	4		0
I_IN	5		2.5 V
I_INC	6		2.5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
Q_IN	7		2.5 V
Q_INC	8		2.5 V
AGND1	9		0 V
TKAMOD	10		3.1 V
TKBMOD	11		3.1 V
CP_MOD	12		2.1 V
DVCC	13	supply voltage	5 V

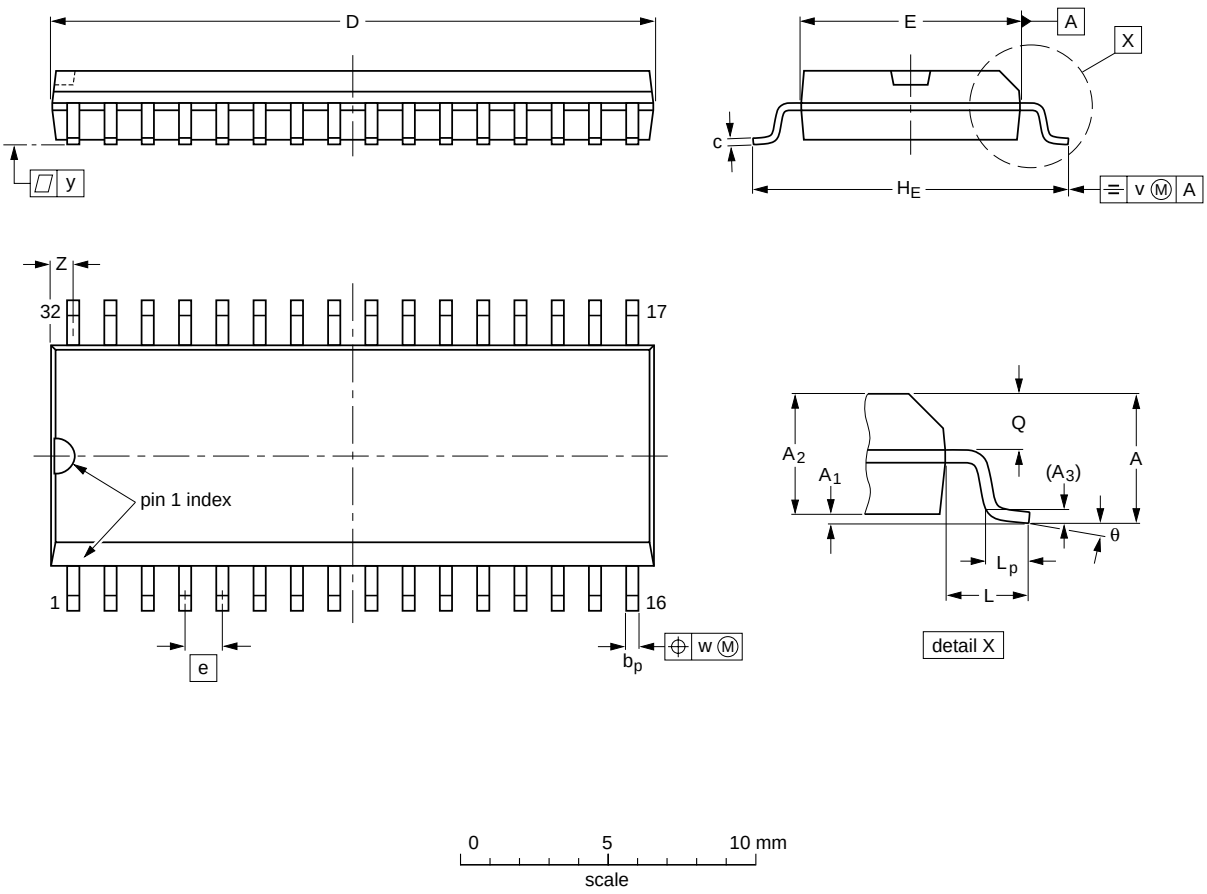
SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
CLK	14		–
DATA	15		–
$\overline{EN}$	16		–
OSC_IN	17		2.9 V
DGND	18		0

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
CP_CONV	19		2.1 V
TUNECONV	20		V_{VT}
TKBCONV	21		3.1 V
TKACONV	22		3.1 V
LOCK	23		0 V 5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
IF_FILT	24		2.1 V
IF_FILTC	25		2.1 V
AVCC1	26	supply voltage	5 V
RF_OUTC	27		3.7 V
RF_OUT	28		3.7 V
AVCC2	29	supply voltage	5 V
RF_IN	30		2.1 V
RF_INC	31		2.1 V

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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