DATA SHEET

SCN2681T

Dual asynchronous receiver/transmitter (DUART)

Product specification
Supersedes data of 1995 May 01
IC19 Data Handbook

1998 Sep 04

Philips
Semiconductors

PHILIPS

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCN2681T features a faster bus cycle time than the standard SCN2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCN2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCN2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

For a complete functional description and programming information for the SCN2681T, refer to the SCN2681 product specification.

FEATURES

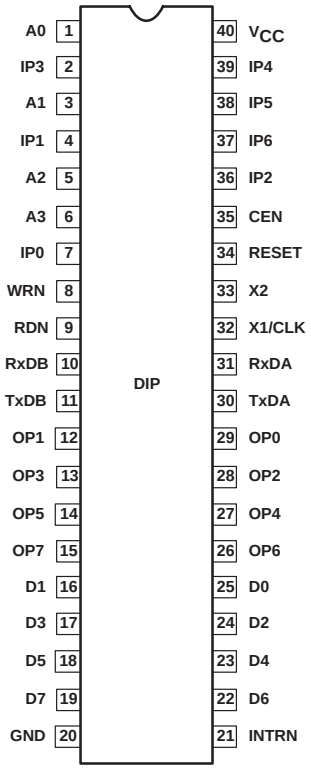
- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
  - Non-standard rates to 115.2
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X – 1MB/sec transmitter and receiver; 16X – 500kB/sec receiver and 250kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available

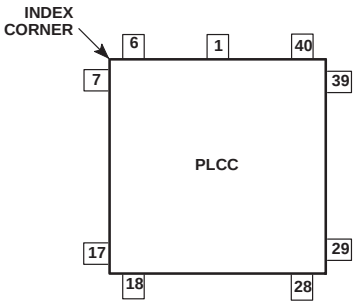
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	DWG #
40-Pin Plastic Dual In-Line Package (600mil-wide DIP)	SCN2681TC1N40	SOT129-1
44-Pin Plastic Lead Chip Carrier (PLCC)	SCN2681TC1A44	SOT187-2

NOTE: For a full register description and programming information see the SCN2681.

PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

SD00098

Figure 1. Pin Configurations

NOTE:
Refer to SCN2681 for functional description.

BLOCK DIAGRAM

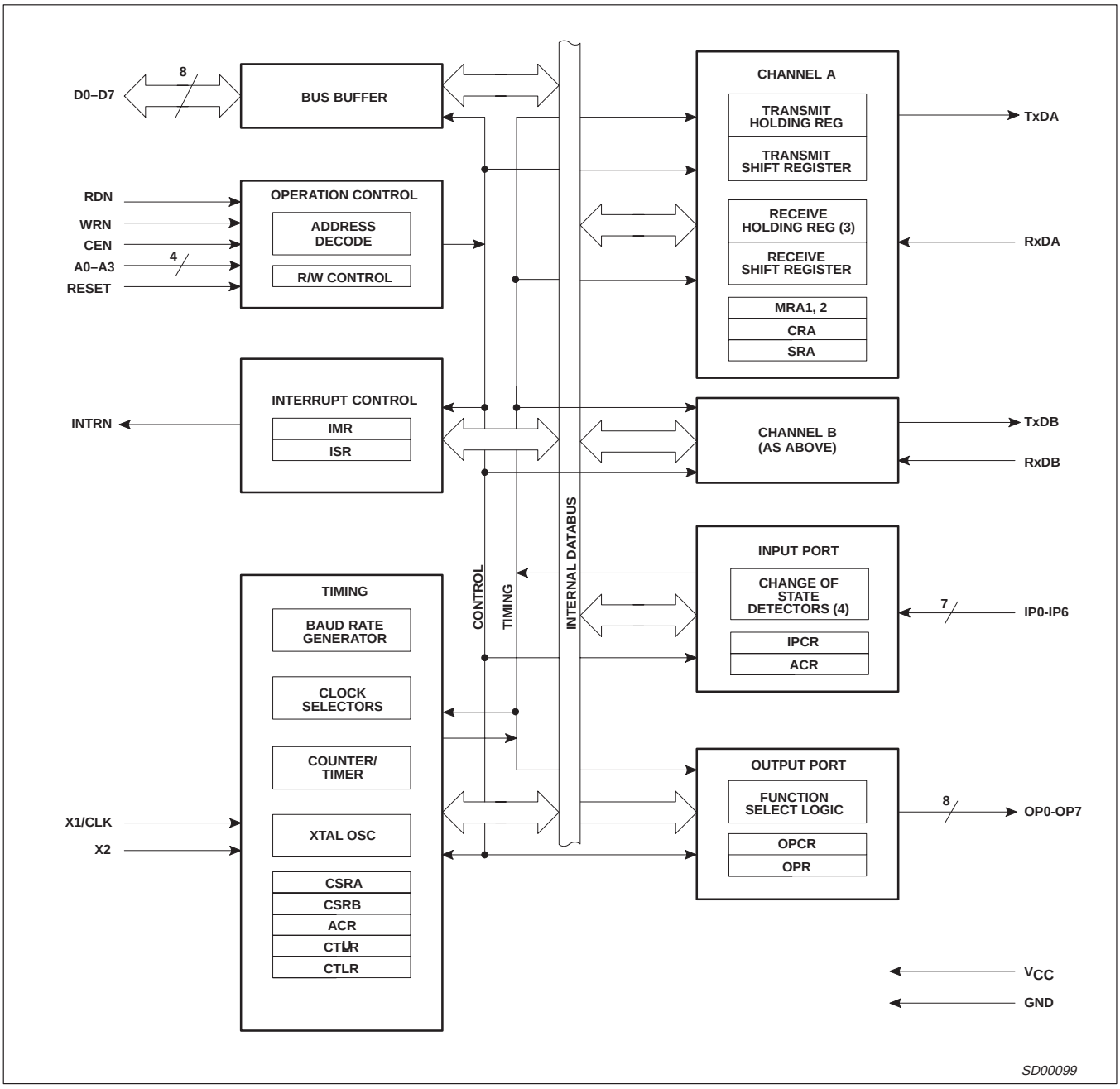


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
D0–D7	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is high, the DUART places the D0–D7 lines in the three-state condition.
WRN	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state. Clears Test modes, sets MR pointer to MR1.
INTRN	O	**Interrupt Request:** Active-low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7, Clock Timing.
X2	I	**Crystal 2:** Crystal connection. See Figure 7. If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. ‘Mark’ is high, ‘space’ is low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. ‘Mark’ is high, ‘space’ is low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the ‘mark’ condition when the transmitter is disabled, idle, or when operating in local loopback mode. ‘Mark’ is high, ‘space’ is low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the ‘mark’ condition when the transmitter is disabled, idle, or when operating in local loopback mode. ‘Mark’ is high, ‘space’ is low.
OP0	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output, or open-drain, active-low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output, or channel A open-drain, active-low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output, or channel B open-drain, active-low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output, or channel A open-drain, active-low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or channel B open-drain, active-low TxRDYB output.
IP0	I	**Input 0:** General purpose input, or channel A clear to send active-low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	I	**Input 1:** General purpose input, or channel B clear to send active-low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	I	**Input 2:** General purpose input, or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to GND[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			
V_{IH}	Input high voltage (X1/CLK)		3.5			
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.c. outputs)[4]	I_{OH} = -400µA	2.4			
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-state leakage current	V_O = 0.4 to V_{CC}	-10		10	
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 = grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{CC}	Power supply current[5]				150	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

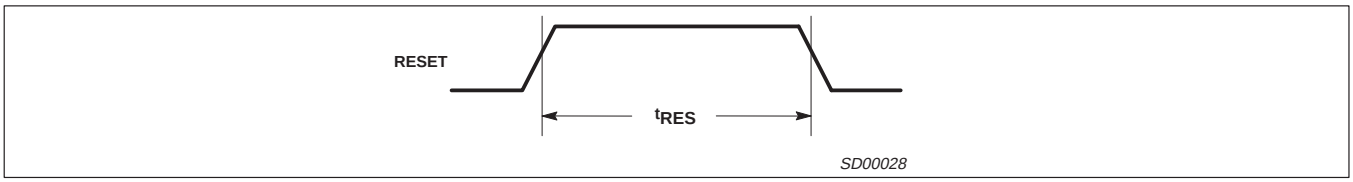


Figure 3. Reset Timing

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RES}	Reset pulse width	1.0		µs

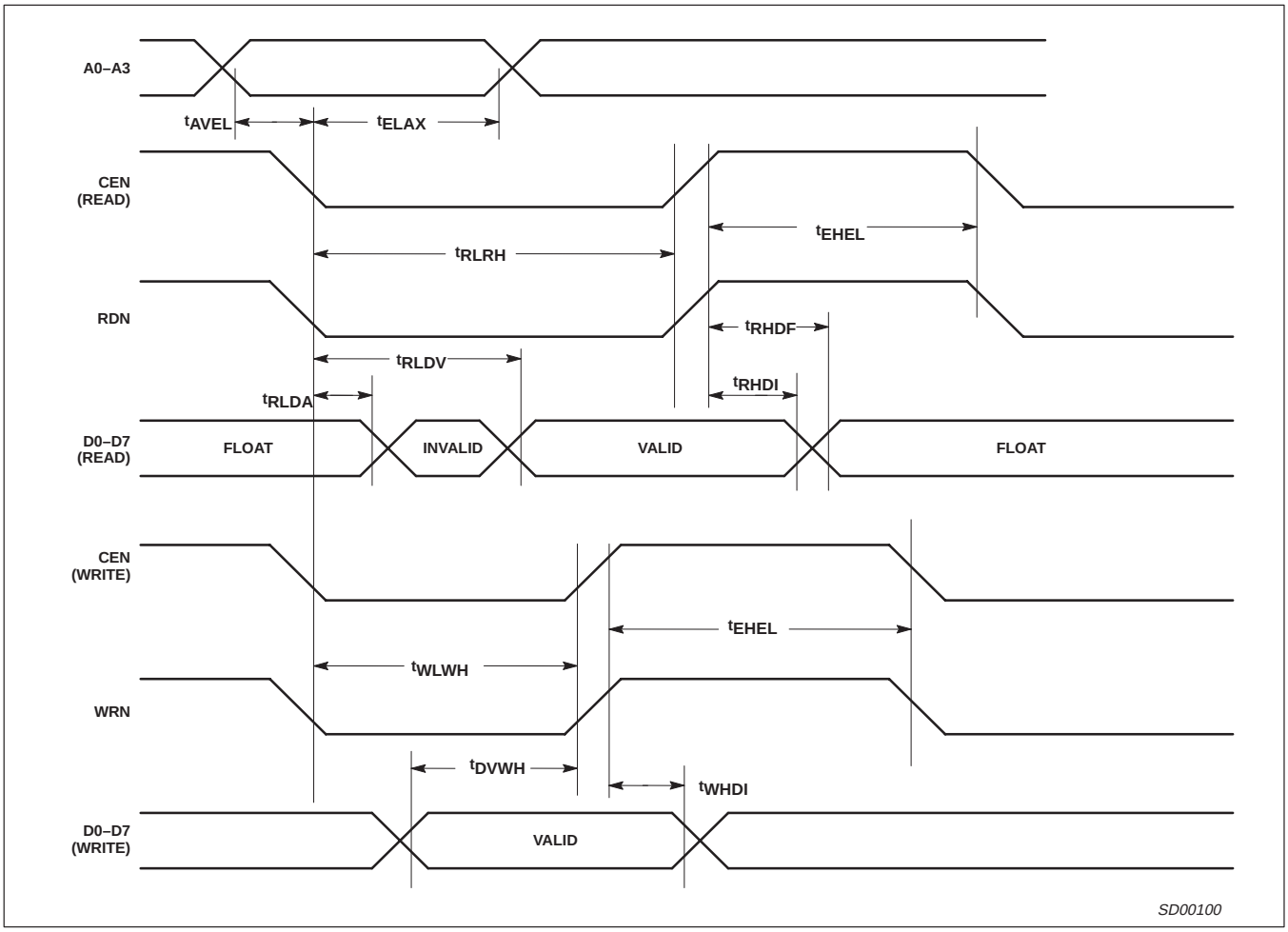


Figure 4. Bus Timing

SYMBOL	PARAMETER[1]	LIMITS		UNIT
		Min	Max	
t_{AVEL}	A0–A3 setup to RDN and CEN, or WRN and CEN low	0		ns
t_{ELAX}	RDN and CEN, or WRN and CEN low to A0–A3 invalid	100		ns
t_{RLRH}	RDN and CEN low to RDN or CEN high	120		ns
t_{EHEL}	CEN high to CEN low[2, 3]	110		ns
t_{RLDA}	CEN and RDN low to data outputs active	15		ns
t_{RLDV}	CEN and RDN low to data valid		100	ns
t_{RHDI}	CEN or RDN high to data invalid	10		ns
t_{RHDF}	CEN or RDN high to data outputs floating		65	ns
t_{WLWH}	WRN and CEN low to WRN or CEN high	75		ns
t_{DVWH}	Data input valid to WRN or CEN high	35		ns
t_{WHDI}	WRN or CEN high to data invalid	15		ns

NOTES:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
2. If CEN is used as the ‘strobing’ input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{EHEL} to guarantee that any status register changes are valid. As a consequence, this minimum time must be met for the RDN input even if the CEN is used as the strobing signal for bus operations.
3. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

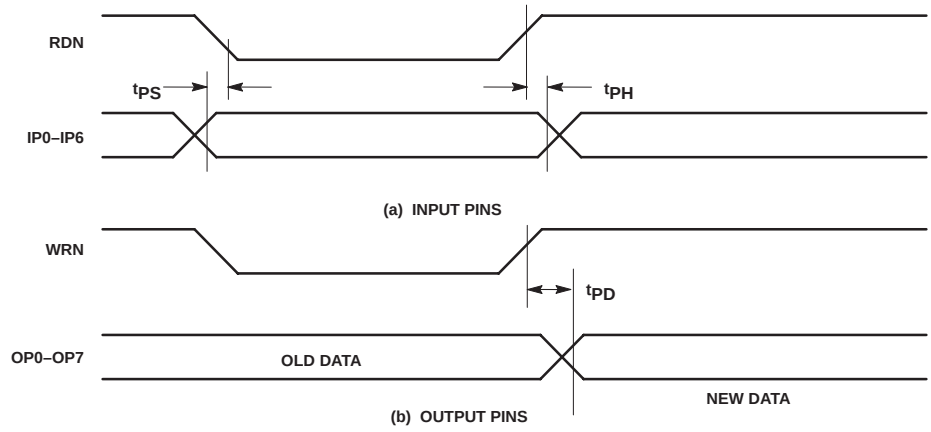
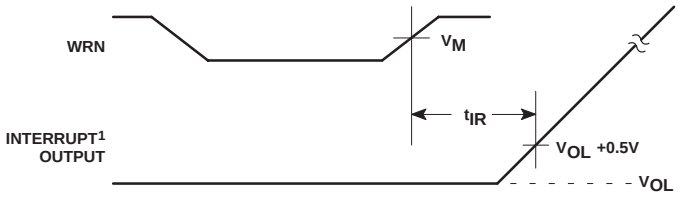


Figure 5. Port Timing

SYMBOL	PARAMETER[1]	LIMITS		UNIT
		Min	Max	
t_{PS}	Port input setup time before RDN low	0		ns
t_{PH}	Port input hold time after RDN high	0		ns
t_{PD}	Port output valid after WRN high		200	ns

NOTE:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

SD00102

Figure 6. Interrupt Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:			
	Read RHR (RxRDY/FFULL interrupt)		200	ns
	Write THR (TxRDY interrupt)		200	ns
	Reset command (delta break interrupt)		200	ns
	Stop C/T command (counter interrupt)		200	ns
	Read IPCR (input port change interrupt)		200	ns
	Write IMR (clear of interrupt mask bit)		200	ns

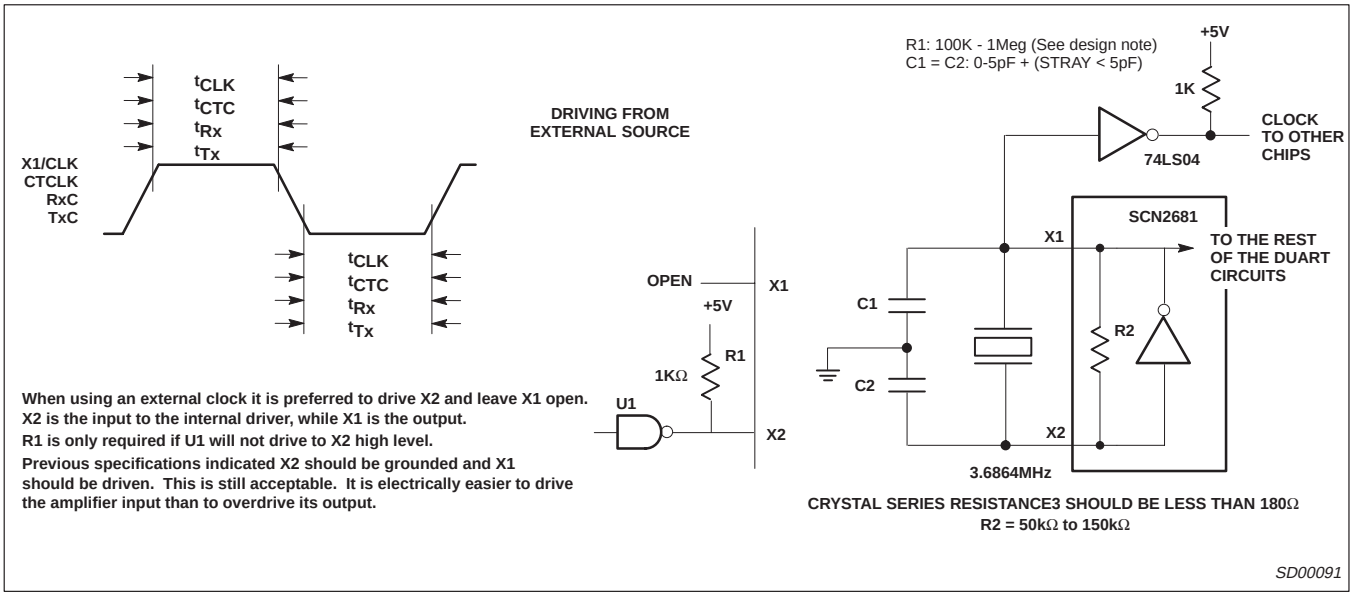


Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	X1/CLK high or low time	90			ns
t_{CLK}	X1/CLK frequency	2		4	MHz
f_{CLK}	CTCLK (IP2) high or low time	55			ns
t_{CTC}	CTCLK (IP2) frequency[1]	0		8	MHz
f_{CTC}	RxC high or low time	55			ns
t_{RX}	RxC frequency (16X)[1]	0	3.6864	8	MHz
f_{RX}	(1X)[1]	0		1	MHz
t_{TX}	TxC high or low time	110			ns
f_{TX}	TxC frequency (16X)[1]	0		4	MHz
	(1X)[1]	0		1	MHz

NOTE:
1. Minimum frequencies are not tested but are guaranteed by design.

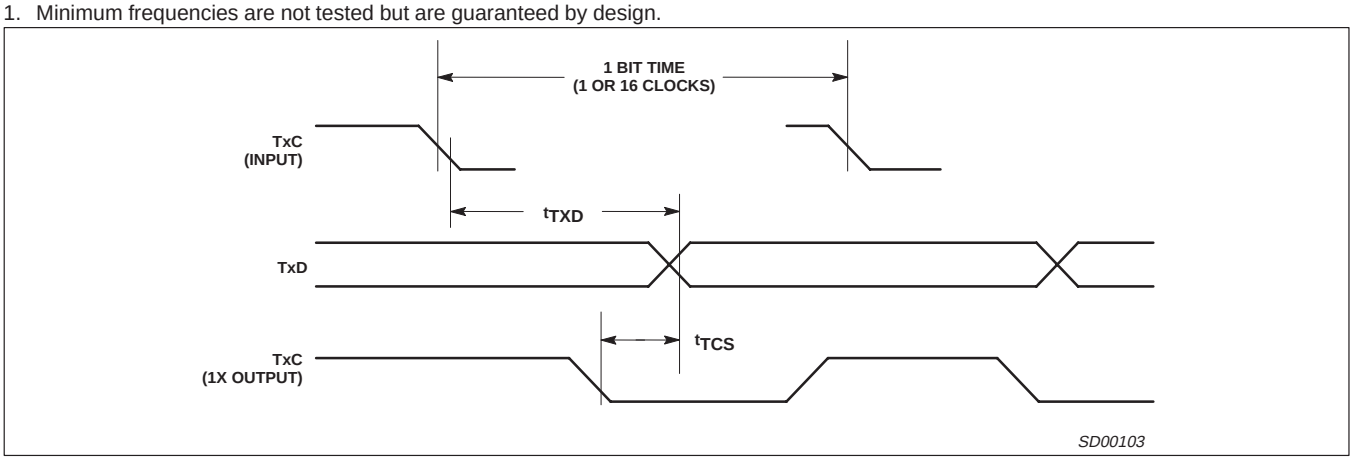


Figure 8. Transmit

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{TXD}	TxD output delay from TxC external clock input on IP pin		300	ns
t_{TCS}	Output delay from TxC low at OP pin to TxD data output	0	100	ns

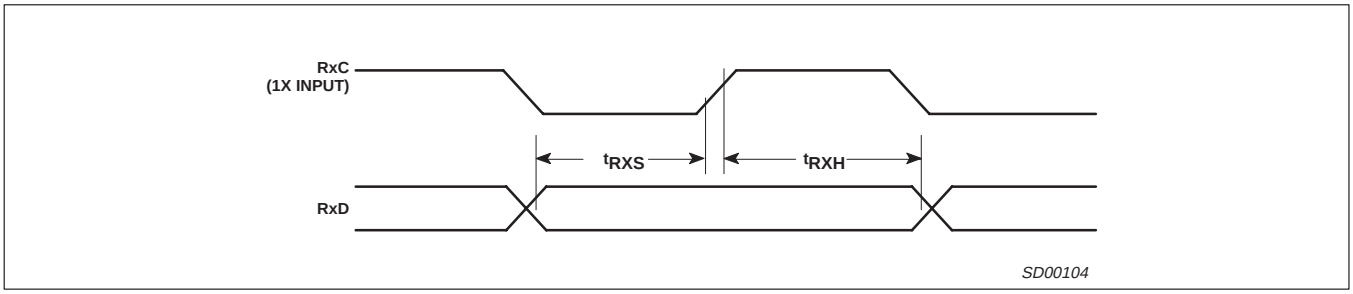


Figure 9. Receive

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXS}	RxD data setup time before RxC high at external clock input on IP pin	200		ns
t_{RXH}	RxD data hold time after RxC high at external clock input on IP pin	25		ns

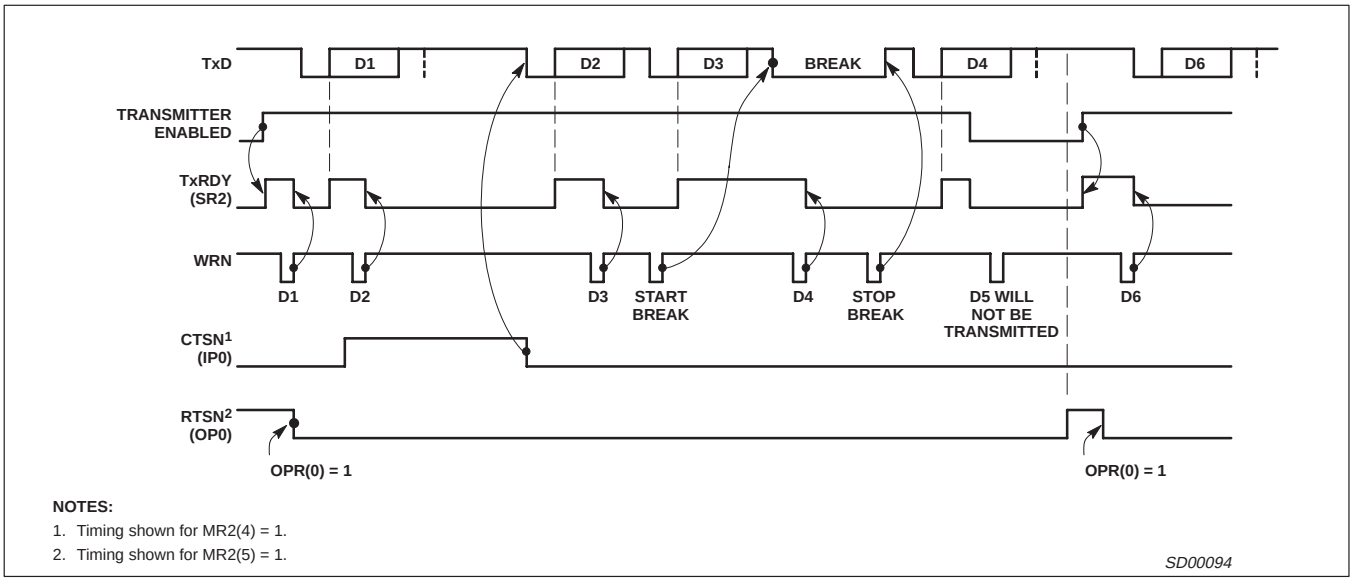


Figure 10. Transmitter Timing

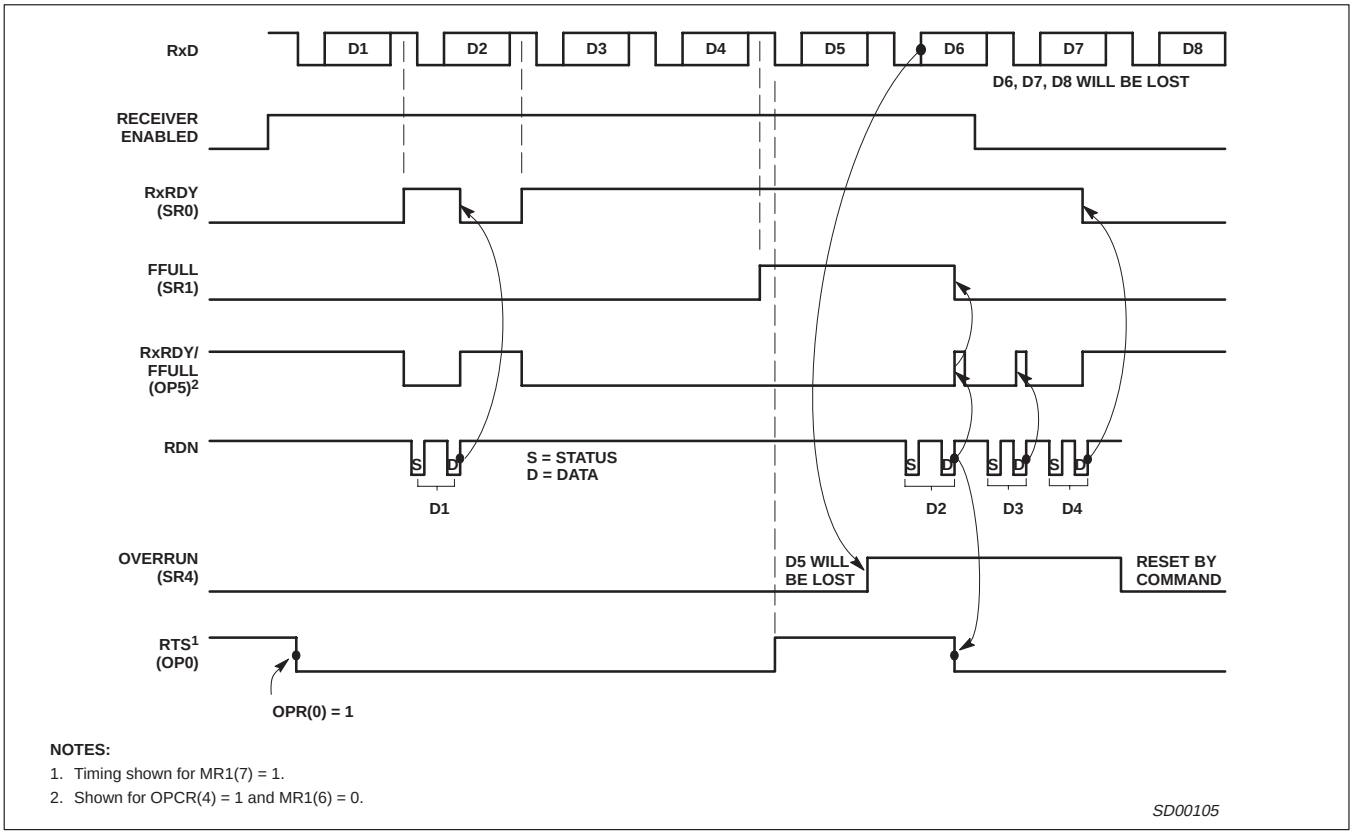


Figure 11. Receiver Timing

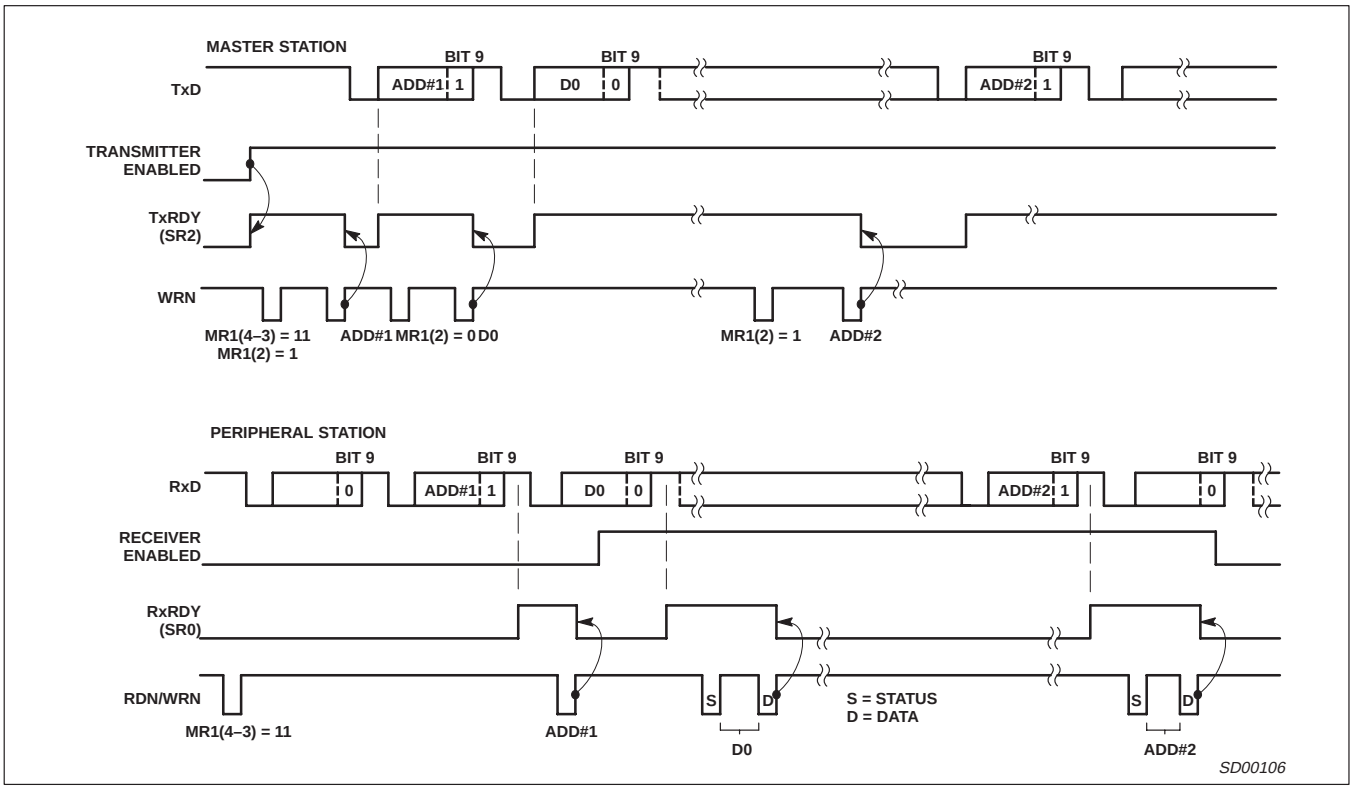
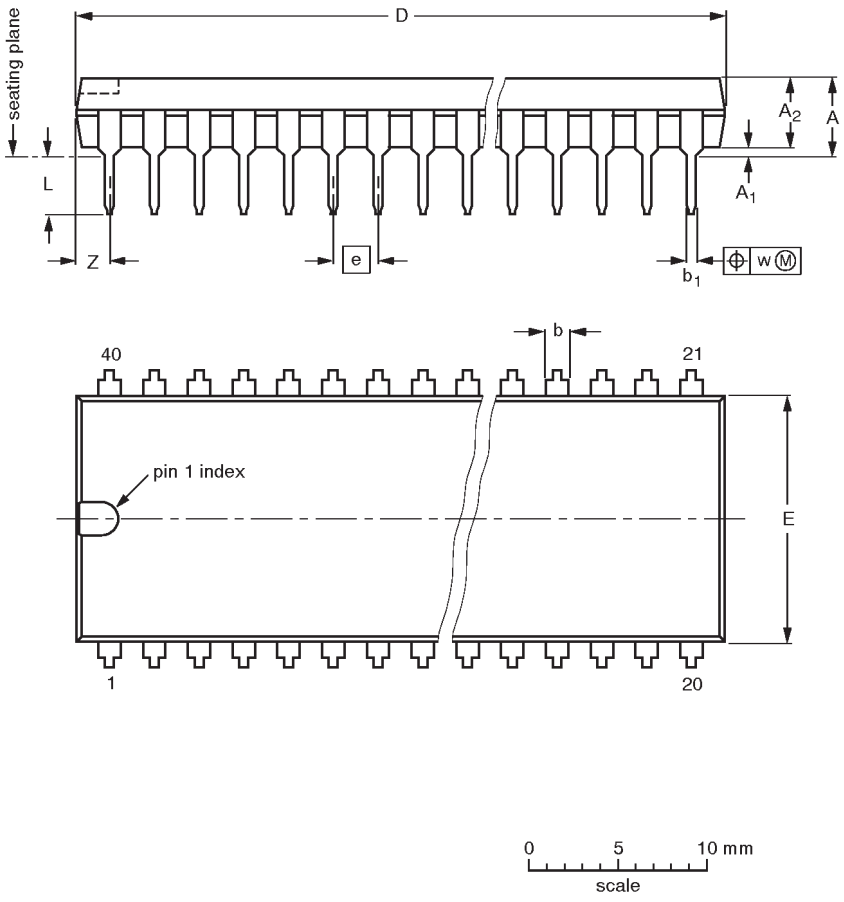


Figure 12. Wake-Up Mode

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

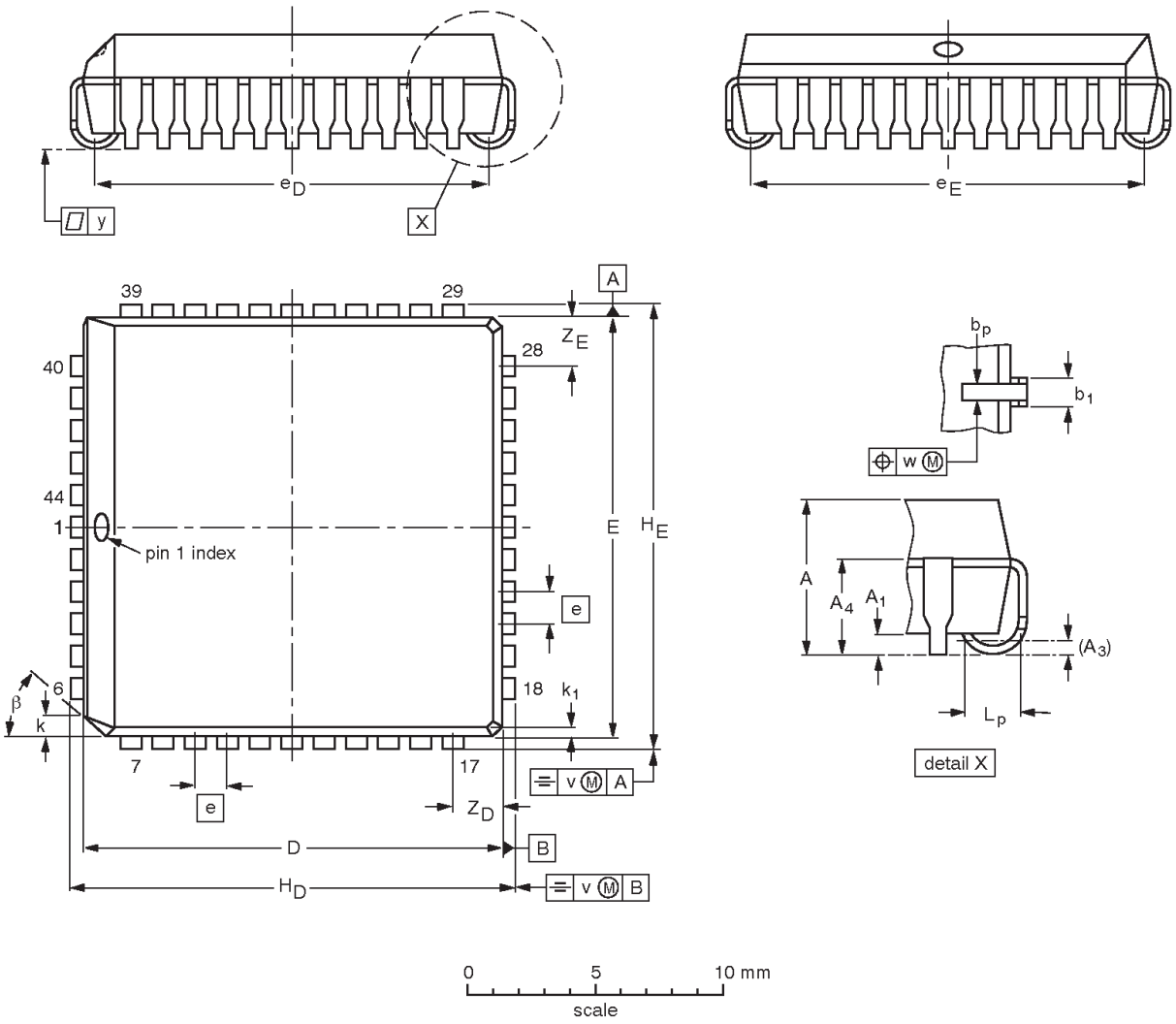
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~95-02-25~~ 97-12-16

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Date of release: 09-98

Document order number: 9397 750 04363

Let's make things better.

Philips Semiconductors

PHILIPS