

# PTN3332

High speed differential line receiver

Rev. 01 — 07 January 2004

Product data

## 1. Description

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The PTN3332 is a differential line receiver that implements the electrical characteristics of Low-Voltage Differential Signaling (LVDS). This device meets or exceeds the requirements of the ANSI *TIA/EIA-644 Standard*. LVDS is used to achieve higher data rates on commonly used media. LVDS overcomes the limitations of achievable slew rates and EMI restrictions of previous differential signaling techniques. The PTN3332 operates at a 3.3 volt supply level. Any of the four differential receivers provides a valid logical output state with a  $\pm 100$  mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 volt of ground potential difference between two LVDS nodes.

The intended application of this device is for point-to-point baseband transmission rates over a controlled impedance media of approximately 100  $\Omega$ . The maximum rates and distance of data transfer are dependent upon the attenuation characteristics of the media selected and the noise coupling to the environment.

The PTN3332 is designed to function over the full industrial temperature range of  $-40$  °C to  $+85$  °C.

## 2. Features

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- Meets or exceeds the requirements of ANSI *TIA/EIA-644 Standard*
- Designed for signaling rates of up to 400 Mbps
- Differential input thresholds of  $\pm 100$  mV
- Power dissipation of 60 mW typical at 200 MHz
- Typical propagation delay of 2.6 ns
- Low Voltage TTL (LVTTTL) logic output levels
- Pin compatible with AM26LS32 and SN65LVDS32
- Open-circuit fail safe.

## 3. Applications

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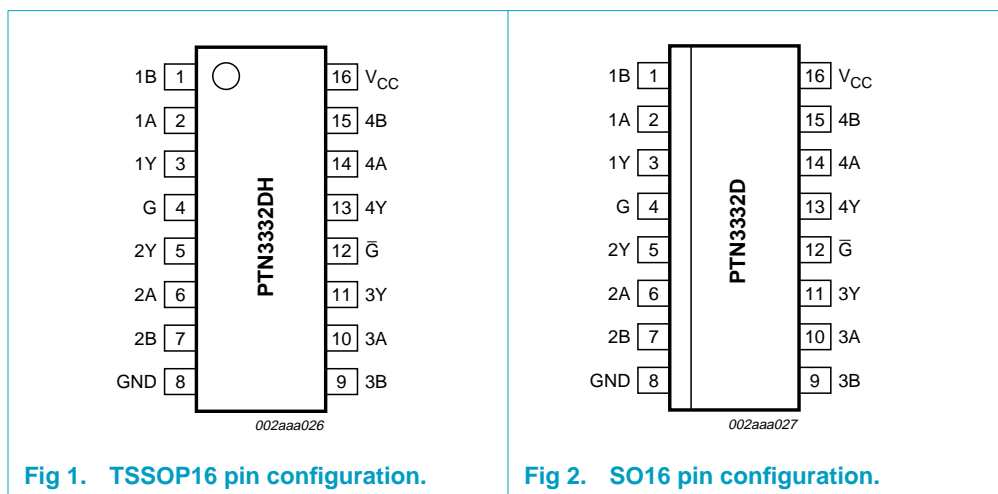
- Low voltage, low EMI, high speed differential signal receiver
- Point-to-point high speed data transmission
- High performance switches and routers.



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## 4. Pinning information

### 4.1 Pinning



### 4.2 Pin description

Table 1: Pin description

Symbol	Pin	Description
1B	1	LVDS inverting input
1A	2	LVDS non-inverting input
1Y	3	LVTTL output
G	4	Enable (active-HIGH)
2Y	5	LVTTL output
2A	6	LVDS non-inverting input
2B	7	LVDS inverting input
GND	8	Ground
3B	9	LVDS inverting input
3A	10	LVDS non-inverting input
3Y	11	LVTTL output
$\bar{G}$	12	Enable (active-LOW)
4Y	13	LVTTL output
4A	14	LVDS non-inverting input
4B	15	LVDS inverting input
V <sub>CC</sub>	16	Supply

## 5. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PTN3332DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PTN3332D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

## 6. Functional diagram division

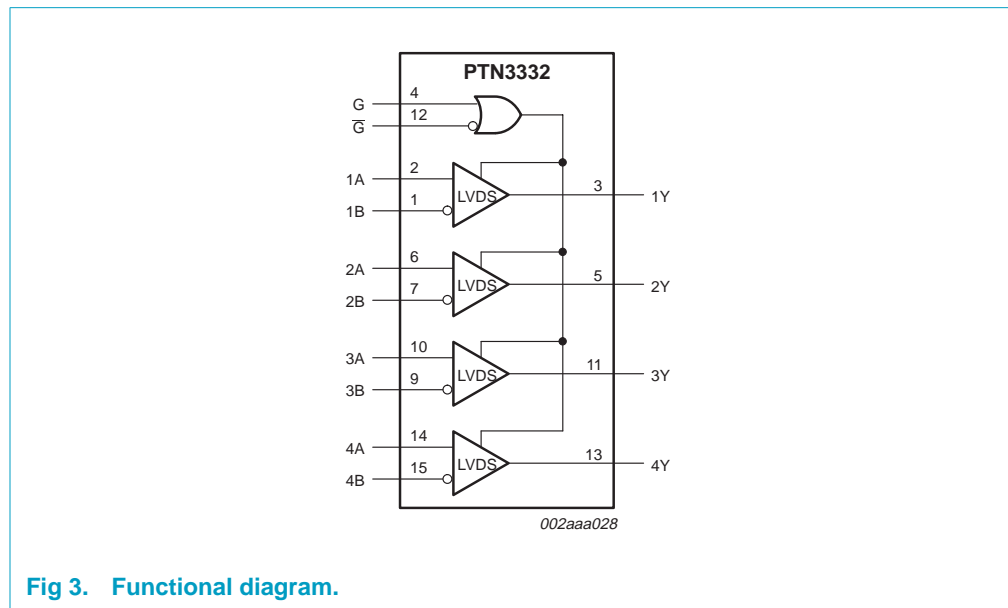


Fig 3. Functional diagram.

## 7. Functional description

### 7.1 Function table

Table 3: Function table division

Differential input A, B	Enables		Output Y
	G	$\bar{G}$	
$V_{ID} \geq 100 \text{ mV}$	H	X	H
	X	L	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	X	?
	X	L	?
$V_{ID} \leq -100 \text{ mV}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	L
	X	L	L

[1] H = HIGH level; L = LOW level; X = irrelevant; Z = high impedance; ? = indeterminate state.

## 8. Limiting values

**Table 4: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	supply voltage	-0.5	4.0	V
$V_I$	input voltage (enables and outputs)	-0.5	$V_{CC} + 0.5$	V
	input voltage (A or B inputs)	-0.5	4.0	V
$T_{amb}$	operating ambient temperature range	-40	+85	°C
$T_j$	operating junction temperature	-40	+150	°C
$T_{stg}$	storage temperature range	-65	+150	°C
	ESD	>2	-	kV

- [1] Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## 9. Recommended operating conditions

**Table 5: Recommended operating conditions**

Symbol	Parameter	Min	Nom	Max	Unit
$V_{CC}$	supply voltage	3	3.3	3.6	V
$V_{IH}$	HIGH-level input voltage	2	-	-	V
$V_{IL}$	LOW-level input voltage	-	-	0.8	V
$V_{ID}$	Magnitude of differential input voltage	0.1	-	0.6	V
$V_{IC}$	Common-mode input voltage	$V_{ID}/2$	-	$2.4 - V_{ID}/2$	V
$T_{amb}$	Operating temperature range	-40	-	+85	°C

## 10. Static characteristics

**Table 6: DC electrical characteristics**

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{rr+}$	positive differential input voltage threshold	See Figure 4 and Table 8.	–	–	100	mV
$V_{rr-}$	negative differential input voltage threshold		–100	–	–	mV
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -8$ mA	2.4	–	–	V
		$I_{OH} = -4$ mA	2.8	–	–	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 8$ mA	–	–	0.4	V
$I_{CC}$	supply current	enabled, no load	–	10	18	mA
		disabled	–	0.25	0.5	mA
$I_I$	input current (A or B inputs)	$V_I = 0$ V	–2	–10	–20	$\mu$ A
		$V_I = 2.4$ V	–1.2	–3	–	$\mu$ A
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_{CC} = 0$ V; $V_I = 3.6$ V	–	6	20	$\mu$ A
$I_{IH}$	HIGH-level input current (G or $\overline{G}$ inputs)	$V_{IH} = 2$ V	–	–	10	$\mu$ A
$I_{IL}$	LOW-level input current (G or $\overline{G}$ inputs)	$V_{IL} = 0.8$ V	–	–	10	$\mu$ A
$I_{OZ}$	High-impedance output current	$V_O = 0$ V or $V_{CC}$	–10	–	10	$\mu$ A

[1] All typical values are at  $T_{amb} = 25$  °C and  $V_{CC} = 3.3$  V.

## 11. Dynamic characteristics

**Table 7: AC electrical characteristics**

Over recommended operating conditions, unless otherwise noted.

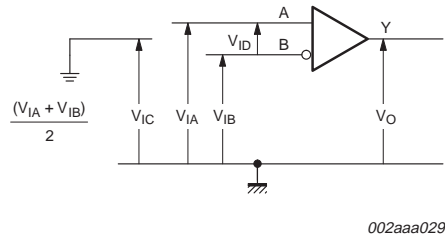
Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$t_{PLH}$	propagation delay, LOW-to-HIGH level output	$C_L = 10$ pF	1.3	2.6	6	ns
$t_{PHL}$	propagation delay, HIGH-to-LOW level output	See Figure 5.	1.3	2.5	6	ns
$t_r$	output rise time (20 to 80%)		–	0.6	–	ns
$t_f$	output fall time (80 to 20%)		–	0.7	–	ns
$t_{sk(p)}$	pulse skew ( $t_{PHL} - t_{PLH}$ )		–	–	0.4	ns
$t_{sk(o)}$	channel-to-channel output skew		[2]	0.1	0.3	ns
$t_{sk(p-p)}$	part-to-part skew		[3]	–	1	ns
$t_{PZH}$	propagation delay, high-impedance to HIGH-level output	See Figure 6.	–	8	12	ns
$t_{PZL}$	propagation delay, high-impedance to LOW-level output		–	3	12	ns
$t_{PHZ}$	propagation delay, HIGH-level to high-impedance output		–	6.5	12	ns
$t_{PLZ}$	propagation delay, LOW-level to high-impedance output		–	5.5	12	ns

[1] All typical values are at  $T_{amb} = 25$  °C, and  $V_{CC} = 3.3$  V.

[2]  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

[3]  $t_{sk(p-p)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

## 12. Test figures



**Fig 4. Voltage definitions.**

**Table 8: Receiver minimum and maximum input threshold test voltages**

Applied voltages		Resulting differential input voltage	Resulting common-mode input voltage
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

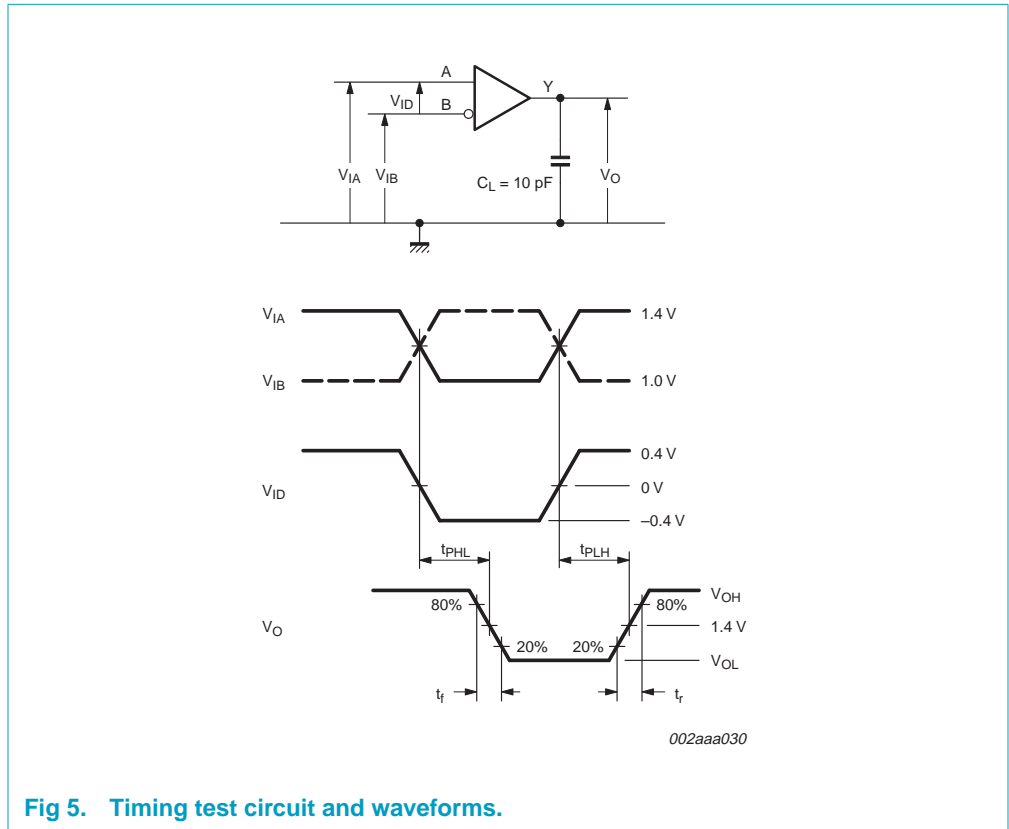


Fig 5. Timing test circuit and waveforms.



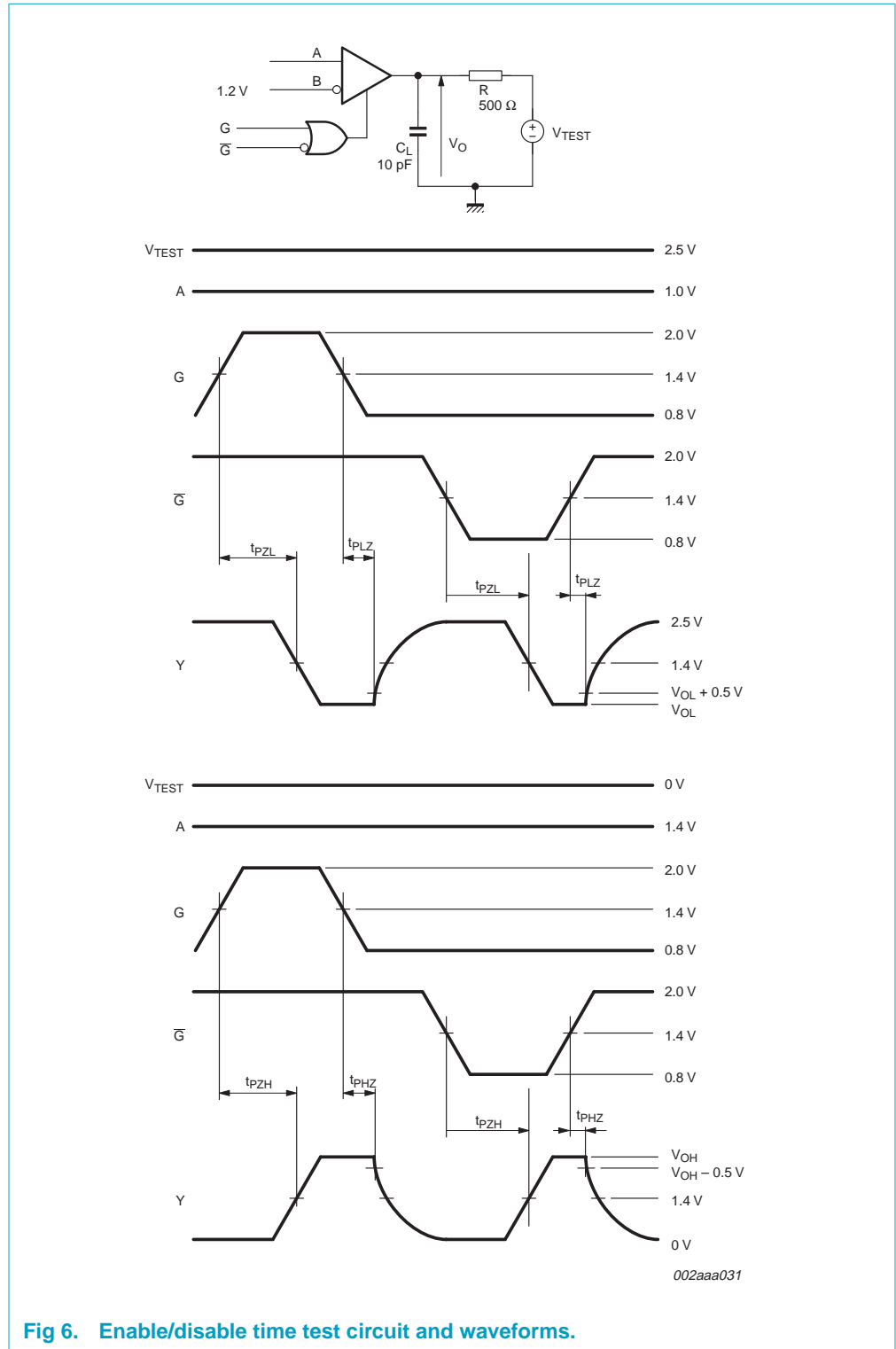


Fig 6. Enable/disable time test circuit and waveforms.

### 13. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

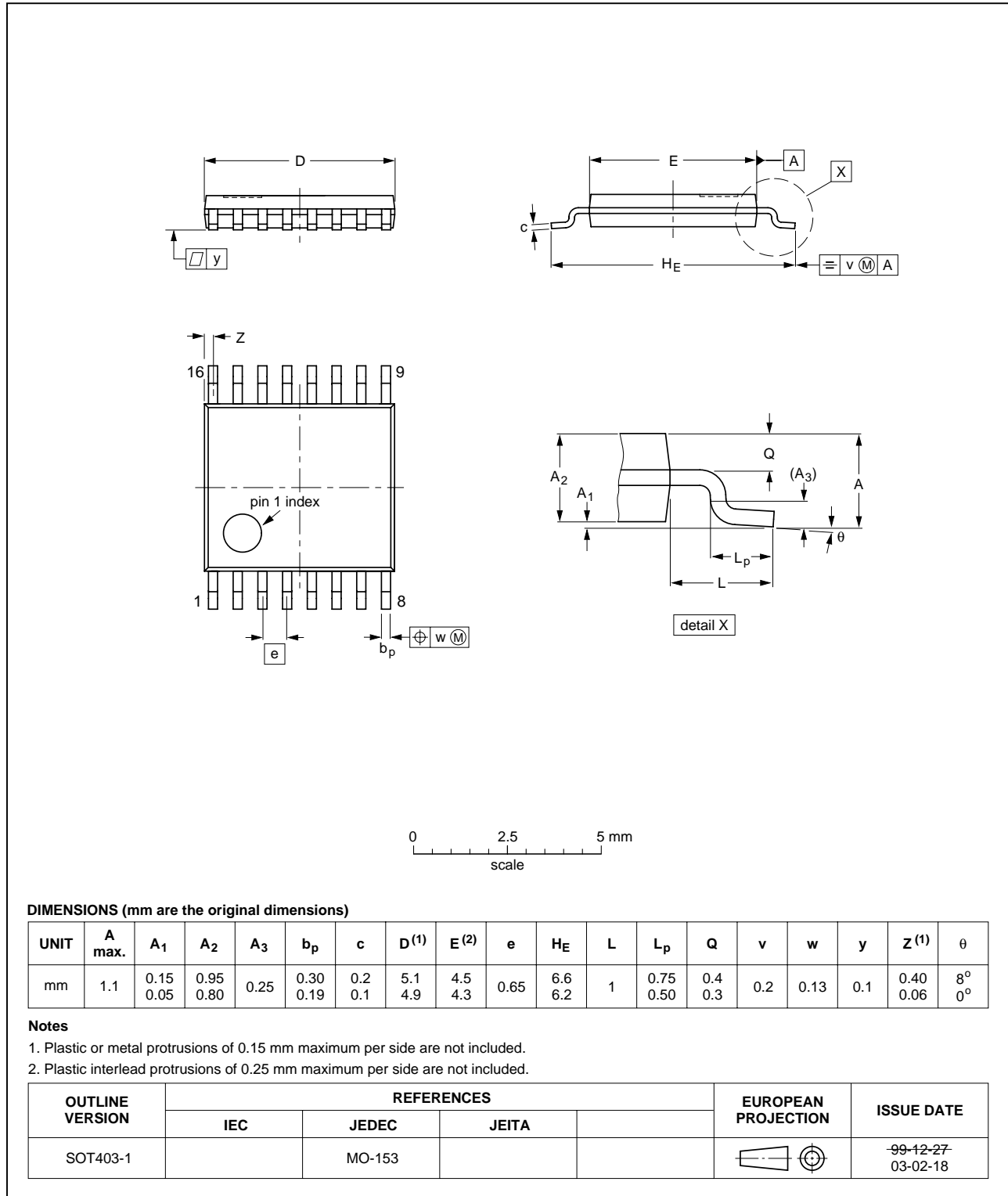


Fig 7. TSSOP16 package outline (SOT403-1).

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

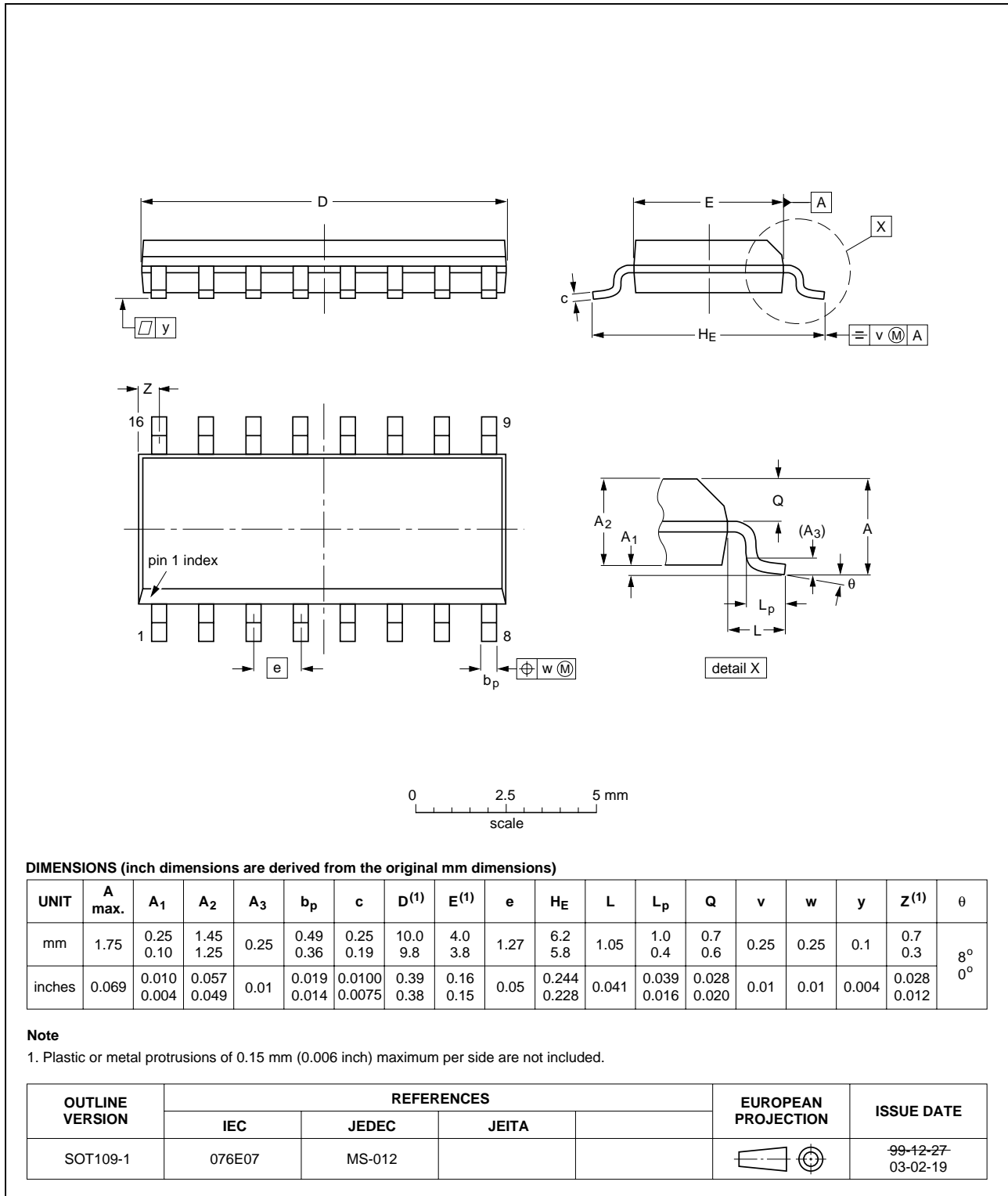


Fig 8. SO16 package outline (SOT109-1).

## 14. Soldering

### 14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

### 14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

#### 14.5 Package related soldering information

**Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods**

Package <sup>[1]</sup>	Soldering method	
	Wave	Reflow <sup>[2]</sup>
BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>[4]</sup>	suitable
PLCC <sup>[5]</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>[5][6]</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>[7]</sup>	suitable
CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ }^{\circ}\text{C} \pm 10\text{ }^{\circ}\text{C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a  $45^{\circ}$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 15. Revision history

Table 10: Revision history

Rev	Date	CPCN	Description
01	20040107	-	Product data (9397 750 08341). ECN 853-2443 A14996 dated 15 December 2003.

## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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