

PMN34UN

μ TrenchMOS™ ultra low level FET

Rev. 01 — 26 February 2003

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMN34UN in SOT457 (TSOP6).

2. Features

- TrenchMOS™ technology
- Very fast switching
- Low threshold voltage
- Surface mount package.

3. Applications

- Battery-powered motor control
- Load switch in notebook computers
- High-speed switch in set top box power supplies
- Driver FET in DC-to-DC converters.

4. Pinning information

Table 1: Pinning - SOT457 (TSOP6), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,5,6	drain (d)	<p>Top view MBK092</p> <p>SOT457 (TSOP6)</p>	<p>MBB076</p>
3	gate (g)		
4	source (s)		

5. Quick reference data

Table 2: Quick reference data

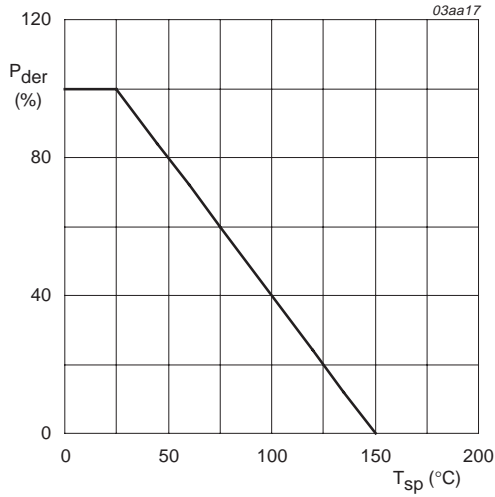
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V}$	-	4.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	1.75	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ °C}$	38	46	m Ω
		$V_{GS} = 2.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ °C}$	45	54	m Ω
		$V_{GS} = 1.8\text{ V}; I_D = 1.5\text{ A}; T_j = 25\text{ °C}$	54	77	m Ω

6. Limiting values

Table 3: Limiting values

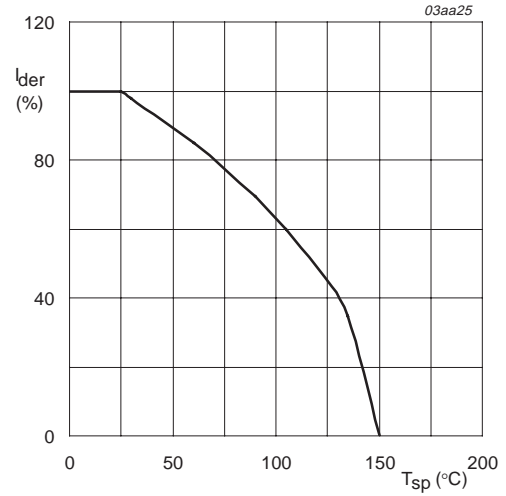
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 8	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V};$ Figure 2 and 3	-	4.9	A
		$T_{sp} = 70\text{ °C}; V_{GS} = 4.5\text{ V};$ Figure 2	-	3.9	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	19.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C};$ Figure 1	-	1.75	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	1.45	A



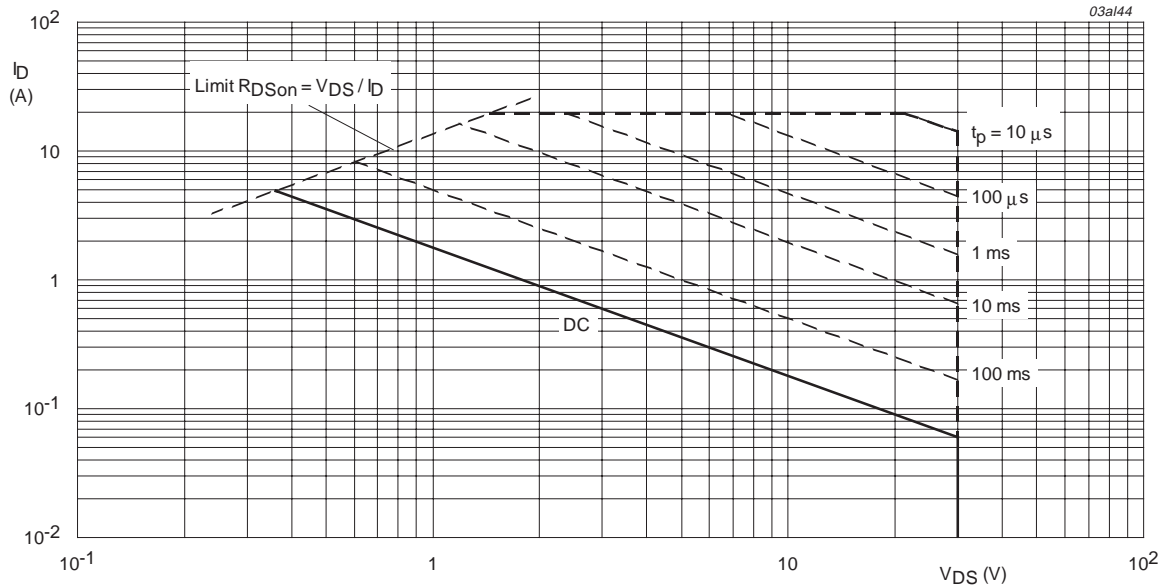
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	70	K/W

7.1 Transient thermal impedance

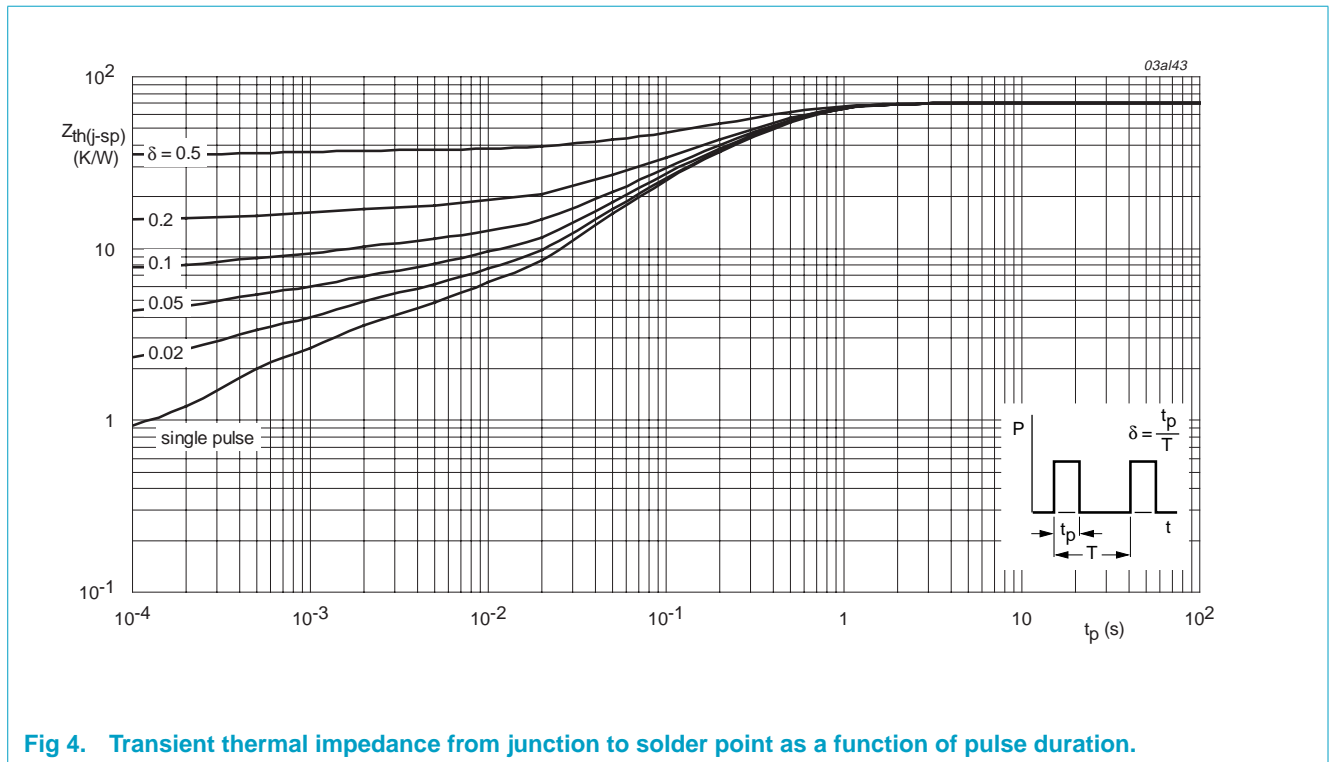


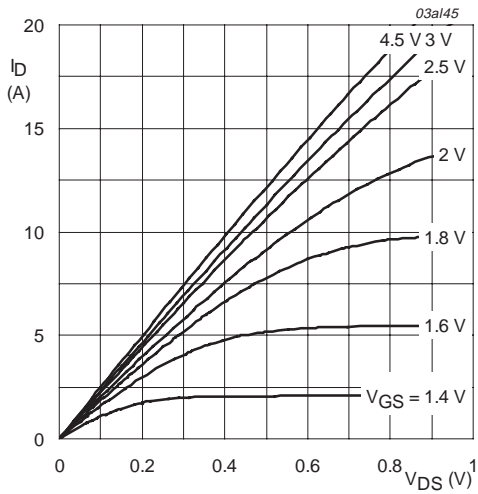
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

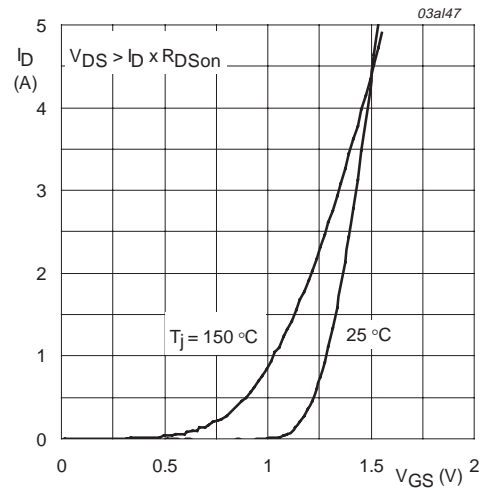
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9	0.45	0.7	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	0.01	1.0	μA
		$T_j = 55\text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 8\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 2\text{ A}$; Figure 7 and 8	-	38	46	$\text{m}\Omega$
		$V_{GS} = 2.5\text{ V}$; $I_D = 2\text{ A}$; Figure 7 and 8	-	45	54	$\text{m}\Omega$
		$V_{GS} = 1.8\text{ V}$; $I_D = 1.5\text{ A}$; Figure 7 and 8	-	54	77	$\text{m}\Omega$
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{DD} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; Figure 13	-	9.9	-	nC
Q_{gs}	gate-source charge		-	1.4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2.1	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	790	-	pF
C_{oss}	output capacitance		-	90	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$; $R_D = 12\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	10	-	ns
t_r	rise time		-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
t_f	fall time		-	10	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1.7\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.73	1.2	V



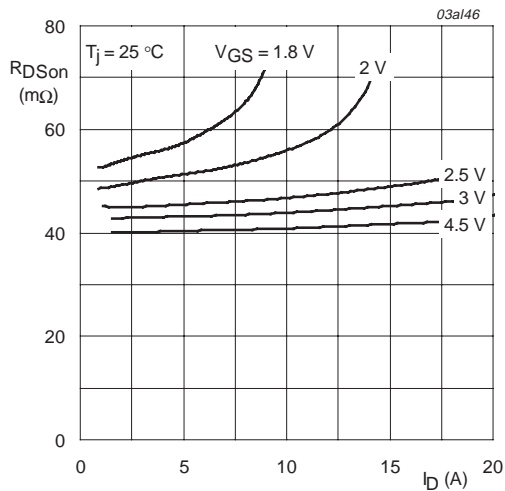
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



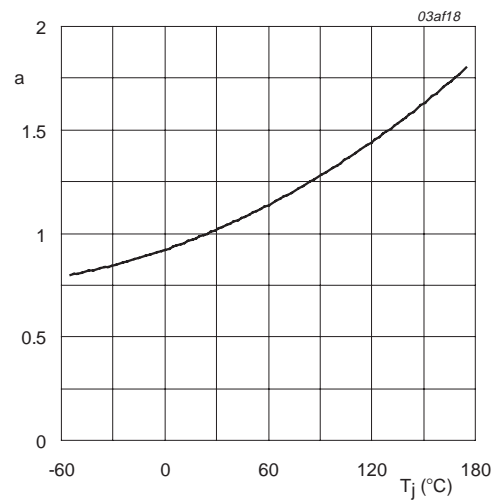
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



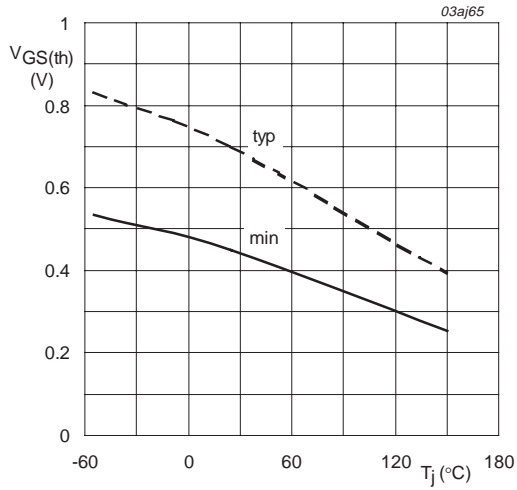
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



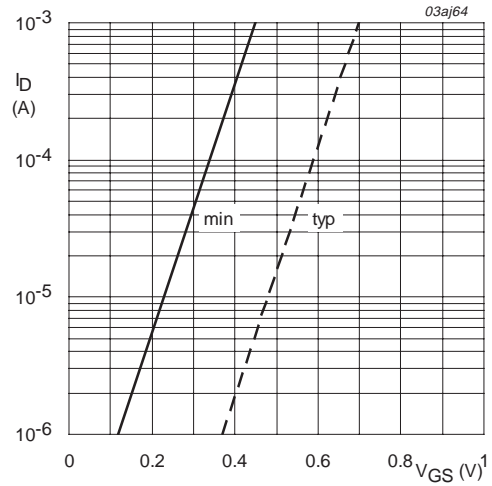
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



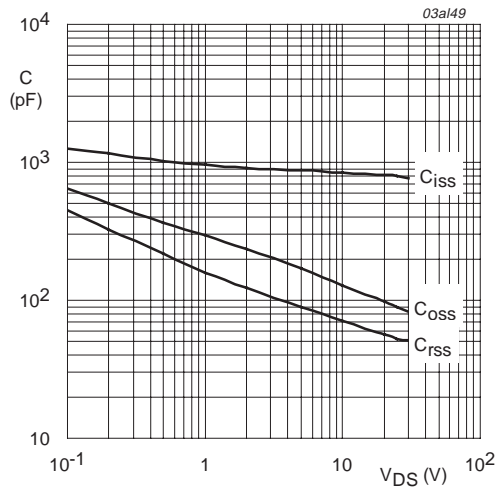
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



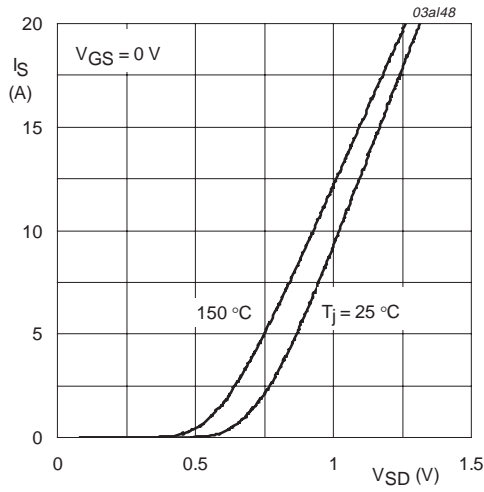
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



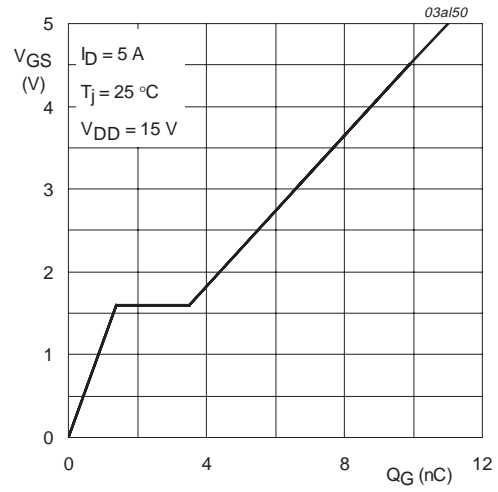
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 5\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 6 leads

SOT457

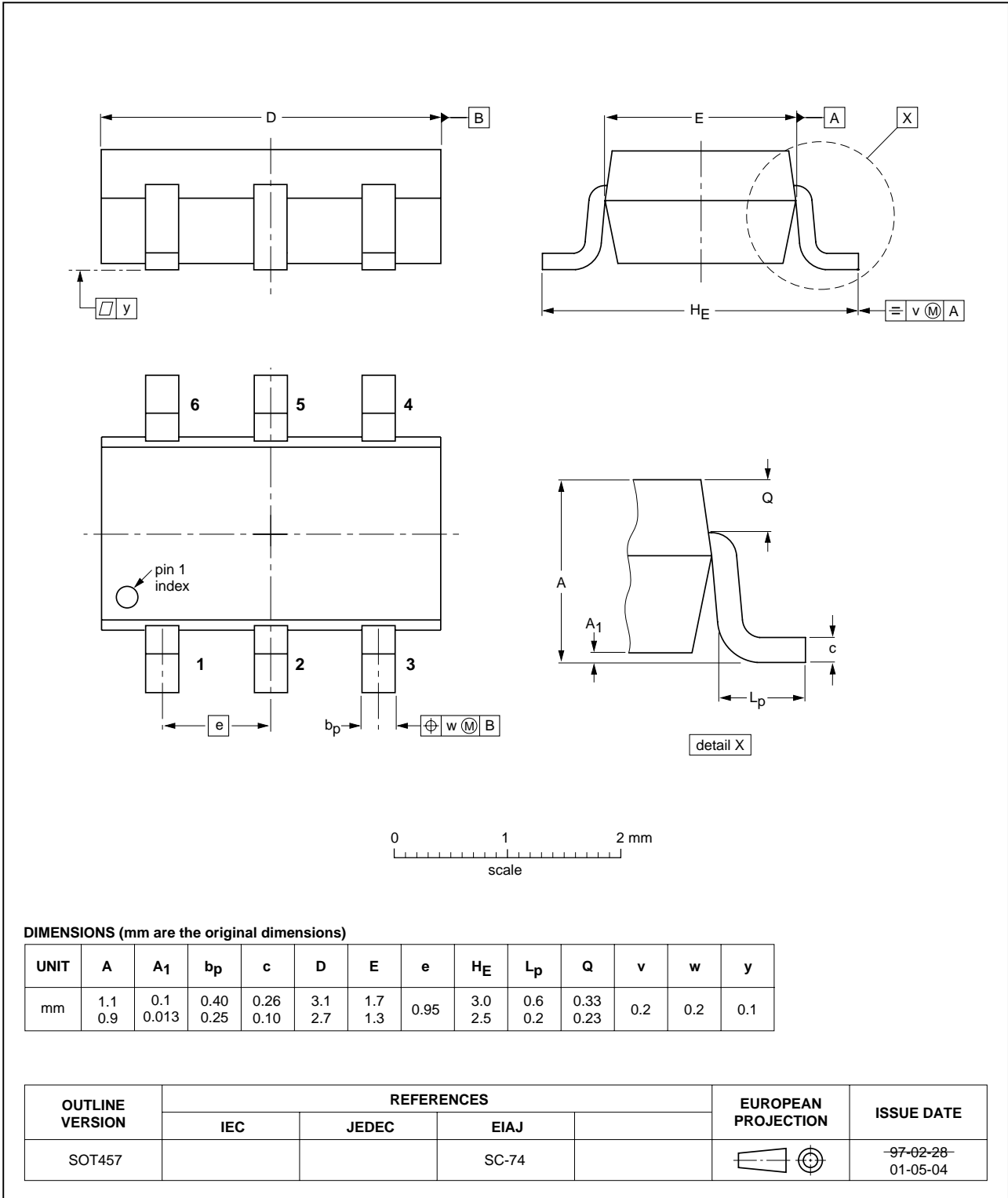


Fig 14. SOT457 (TSOP6).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20030226	-	Product data (9397 750 10979)

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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