

Programmable logic sequencer

(16 × 45 × 12)

PLS159A

DESCRIPTION

The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C . It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output (\bar{C}). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement (\bar{I} , \bar{B} , \bar{Q} , \bar{C}) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates can drive bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. There are 4 AND gates for the Asynchronous Preset/Reset functions.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

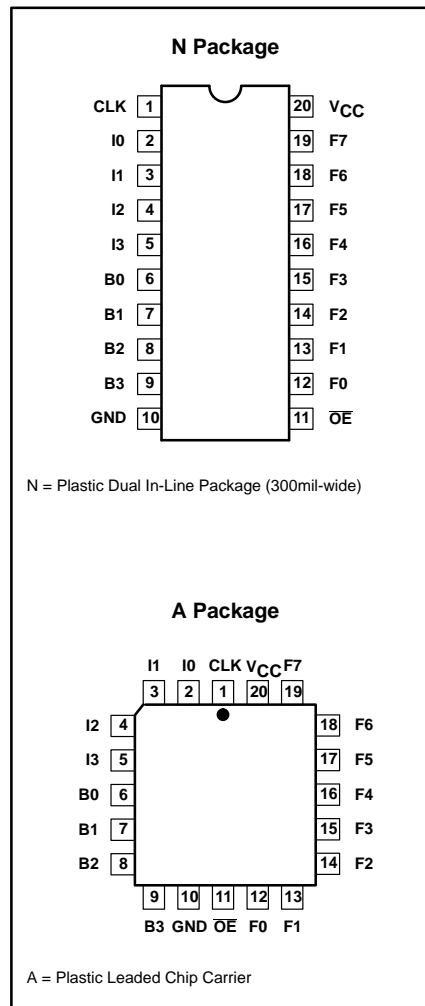
FEATURES

- High-speed version of PLS159
- $f_{MAX} = 18\text{MHz}$
 - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
 - 32 logic terms
 - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops ($F_n = 1$)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\bar{O}E$ control
- Positive edge-triggered clock
- Input loading: $-100\mu\text{A}$ (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

PIN CONFIGURATIONS



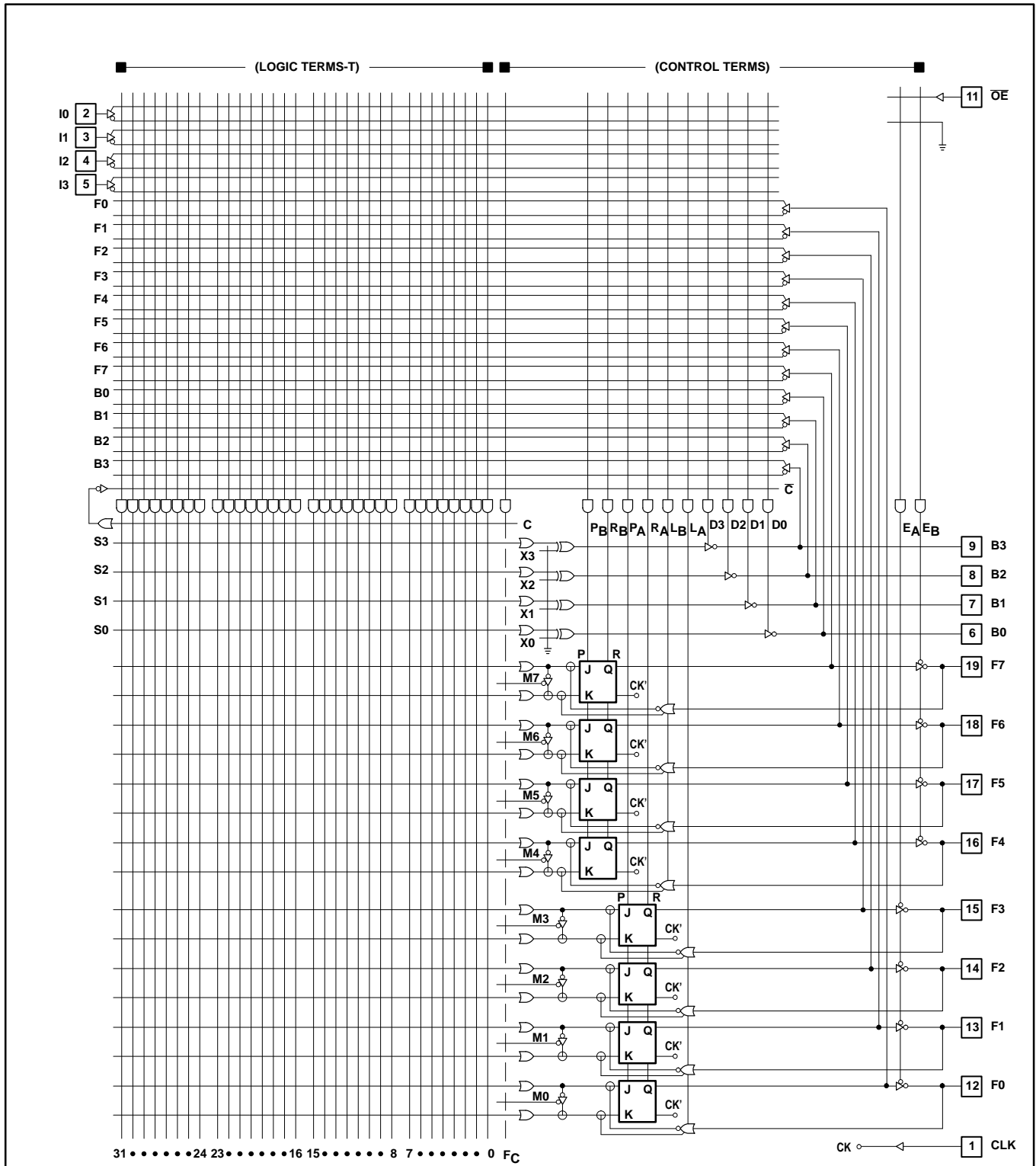
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Dual In-Line Package (300mil-wide)	PLS159AN	0408D
20-Pin Plastic Leaded Chip Carrier	PLS159AA	0400E

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LOGIC DIAGRAM



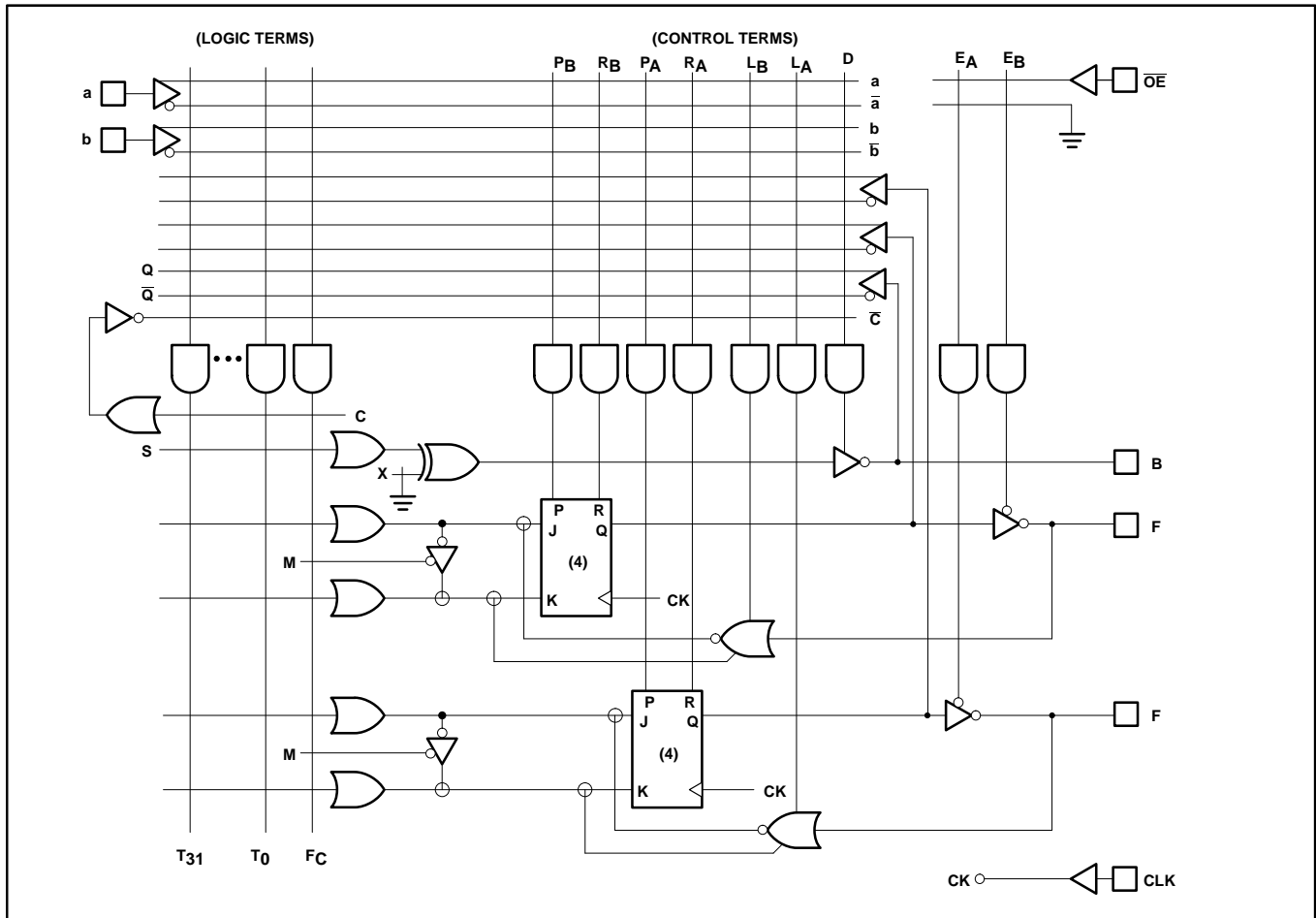
NOTES:

1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. Programmable connection.

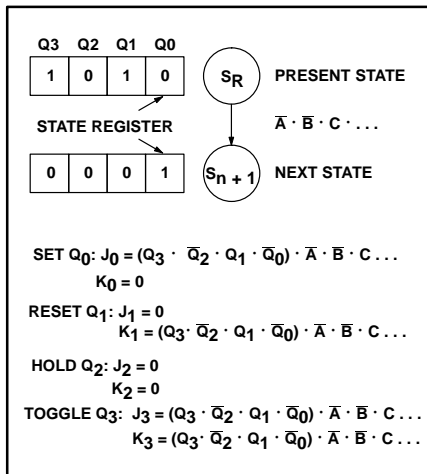
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FUNCTIONAL DIAGRAM



LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

OE	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	\bar{Q}
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	\bar{Q}	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:

- Positive Logic:
 $J\text{-}K = T_0 + T_1 + T_2 \dots T_{31}$
 $T_n = \bar{C} \cdot (I_0 \cdot I_1 \cdot I_2 \dots) \cdot (Q_0 \cdot Q_1 \dots) \cdot (B_0 \cdot B_1 \dots)$
- ↑ denotes transition from Low to High level.
- X = Don't care
- * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
- At P = R = H, Q = H. The final state of Q depends on which is released first.
- ** = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

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VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. \overline{OE} is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

CAUTION: PLS159A**PROGRAMMING ALGORITHM**

The programming voltage required to program the PLS159A is higher (17.5V) than that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to insure that the correct algorithm is used.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage		+7	V _{DC}
V _{IN}	Input voltage		+5.5	V _{DC}
V _{OUT}	Output voltage		+5.5	V _{DC}
I _{IN}	Input currents	-30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{amb}	Operating temperature range	0	+75	°C
T _{stg}	Storage temperature range	-65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

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DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage²						
V_{IH}	High	$V_{\text{CC}} = \text{MAX}$	2.0			V
V_{IL}	Low	$V_{\text{CC}} = \text{MIN}$			0.8	V
V_{IC}	Clamp	$V_{\text{CC}} = \text{MIN}$, $I_{\text{IN}} = -12\text{mA}$		-0.8	-1.2	V
Output voltage²						
V_{OH}	High	$V_{\text{CC}} = \text{MIN}$, $I_{\text{OH}} = -2\text{mA}$	2.4			V
V_{OL}	Low	$I_{\text{OL}} = 10\text{mA}$		0.35	0.5	V
Input current						
I_{IH}	High	$V_{\text{CC}} = \text{MAX}$, $V_{\text{IN}} = 5.5\text{V}$		<1	80	μA
I_{IL}	Low	$V_{\text{IN}} = 0.45\text{V}$		-10	-100	μA
Output current						
$I_{\text{O(OFF)}}$	Hi-Z state ^{4, 7}	$V_{\text{CC}} = \text{MAX}$, $V_{\text{OUT}} = 5.5\text{V}$		1	80	μA
		$V_{\text{OUT}} = 0.45\text{V}$		-1	-140	μA
I_{OS}	Short circuit ^{3, 5}	$V_{\text{OUT}} = 0\text{V}$	-15		-70	mA
I_{CC}	V_{CC} supply current ⁶	$V_{\text{CC}} = \text{MAX}$		150	190	mA
Capacitance						
C_{IN}	Input	$V_{\text{CC}} = 5.0\text{V}$, $V_{\text{IN}} = 2.0\text{V}$		8		pF
C_{OUT}	Output	$V_{\text{OUT}} = 2.0\text{V}$		15		pF

NOTES:

- All typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^{\circ}\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test one at a time.
- Measured with V_{IH} applied to $\overline{\text{OE}}$.
- Duration of short circuit should not exceed 1 second.
- I_{CC} is measured with the $\overline{\text{OE}}$ input grounded, all other inputs at 4.5V and the outputs open.
- Leakage values are a combination of input and output leakage.

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AC ELECTRICAL CHARACTERISTICS

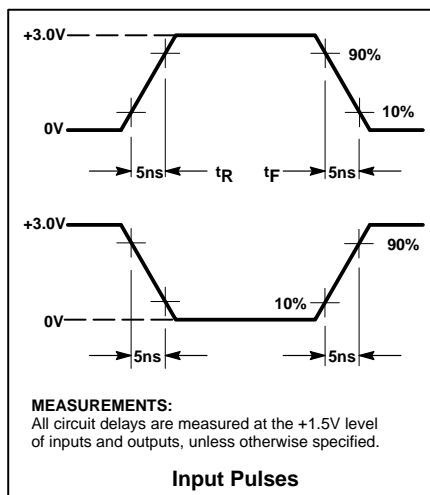
0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, R₁ = 470Ω, R₂ = 1kΩ

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS			UNIT
					MIN	TYP ¹	MAX	
Pulse width								
t _{CKH}	Clock ² High	CK +	CK -	C _L = 30pF	20	15		ns
t _{CKL}	Clock Low	CK -	CK +	C _L = 30pF	20	15		ns
t _{CKP}	Period	CK +	CK +	C _L = 30pF	55	45		ns
t _{PRH}	Preset/Reset pulse	(I,B) -	(I,B) +	C _L = 30pF	35	30		ns
Setup time⁵								
t _{IS1}	Input	(I,B) ±	CK +	C _L = 30pF	35	30		ns
t _{IS2}	Input (through F _n)	F ±	CK +	C _L = 30pF	15	10		ns
t _{IS3}	Input (through Complement Array) ⁴	(I,B) ±	CK +	C _L = 30pF	55	45		ns
Hold time								
t _{IH1}	Input	(I,B) ±	CK +	C _L = 30pF	0	-5		ns
t _{IH2}	Input (through F _n)	F ±	CK +	C _L = 30pF	15	10		ns
Propagation delay								
t _{CKO}	Clock	CK +	F ±	C _L = 30pF		15	20	ns
t _{OE1}	Output enable ³	\overline{OE} -	F -	C _L = 30pF		20	30	ns
t _{OD1}	Output disable ³	\overline{OE} +	F +	C _L = 5pF		20	30	ns
t _{PD}	Output	(I,B) ±	B ±	C _L = 30pF		25	35	ns
t _{OE2}	Output enable ³	(I,B) +	B ±	C _L = 30pF		20	30	ns
t _{OD2}	Output disable ³	(I,B) -	B +	C _L = 5pF		20	30	ns
t _{PRO}	Preset/Reset	(I,B) +	F ±	C _L = 30pF		35	45	ns
t _{PPR}	Power-on/preset	V _{CC} +	F -	C _L = 30pF		0	10	ns

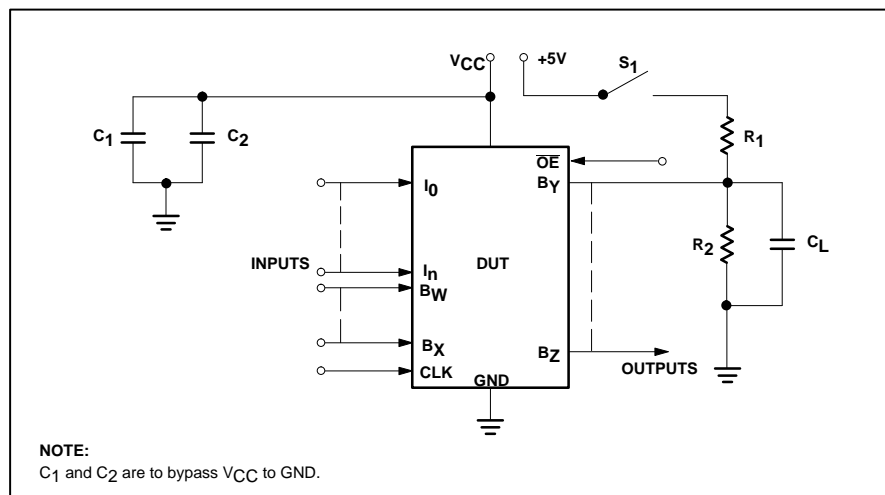
NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} - 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S₁ closed.
4. When using the Complement Array t_{CKP} = 75ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

VOLTAGE WAVEFORMS



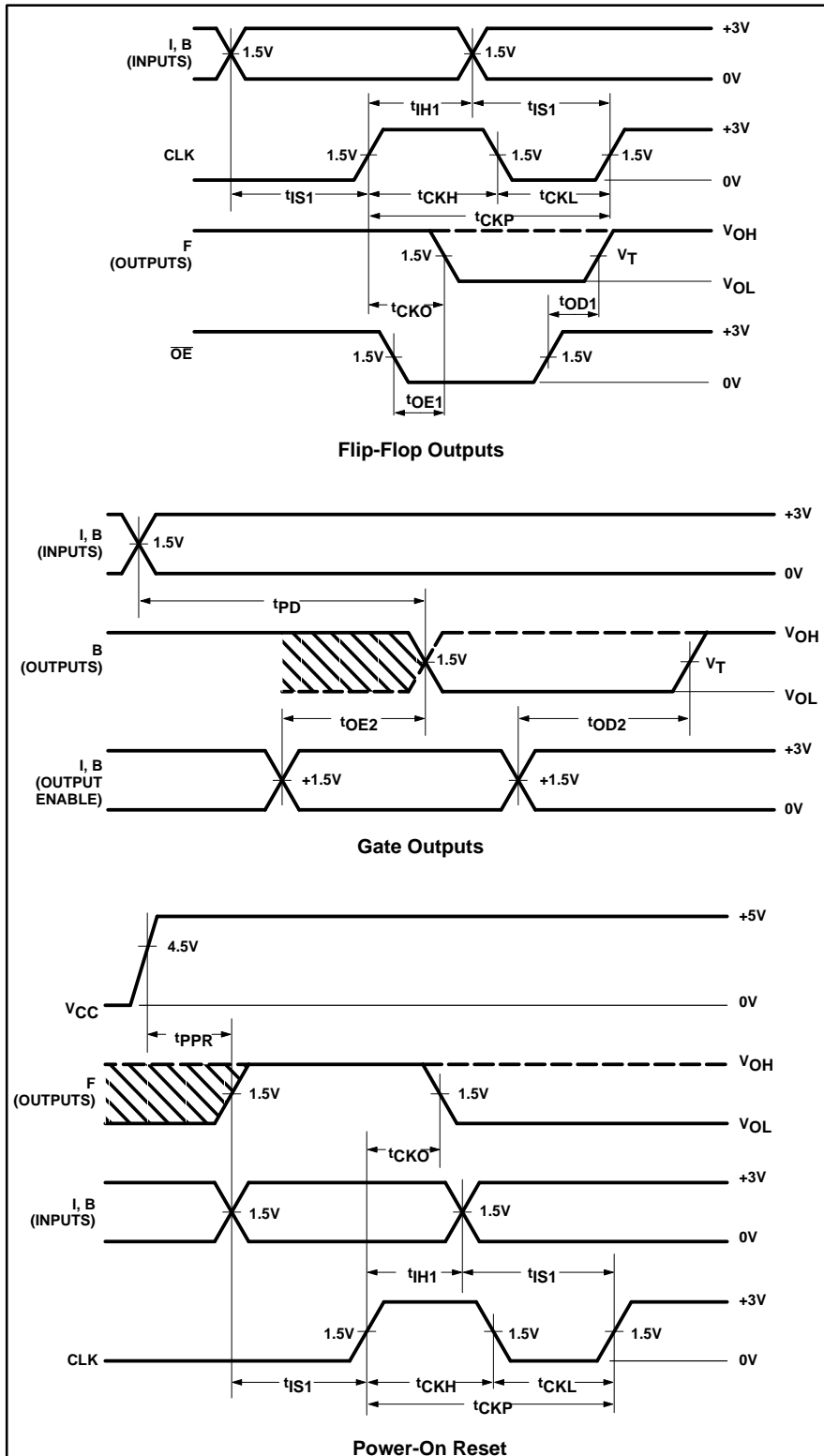
TEST LOAD CIRCUIT



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TIMING DIAGRAMS



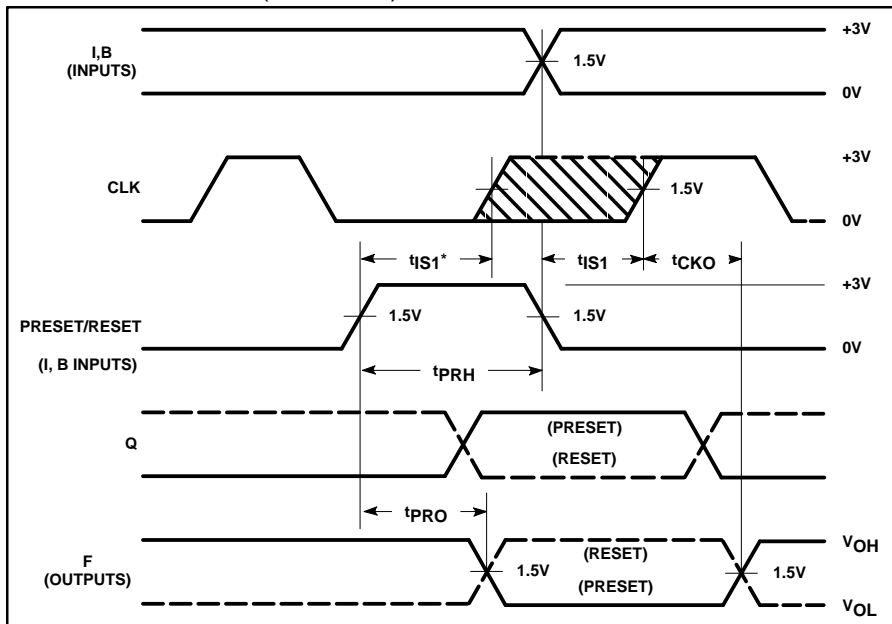
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with OE Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

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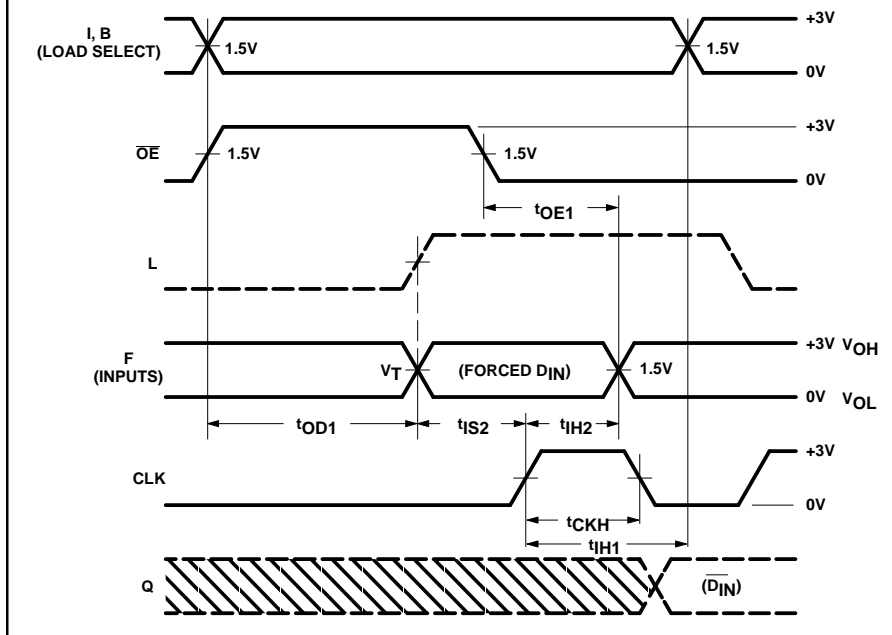
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TIMING DIAGRAMS (Continued)



* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if t_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

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LOGIC PROGRAMMING

The PLS159A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS159A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE,

COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-party Programmer/Software Support*) of this data handbook for additional information.

“AND” ARRAY – (I), (B), (Qp)

<p>(T, FC, L, P, R, D)_n</p> <table border="1"> <thead> <tr> <th>STATE</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>INACTIVE^{1, 2}</td> <td>O</td> </tr> </tbody> </table>	STATE	CODE	INACTIVE ^{1, 2}	O	<p>(T, FC, L, P, R, D)_n</p> <table border="1"> <thead> <tr> <th>STATE</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>I, B, Q</td> <td>H</td> </tr> </tbody> </table>	STATE	CODE	I, B, Q	H	<p>(T, FC, L, P, R, D)_n</p> <table border="1"> <thead> <tr> <th>STATE</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>$\bar{i}, \bar{b}, \bar{q}$</td> <td>L</td> </tr> </tbody> </table>	STATE	CODE	$\bar{i}, \bar{b}, \bar{q}$	L	<p>(T, FC, L, P, R, D)_n</p> <table border="1"> <thead> <tr> <th>STATE</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>DON'T CARE</td> <td>-</td> </tr> </tbody> </table>	STATE	CODE	DON'T CARE	-
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STATE	CODE																		
DON'T CARE	-																		

“COMPLEMENT” ARRAY – (C)

<p>(T_n, FC)</p> <table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>INACTIVE^{1, 3, 5}</td> <td>O</td> </tr> </tbody> </table>	ACTION	CODE	INACTIVE ^{1, 3, 5}	O	<p>(T_n, FC)</p> <table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>GENERATE⁵</td> <td>A</td> </tr> </tbody> </table>	ACTION	CODE	GENERATE ⁵	A	<p>(T_n, FC)</p> <table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>PROPAGATE</td> <td>•</td> </tr> </tbody> </table>	ACTION	CODE	PROPAGATE	•	<p>(T_n, FC)</p> <table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>TRANSPARENT</td> <td>-</td> </tr> </tbody> </table>	ACTION	CODE	TRANSPARENT	-
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GENERATE ⁵	A																		
ACTION	CODE																		
PROPAGATE	•																		
ACTION	CODE																		
TRANSPARENT	-																		

“OR” ARRAY – (F-F CONTROL MODE)

<table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>J-K OR D (CONTROLLED)¹</td> <td>A</td> </tr> </tbody> </table>	ACTION	CODE	J-K OR D (CONTROLLED) ¹	A	<table border="1"> <thead> <tr> <th>ACTION</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>J-K ONLY</td> <td>•</td> </tr> </tbody> </table>	ACTION	CODE	J-K ONLY	•
ACTION	CODE								
J-K OR D (CONTROLLED) ¹	A								
ACTION	CODE								
J-K ONLY	•								

“OR” ARRAY – (Q_n = D-Type)

<table border="1"> <thead> <tr> <th>T_n STATUS</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>ACTIVE (Set)¹</td> <td>A</td> </tr> </tbody> </table>	T _n STATUS	CODE	ACTIVE (Set) ¹	A	<table border="1"> <thead> <tr> <th>T_n STATUS</th> <th>CODE</th> </tr> </thead> <tbody> <tr> <td>INACTIVE (Reset)</td> <td>•</td> </tr> </tbody> </table>	T _n STATUS	CODE	INACTIVE (Reset)	•
T _n STATUS	CODE								
ACTIVE (Set) ¹	A								
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INACTIVE (Reset)	•								

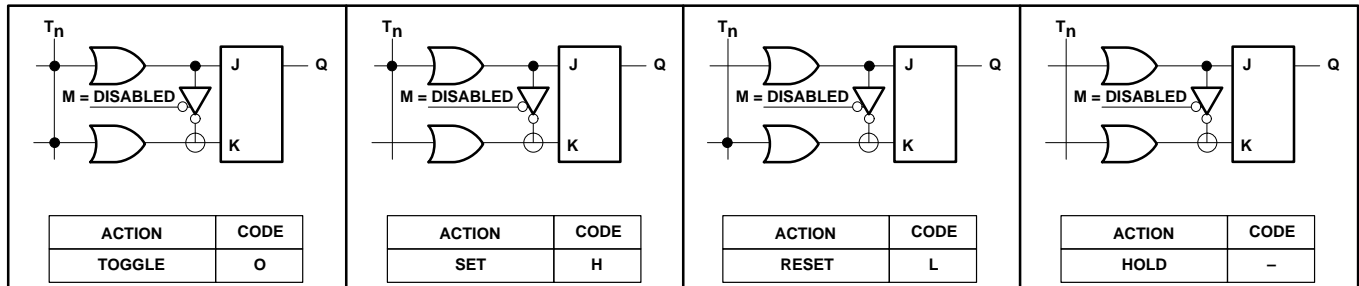
Notes on following page.

CAUTION:
THE PLS159A Programming Algorithm is different from the PLS159.

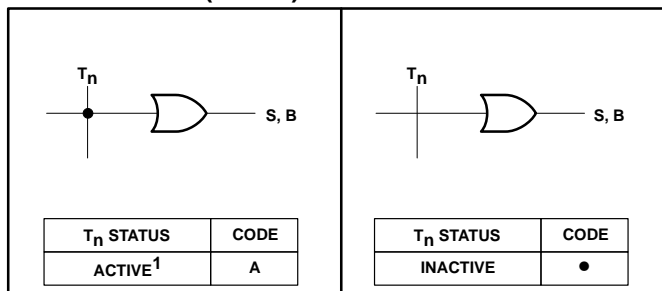
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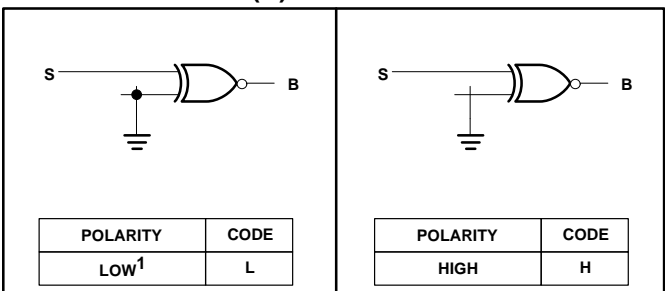
“OR” ARRAY – (Q_n = J-K Type)



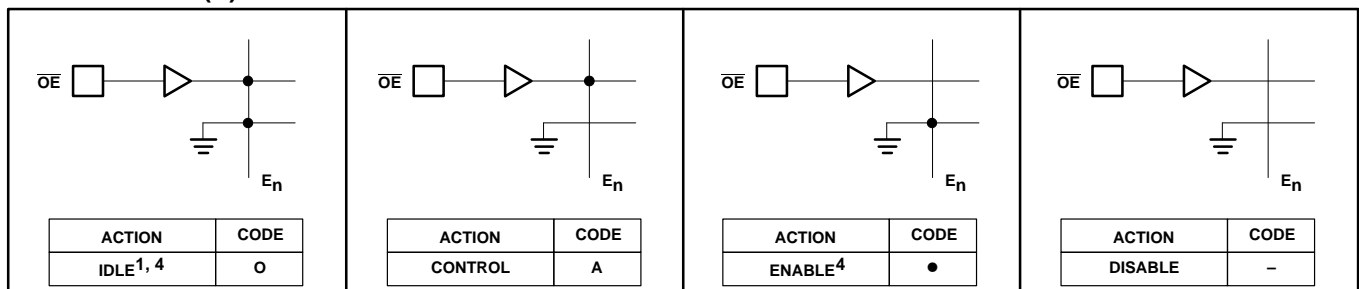
“OR” ARRAY – (S or B)



“EX-OR” ARRAY – (B)



“OE” ARRAY – (E)



NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)_n will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)_n due to their lack of “OR” array links.

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SNAP RESOURCE SUMMARY DESIGNATIONS

