DATA SHEET

74LVC1G74

Single D-type flip-flop with set and reset; positive edge trigger

Product specification
Supersedes data of 2004 Sep 09

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Philips
Semiconductors

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Single D-type flip-flop with set and reset; positive edge trigger

74LVC1G74

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC1G74 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC1G74 is a single positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}$D) and ($\overline{R}$D) inputs, and complementary Q and $\overline{Q}$ outputs.

This device is fully specified for partial power down applications using I_{off}. The I_{off} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay			
	CP to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	3.5	ns
	$\overline{S}$D to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
	$\overline{R}$D to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V	280	MHz
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; notes 1 and 2	15	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = number of inputs switching;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLES

Table 1 Asynchronous operation. See note 1.

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 Synchronous operation. See note 1.

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note to Tables 1 and 2

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   ↑ = LOW-to-HIGH CP transition;
   Q_{n+1} = state after the next LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G74DP	–40 °C to +125 °C	8	TSSOP8	plastic	SOT505-2	V74
74LVC1G74DC	–40 °C to +125 °C	8	VSSOP8	plastic	SOT765-1	V74
74LVC1G74GT	–40 °C to +125 °C	8	XSON8	plastic	SOT833-1	V74

PINNING

SYMBOL	PIN	DESCRIPTION
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
$\overline{Q}$	3	complement flip-flop output
GND	4	ground (0 V)
Q	5	true flip-flop output
$\overline{RD}$	6	asynchronous reset-direct input (active LOW)
$\overline{SD}$	7	asynchronous set-direct input (active LOW)
V_{CC}	8	supply voltage

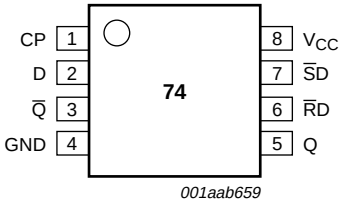
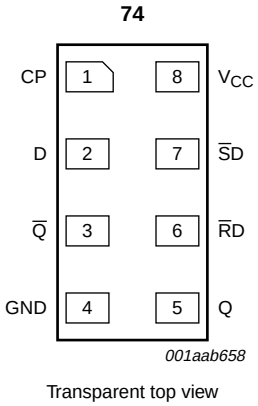


Fig.1 Pin configuration TSSOP8 and VSSOP8.



Transparent top view

Fig.2 Pin configuration XSON8.

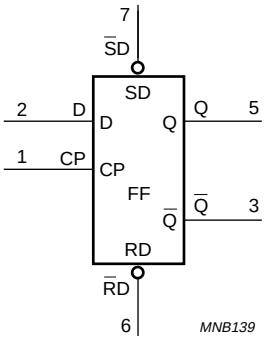


Fig.3 Logic symbol.

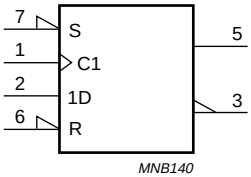


Fig.4 IEC logic symbol.

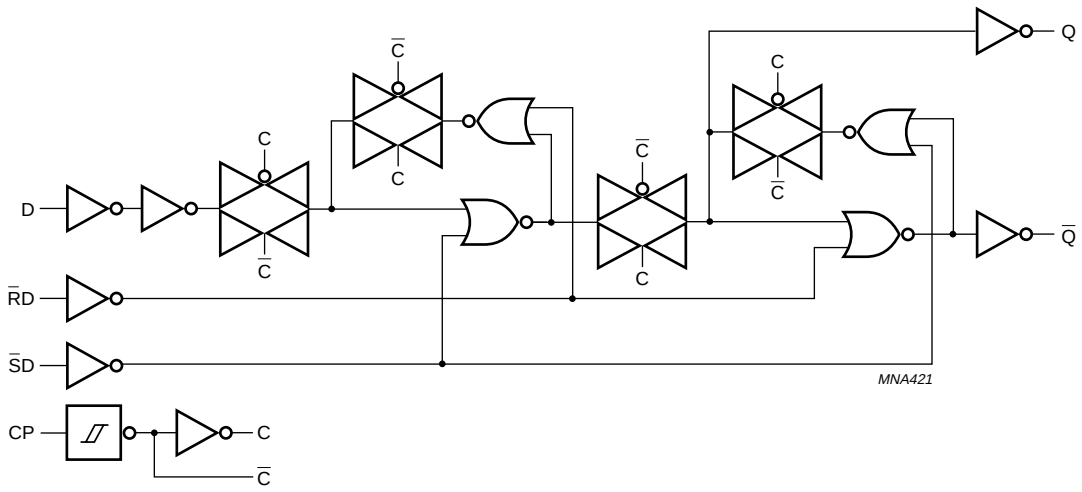


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	active mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	–	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	1.2	1.54	–	V
		I_O = –8 mA	2.3	1.9	2.15	–	V
		I_O = –12 mA	2.7	2.2	2.50	–	V
		I_O = –24 mA	3.0	2.3	2.62	–	V
		I_O = –32 mA	4.5	3.8	4.11	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	-	0.10	V
		I_O = 4 mA	1.65	–	0.07	0.45	V
		I_O = 8 mA	2.3	–	0.12	0.30	V
		I_O = 12 mA	2.7	–	0.17	0.40	V
		I_O = 24 mA	3.0	–	0.33	0.55	V
		I_O = 32 mA	4.5	–	0.39	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	0.95	–	–	V
		I_O = –8 mA	2.3	1.7	–	–	V
		I_O = –12 mA	2.7	1.9	–	–	V
		I_O = –24 mA	3.0	2.0	–	–	V
		I_O = –32 mA	4.5	3.4	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.10	V
		I_O = 4 mA	1.65	–	–	0.70	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±20	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	–	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0	2.3 to 5.5	–	–	5000	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay CP to Q, $\overline{Q}$	see Figs 6 and 8	1.65 to 1.95	1.5	6.0	13.4	ns
			2.3 to 2.7	1.0	3.5	7.1	ns
			2.7	1.0	3.5	7.1	ns
			3.0 to 3.6	1.0	3.5(2)	5.9	ns
			4.5 to 5.5	1.0	2.5	4.1	ns
	propagation delay $\overline{SD}$ to Q, $\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.5	6.0	12.9	ns
			2.3 to 2.7	1.0	3.5	7.0	ns
			2.7	1.0	3.5	7.0	ns
			3.0 to 3.6	1.0	3.0(2)	5.9	ns
			4.5 to 5.5	1.0	2.5	4.1	ns
	propagation delay $\overline{RD}$ to Q, $\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.5	5.0	12.9	ns
			2.3 to 2.7	1.0	3.5	7.0	ns
			2.7	1.0	3.5	7.0	ns
			3.0 to 3.6	1.0	3.0(2)	5.9	ns
			4.5 to 5.5	1.0	2.5	4.1	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8	1.65 to 1.95	6.2	–	–	ns
			2.3 to 2.7	2.7	–	–	ns
			2.7	2.7	–	–	ns
			3.0 to 3.6	2.7	1.3(2)	–	ns
			4.5 to 5.5	2.0	–	–	ns
	set or reset pulse width LOW	see Figs 7 and 8	1.65 to 1.95	6.2	–	–	ns
			2.3 to 2.7	2.7	–	–	ns
			2.7	2.7	–	–	ns
			3.0 to 3.6	2.7	1.6(2)	–	ns
			4.5 to 5.5	2.0	–	–	ns
t_{rem}	removal time set or reset	see Figs 7 and 8	1.65 to 1.95	1.9	–	–	ns
			2.3 to 2.7	1.4	–	–	ns
			2.7	1.3	–	–	ns
			3.0 to 3.6	1.2	–3.0(2)	–	ns
			4.5 to 5.5	1.0	–	–	ns
t_{su}	set-up time D to CP	see Figs 6 and 8	1.65 to 1.95	2.9	–	–	ns
			2.3 to 2.7	1.7	–	–	ns
			2.7	1.7	–	–	ns
			3.0 to 3.6	1.3	0.5(2)	–	ns
			4.5 to 5.5	1.1	–	–	ns

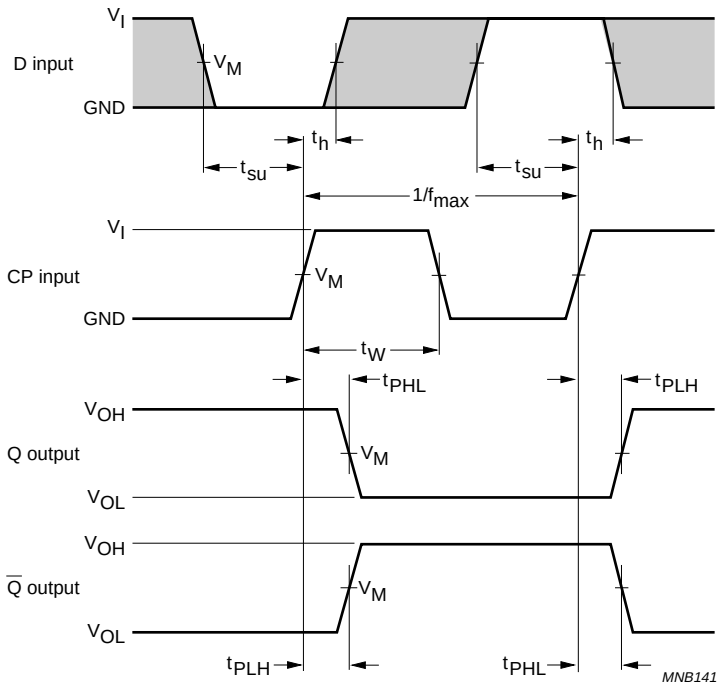
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_h	hold time D to CP	see Figs 6 and 8	1.65 to 1.95	0.0	–	–	ns
			2.3 to 2.7	0.3	–	–	ns
			2.7	0.5	–	–	ns
			3.0 to 3.6	1.2	0.6[2]	–	ns
			4.5 to 5.5	0.5	–	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8	1.65 to 1.95	80	–	–	MHz
			2.3 to 2.7	175	–	–	MHz
			2.7	175	–	–	MHz
			3.0 to 3.6	175	280[2]	–	MHz
			4.5 to 5.5	200	–	–	MHz
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay CP to Q, $\overline{Q}$	see Figs 6 and 8	1.65 to 1.95	1.5	–	13.4	ns
			2.3 to 2.7	1.0	–	7.1	ns
			2.7	1.0	–	7.1	ns
			3.0 to 3.6	1.0	–	5.9	ns
			4.5 to 5.5	1.0	–	4.1	ns
	propagation delay $\overline{S}$D to Q, $\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.5	–	12.9	ns
			2.3 to 2.7	1.0	–	7.0	ns
			2.7	1.0	–	7.0	ns
			3.0 to 3.6	1.0	–	5.9	ns
			4.5 to 5.5	1.0	–	4.1	ns
	propagation delay $\overline{R}$D to Q, $\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.5	–	12.9	ns
			2.3 to 2.7	1.0	–	7.0	ns
			2.7	1.0	–	7.0	ns
			3.0 to 3.6	1.0	–	5.9	ns
			4.5 to 5.5	1.0	–	4.1	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8	1.65 to 1.95	6.2	–	–	ns
			2.3 to 2.7	2.7	–	–	ns
			2.7	2.7	–	–	ns
			3.0 to 3.6	2.7	–	–	ns
			4.5 to 5.5	2.0	–	–	ns
	set or reset pulse width LOW	see Figs 7 and 8	1.65 to 1.95	6.2	–	–	ns
			2.3 to 2.7	2.7	–	–	ns
			2.7	2.7	–	–	ns
			3.0 to 3.6	2.7	–	–	ns
			4.5 to 5.5	2.0	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_{rem}	removal time set or reset	see Figs 7 and 8	1.65 to 1.95	1.9	–	–	ns
			2.3 to 2.7	1.4	–	–	ns
			2.7	1.3	–	–	ns
			3.0 to 3.6	1.2	–	–	ns
			4.5 to 5.5	1.0	–	–	ns
t_{su}	set-up time D to CP	see Figs 6 and 8	1.65 to 1.95	2.9	–	–	ns
			2.3 to 2.7	1.7	–	–	ns
			2.7	1.7	–	–	ns
			3.0 to 3.6	1.3	–	–	ns
			4.5 to 5.5	1.1	–	–	ns
t_h	hold time D to CP	see Figs 6 and 8	1.65 to 1.95	0.0	–	–	ns
			2.3 to 2.7	0.3	–	–	ns
			2.7	0.5	–	–	ns
			3.0 to 3.6	1.2	–	–	ns
			4.5 to 5.5	0.5	–	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8	1.65 to 1.95	80	–	–	MHz
			2.3 to 2.7	175	–	–	MHz
			2.7	175	–	–	MHz
			3.0 to 3.6	175	–	–	MHz
			4.5 to 5.5	200	–	–	MHz

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

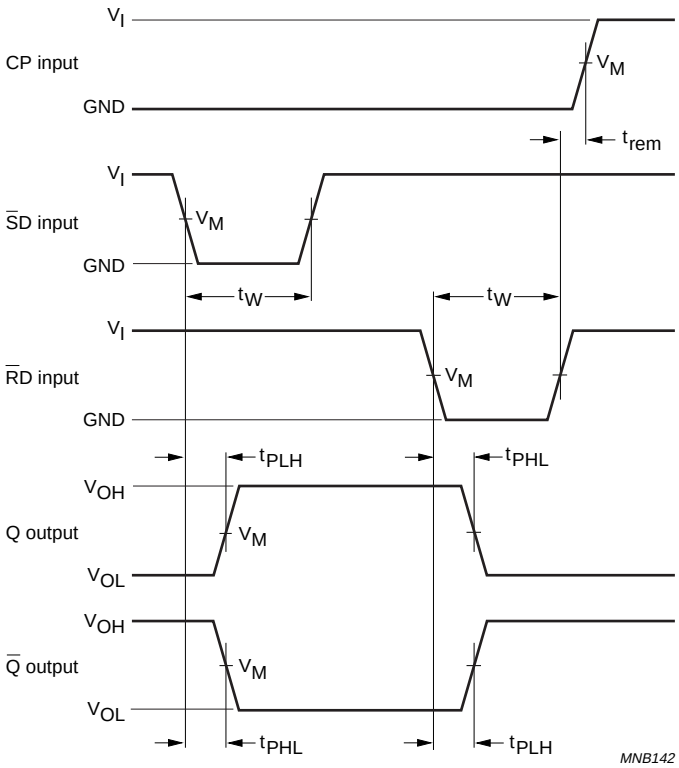


The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

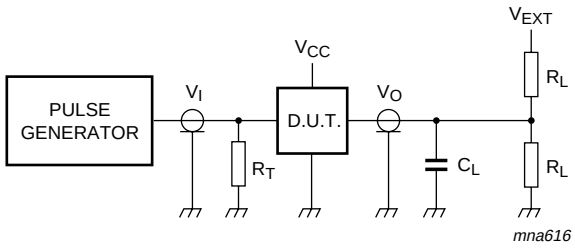
Fig.6 The clock input (CP) to output (Q, $\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum clock pulse frequency.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 The set ($\overline{S}D$) and reset ($\overline{R}D$) input to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{R}D$ to CP removal time.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Definitions for test circuit:

R_L = Load resistor.

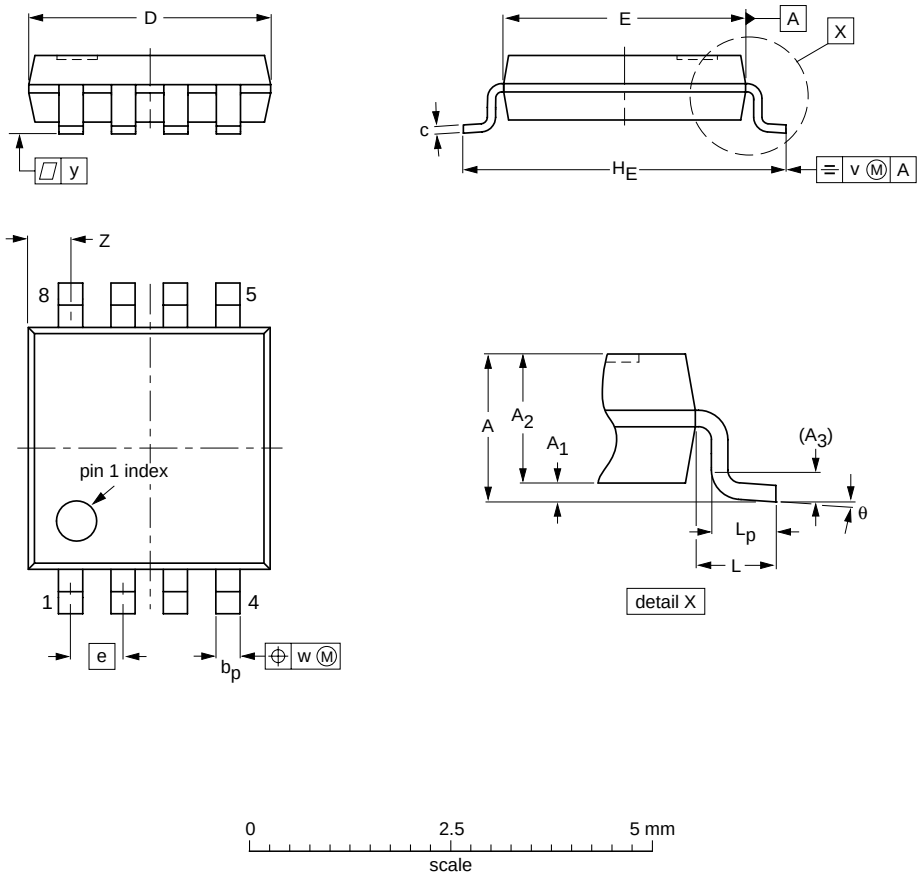
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

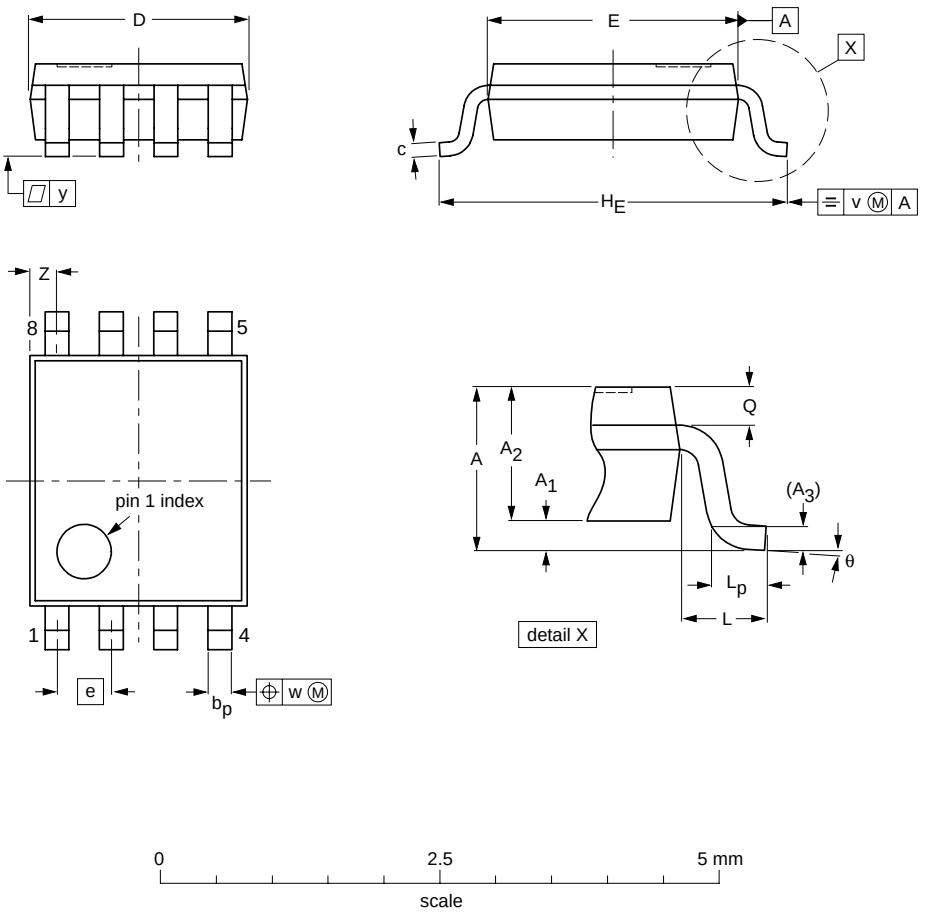
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



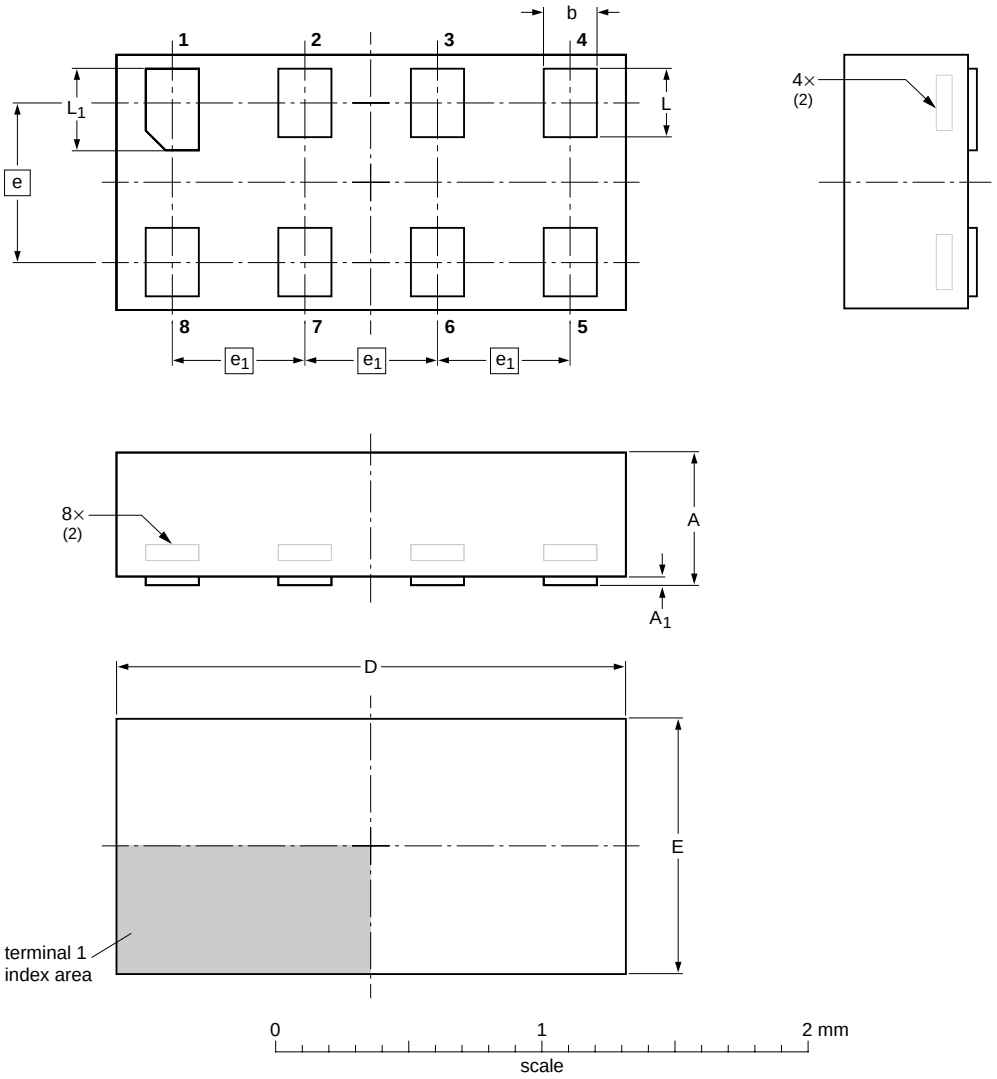
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~04-07-22~~ 04-11-09

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LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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