74HC590

8-bit binary counter with output register; 3-state

Rev. 01 — 30 March 2005 Product data sheet

1. General description

The 74HC590 is a high-speed Si-gate CMOS device and is pin compatible with Low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC590 is an 8-bit binary counter with a storage register and 3-state outputs. The storage register has parallel (Q0 to Q7) outputs. The binary counter features a master reset counter ($\overline{MRC}$) and count enable ($\overline{CE}$) inputs. The counter and storage register have separate positive edge triggered clock (CPC and CPR) inputs. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable. A ripple carry output ($\overline{RCO}$) is provided for cascading. Cascading is accomplished by connecting $\overline{RCO}$ of the first stage to $\overline{CE}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to the counter clock (CPC) input of the following stage. If both clocks are connected together, the counter state always is one count ahead of the register.

2. Features

- Counter and register have independent clock inputs
- Counter has master reset
- Complies with JEDEC standard no. 7A
- Multiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 2000 V
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CPC to $\overline{RCO}$	C_L = 50 pF; V_{CC} = 4.5 V	-	19	-	ns
	propagation delay CPR to Qn	C_L = 50 pF; V_{CC} = 4.5 V	-	17	-	ns
t_{PLH}	propagation delay $\overline{MRC}$ to RCO	C_L = 50 pF; V_{CC} = 4.5 V	-	18	-	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	C_L = 50 pF; V_{CC} = 4.5 V	-	13	-	ns

PHILIPS

Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	C_L = 50 pF; V_{CC} = 4.5 V		-	13	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance		[1] [2]	-	44	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC590D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC590PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC590BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

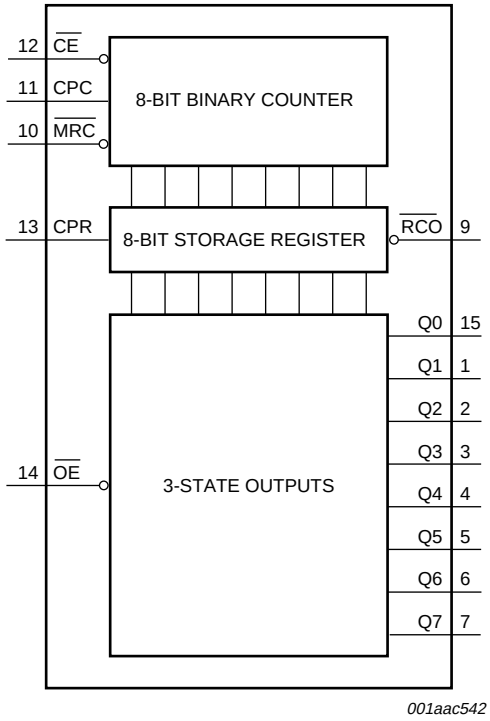


Fig 1. Functional diagram

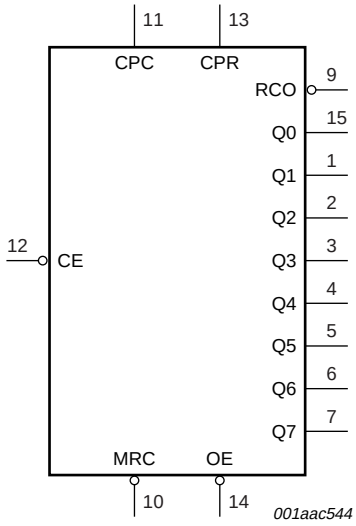


Fig 2. Logic symbol

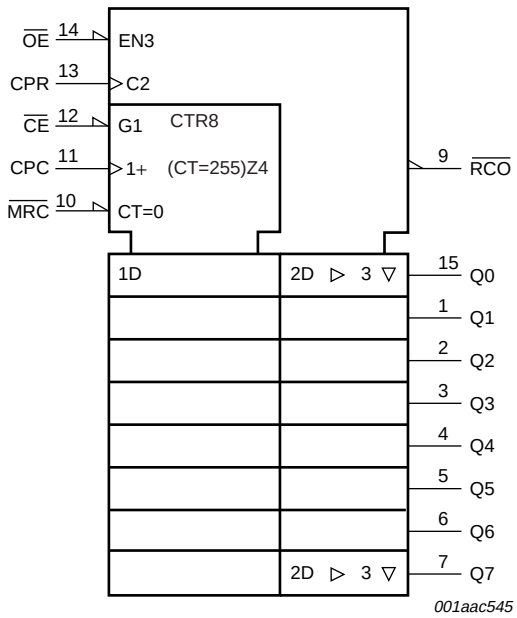


Fig 3. IEC logic symbol

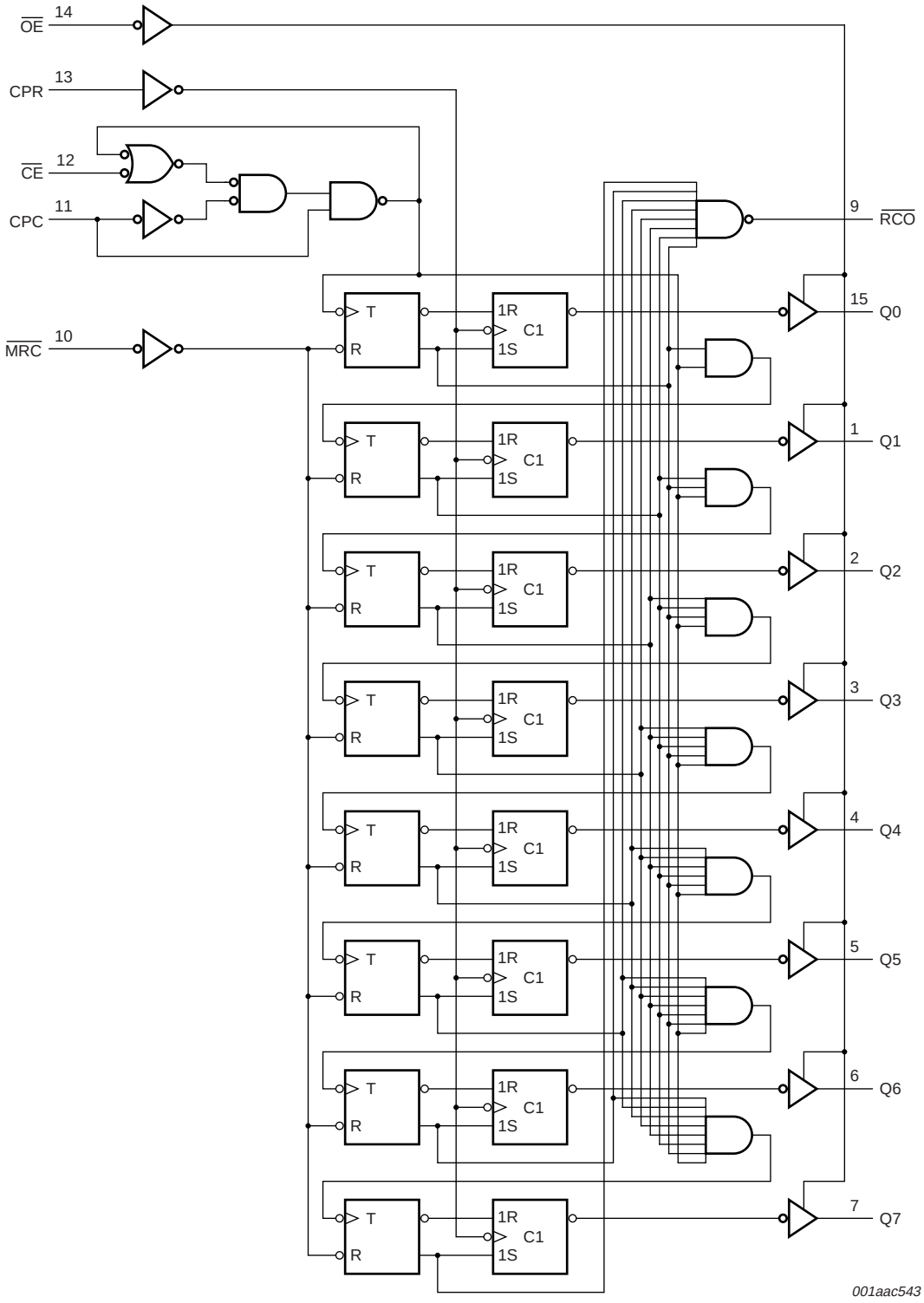


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

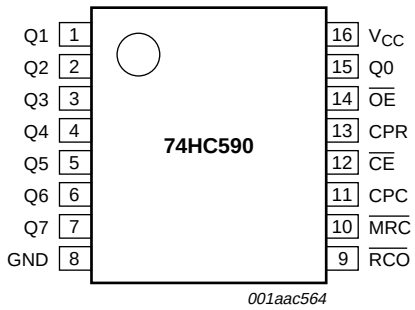
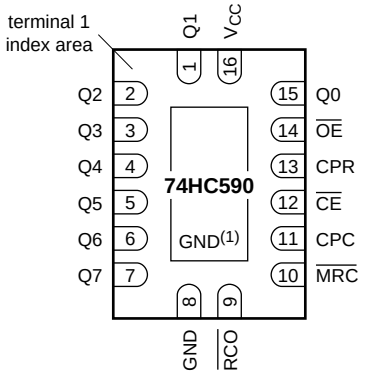


Fig 5. Pin configuration SO16 and TSSOP16



(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Q1	1	parallel data output 1
Q2	2	parallel data output 2
Q3	3	parallel data output 3
Q4	4	parallel data output 4
Q5	5	parallel data output 5
Q6	6	parallel data output 6
Q7	7	parallel data output 7
GND	8	ground (0 V)
$\overline{RCO}$	9	ripple carry output (active LOW)
$\overline{MRC}$	10	master reset counter input (active LOW)
CPC	11	counter clock input (active HIGH)
$\overline{CE}$	12	count enable input (active LOW)
CPR	13	register clock input (active HIGH)
$\overline{OE}$	14	output enable input (active LOW)
Q0	15	parallel data output 0
V_{CC}	16	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1] [2]

Inputs					Description
$\overline{OE}$	CPR	$\overline{MRC}$	$\overline{CE}$	CPC	
H	X	X	X	X	Q outputs disable
L	X	X	X	X	Q outputs enable
X	↑	X	X	X	counter data stored into register
X	↓	X	X	X	register stage is not changed
X	X	L	X	X	counter clear
X	X	H	L	↑	advance one count
X	X	H	L	↓	no count
X	X	H	H	X	no count

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

[2] $\overline{RCO} = \overline{Q0' \cdot Q1' \cdot Q2' \cdot Q3' \cdot Q4' \cdot Q5' \cdot Q6' \cdot Q7'}$ (Q0' to Q7' are internal outputs of the counter)

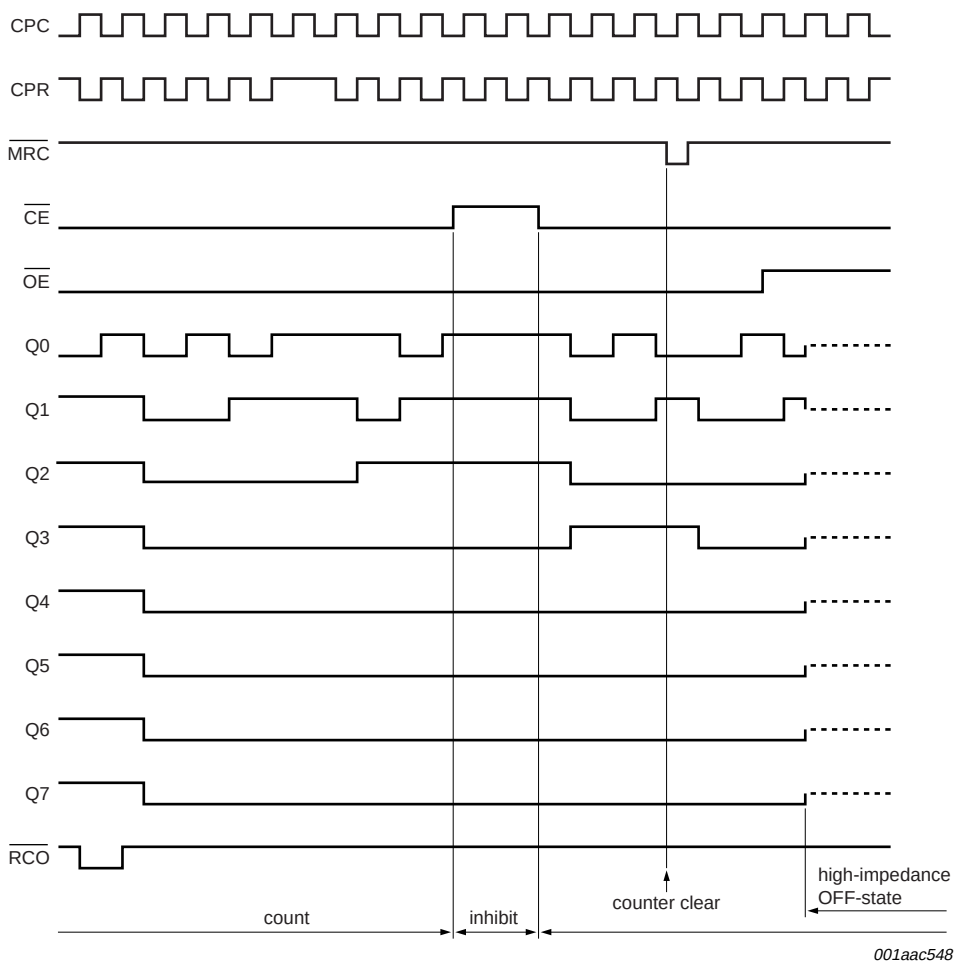


Fig 7. Typical timing sequence

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	source or sink output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V			
	$\overline{RCO}$ standard output		-	±25	mA
	Qn bus driver output		-	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±70	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SO16 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 packages: P_{tot} derates linearly with 8 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
	all outputs	I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
	$\overline{RCO}$ standard output	I_O = –4 mA; V_{CC} = 4.5 V	4.18	4.31	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.68	5.80	-	V
	Qn bus driver output	I_O = –6 mA; V_{CC} = 4.5 V	4.18	4.31	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.68	5.80	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
	all outputs	I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
	$\overline{RCO}$ standard output	I_O = 4 mA; V_{CC} = 4.5 V	-	0.17	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.18	0.26	V
	Qn bus driver output	I_O = 6 mA; V_{CC} = 4.5 V	-	0.17	0.26	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.18	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.5	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	4.0	µA
C_I	input capacitance		-	3.5	-	pF

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
	all outputs	I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
	$\overline{RCO}$ standard output	I_O = −4 mA; V_{CC} = 4.5 V	4.13	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.63	-	-	V
	Qn bus driver output	I_O = −6 mA; V_{CC} = 4.5 V	4.13	-	-	V
		I_O = −7.8 mA; V_{CC} = 6.0 V	5.63	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
	all outputs	I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
	$\overline{RCO}$ standard output	I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
	Qn bus driver output	I_O = 6 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	40	μA

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = = V_{IH} or V_{IL}				
	all outputs	I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
	$\overline{RCO}$ standard output	I_O = −4 mA; V_{CC} = 4.5 V	4.1	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.6	-	-	V
	Qn bus driver output	I_O = −6 mA; V_{CC} = 4.5 V	4.1	-	-	V
		I_O = −7.8 mA; V_{CC} = 6.0 V	5.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = = V_{IH} or V_{IL}				
	all outputs	I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
	$\overline{RCO}$ standard output	I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
	Qn bus driver output	I_O = 6 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	μA

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CPC to $\overline{RCO}$	see Figure 8				
		V_{CC} = 2.0 V	-	52	150	ns
		V_{CC} = 4.5 V	-	19	30	ns
		V_{CC} = 6.0 V	-	15	26	ns
	propagation delay CPR to Qn	see Figure 9				
		V_{CC} = 2.0 V	-	50	140	ns
		V_{CC} = 4.5 V	-	17	28	ns
		V_{CC} = 6.0 V	-	14	24	ns
t_{PLH}	propagation delay $\overline{MRC}$ to $\overline{RCO}$	see Figure 10				
		V_{CC} = 2.0 V	-	53	130	ns
		V_{CC} = 4.5 V	-	18	26	ns
		V_{CC} = 6.0 V	-	14	22	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figure 11				
		V_{CC} = 2.0 V	-	28	105	ns
		V_{CC} = 4.5 V	-	13	21	ns
		V_{CC} = 6.0 V	-	11	18	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Figure 11				
		V_{CC} = 2.0 V	-	28	105	ns
		V_{CC} = 4.5 V	-	13	21	ns
		V_{CC} = 6.0 V	-	11	18	ns
t_W	CPC and CPR clock pulse width HIGH or LOW	see Figure 8 and Figure 9				
		V_{CC} = 2.0 V	100	24	-	ns
		V_{CC} = 4.5 V	20	9	-	ns
		V_{CC} = 6.0 V	17	8	-	ns
	$\overline{MRC}$ reset pulse width LOW	see Figure 10				
		V_{CC} = 2.0 V	75	28	-	ns
		V_{CC} = 4.5 V	15	8	-	ns
		V_{CC} = 6.0 V	13	6	-	ns
t_{su}	set-up time CPC to CPR	see Figure 13				
		V_{CC} = 2.0 V	100	46	-	ns
		V_{CC} = 4.5 V	20	14	-	ns
		V_{CC} = 6.0 V	17	10	-	ns
	set-up time $\overline{CE}$ to CPC	see Figure 12				
		V_{CC} = 2.0 V	100	44	-	ns
		V_{CC} = 4.5 V	20	11	-	ns
		V_{CC} = 6.0 V	17	9	-	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 14.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time $\overline{CE}$ to CPC	see Figure 12					
		V_{CC} = 2.0 V		0	-	-	ns
		V_{CC} = 4.5 V		0	-	-	ns
		V_{CC} = 6.0 V		0	-	-	ns
t_{rem}	removal time $\overline{MRC}$ to CPC	see Figure 10					
		V_{CC} = 2.0 V		75	28	-	ns
		V_{CC} = 4.5 V		15	7	-	ns
		V_{CC} = 6.0 V		13	6	-	ns
f_{max}	maximum clock pulse frequency CPC or CPR	see Figure 8 and Figure 9					
		V_{CC} = 2.0 V		6.6	16	-	MHz
		V_{CC} = 4.5 V		33	52	-	MHz
		V_{CC} = 6.0 V		39	61	-	MHz
C_{PD}	power dissipation capacitance		[1] [2]	-	44	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay CPC to $\overline{RCO}$	see Figure 8					
		V_{CC} = 2.0 V		-	-	190	ns
		V_{CC} = 4.5 V		-	-	38	ns
		V_{CC} = 6.0 V		-	-	33	ns
	propagation delay CPR to Qn	see Figure 9					
		V_{CC} = 2.0 V		-	-	175	ns
		V_{CC} = 4.5 V		-	-	35	ns
		V_{CC} = 6.0 V		-	-	30	ns
t_{PLH}	propagation delay $\overline{MRC}$ to $\overline{RCO}$	see Figure 10					
		V_{CC} = 2.0 V		-	-	165	ns
		V_{CC} = 4.5 V		-	-	33	ns
		V_{CC} = 6.0 V		-	-	28	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figure 11					
		V_{CC} = 2.0 V		-	-	130	ns
		V_{CC} = 4.5 V		-	-	26	ns
		V_{CC} = 6.0 V		-	-	22	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Figure 11					
		V_{CC} = 2.0 V		-	-	130	ns
		V_{CC} = 4.5 V		-	-	26	ns
		V_{CC} = 6.0 V		-	-	22	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	CPC and CPR clock pulse width HIGH or LOW	see Figure 8 and Figure 9				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
	$\overline{MRC}$ reset pulse width LOW	see Figure 10				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
t_{su}	set-up time CPC to CPR	see Figure 13				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
	set-up time $\overline{CE}$ to CPC	see Figure 12				
		V_{CC} = 2.0 V	125	-	-	ns
		V_{CC} = 4.5 V	25	-	-	ns
		V_{CC} = 6.0 V	21	-	-	ns
t_h	hold time $\overline{CE}$ to CPC	see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
t_{rem}	removal time $\overline{MRC}$ to CPC	see Figure 10				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
f_{max}	maximum clock pulse frequency CPC or CPR	see Figure 8 and Figure 9				
		V_{CC} = 2.0 V	5.2	-	-	MHz
		V_{CC} = 4.5 V	26	-	-	MHz
		V_{CC} = 6.0 V	31	-	-	MHz

Table 8: Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CPC to $\overline{RCO}$	see Figure 8				
		V_{CC} = 2.0 V	-	-	230	ns
		V_{CC} = 4.5 V	-	-	45	ns
		V_{CC} = 6.0 V	-	-	40	ns
	propagation delay CPR to Qn	see Figure 9				
		V_{CC} = 2.0 V	-	-	210	ns
		V_{CC} = 4.5 V	-	-	42	ns
		V_{CC} = 6.0 V	-	-	36	ns
t_{PLH}	propagation delay $\overline{MRC}$ to $\overline{RCO}$	see Figure 10				
		V_{CC} = 2.0 V	-	-	200	ns
		V_{CC} = 4.5 V	-	-	40	ns
		V_{CC} = 6.0 V	-	-	34	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figure 11				
		V_{CC} = 2.0 V	-	-	160	ns
		V_{CC} = 4.5 V	-	-	32	ns
		V_{CC} = 6.0 V	-	-	27	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Figure 11				
		V_{CC} = 2.0 V	-	-	160	ns
		V_{CC} = 4.5 V	-	-	32	ns
		V_{CC} = 6.0 V	-	-	27	ns
t_W	CPC and CPR clock pulse width HIGH or LOW	see Figure 8 and Figure 9				
		V_{CC} = 2.0 V	145	-	-	ns
		V_{CC} = 4.5 V	29	-	-	ns
		V_{CC} = 6.0 V	25	-	-	ns
	$\overline{MRC}$ reset pulse width LOW	see Figure 10				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
t_{su}	set-up time CPC to CPR	see Figure 13				
		V_{CC} = 2.0 V	150	-	-	ns
		V_{CC} = 4.5 V	30	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns
	set-up time $\overline{CE}$ to CPC	see Figure 12				
		V_{CC} = 2.0 V	150	-	-	ns
		V_{CC} = 4.5 V	30	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns

Table 8: Dynamic characteristics *…continued*

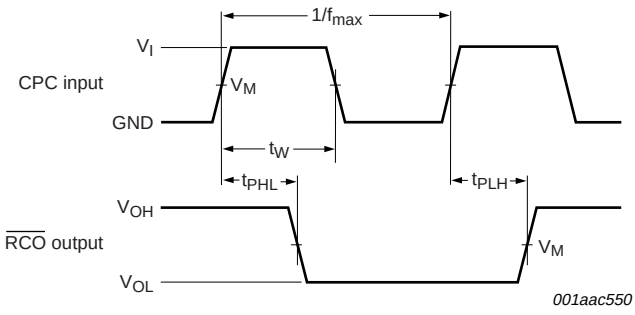
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified; see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_h	hold time $\overline{CE}$ to CPC	see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
t_{rem}	removal time $\overline{MRC}$ to CPC	see Figure 10				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
f_{max}	maximum clock pulse frequency CPC or CPR	see Figure 8 and Figure 9				
		V_{CC} = 2.0 V	4.4	-	-	MHz
		V_{CC} = 4.5 V	22	-	-	MHz
		V_{CC} = 6.0 V	26	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is V_I = GND to V_{CC}.

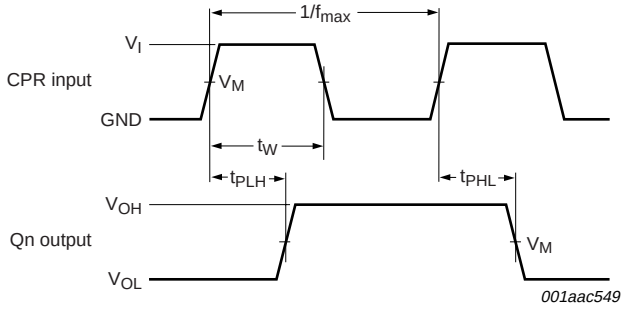
12. Waveforms



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

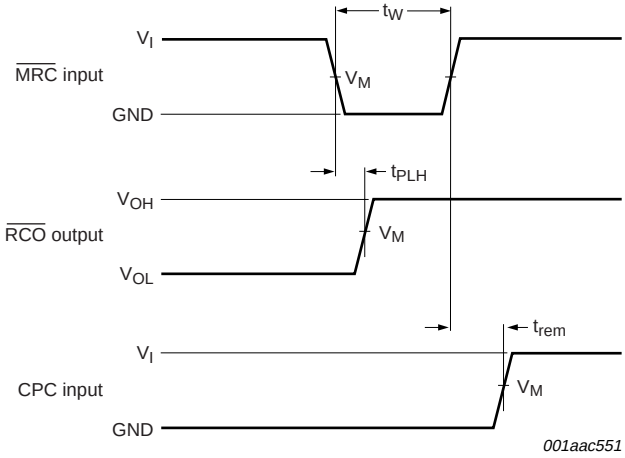
Fig 8. Waveforms showing the propagation delays from the counter clock input (CPC) to ripple carry ($\overline{RCO}$) output and the CPC pulse width



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

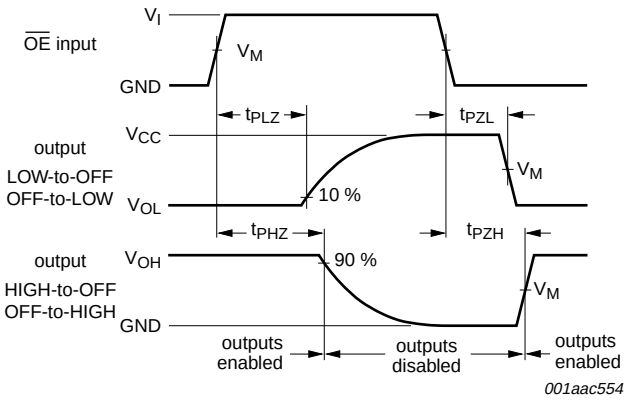
Fig 9. Waveforms showing the propagation delays from the register clock input (CPR) to output (Qn) and the register clock pulse width



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

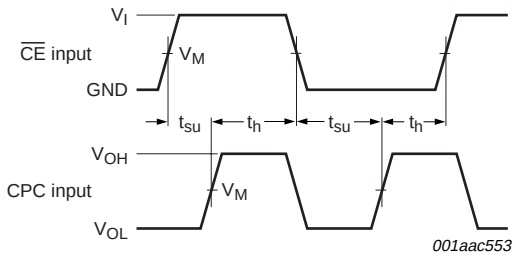
Fig 10. Waveforms showing the propagation delays from the master reset counter input ($\overline{MRC}$) to output ($\overline{RCO}$), the $\overline{MRC}$ pulse width and removal time



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

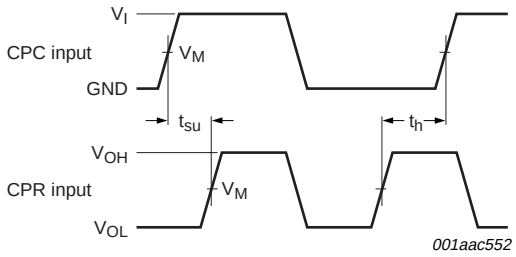
Fig 11. Waveforms showing the 3-state enable and disable times



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

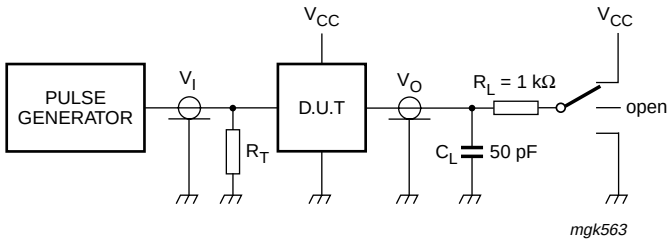
Fig 12. Waveforms showing the set-up and hold times for the count enable input ($\overline{CE}$) to the counter clock input (CPC)



Measurement points: $V_M = 0.5 \times V_I$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 13. Waveforms showing the set-up and hold times for the counter clock input (CPC) to the register clock input (CPR)



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

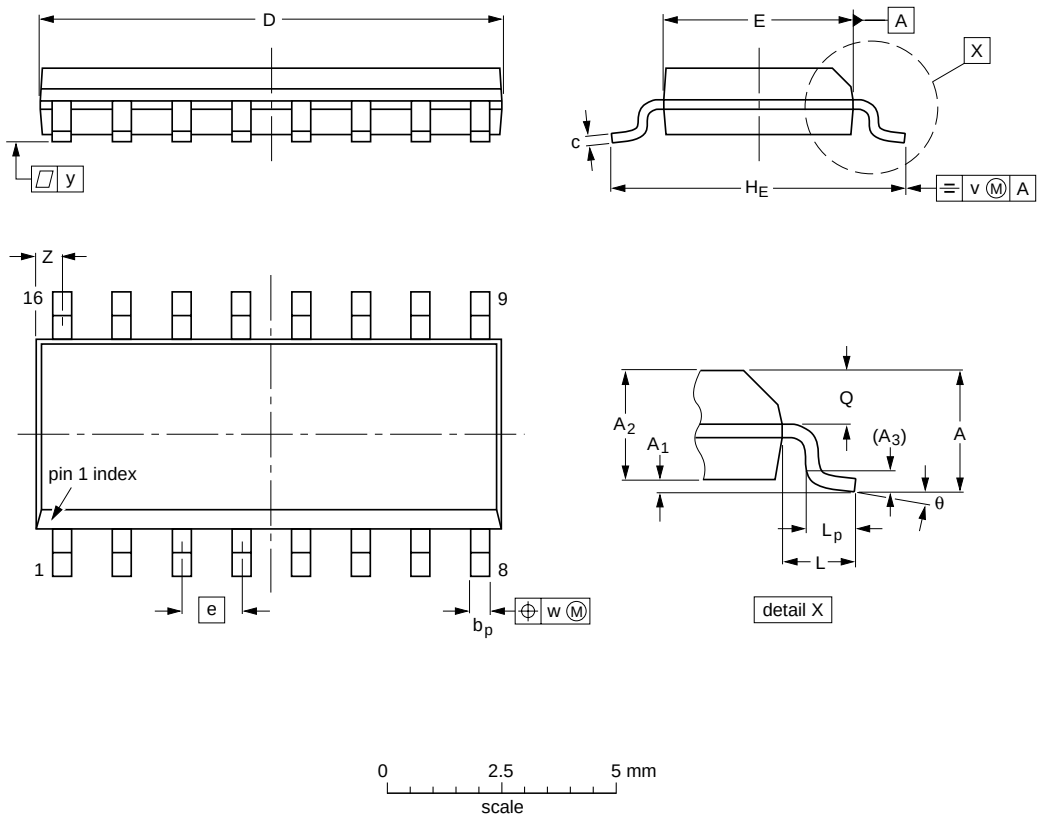
Fig 14. Load circuitry for switching times

Table 9: Test data

Supply voltage	Input		Load		Switch position		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}
2.0 V to 6.0 V	V_{CC}	6 ns	50 pF	1 kΩ	open	V_{CC}	GND

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

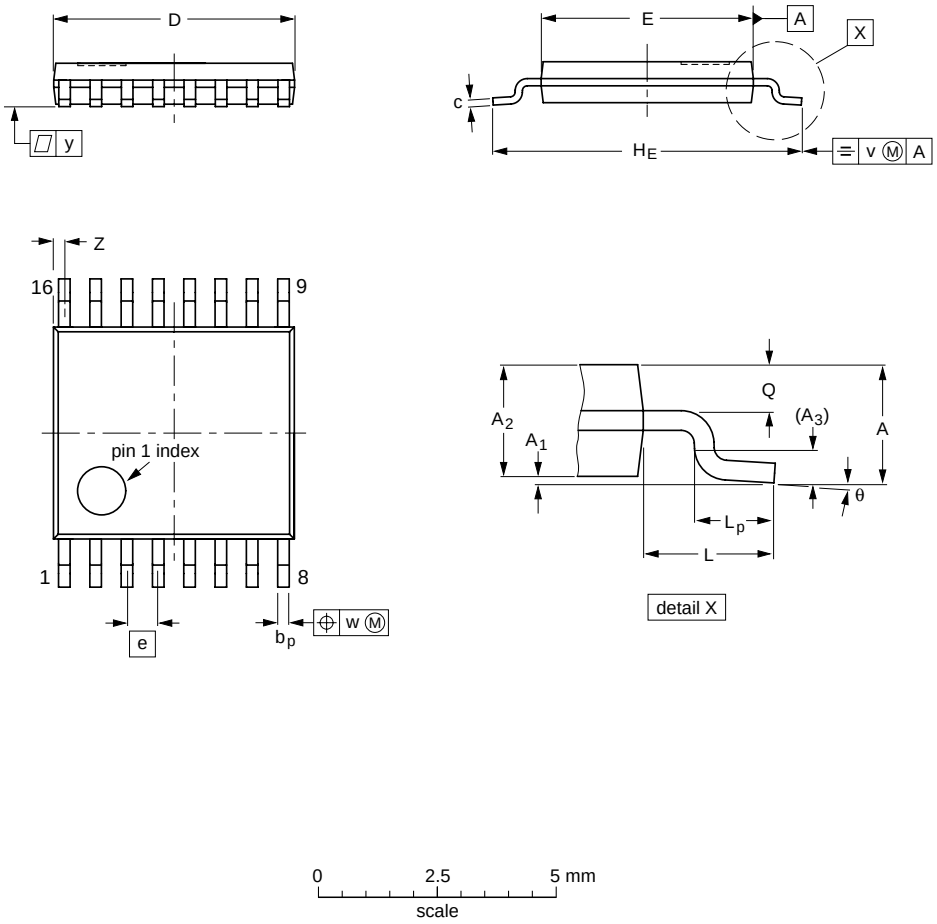
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

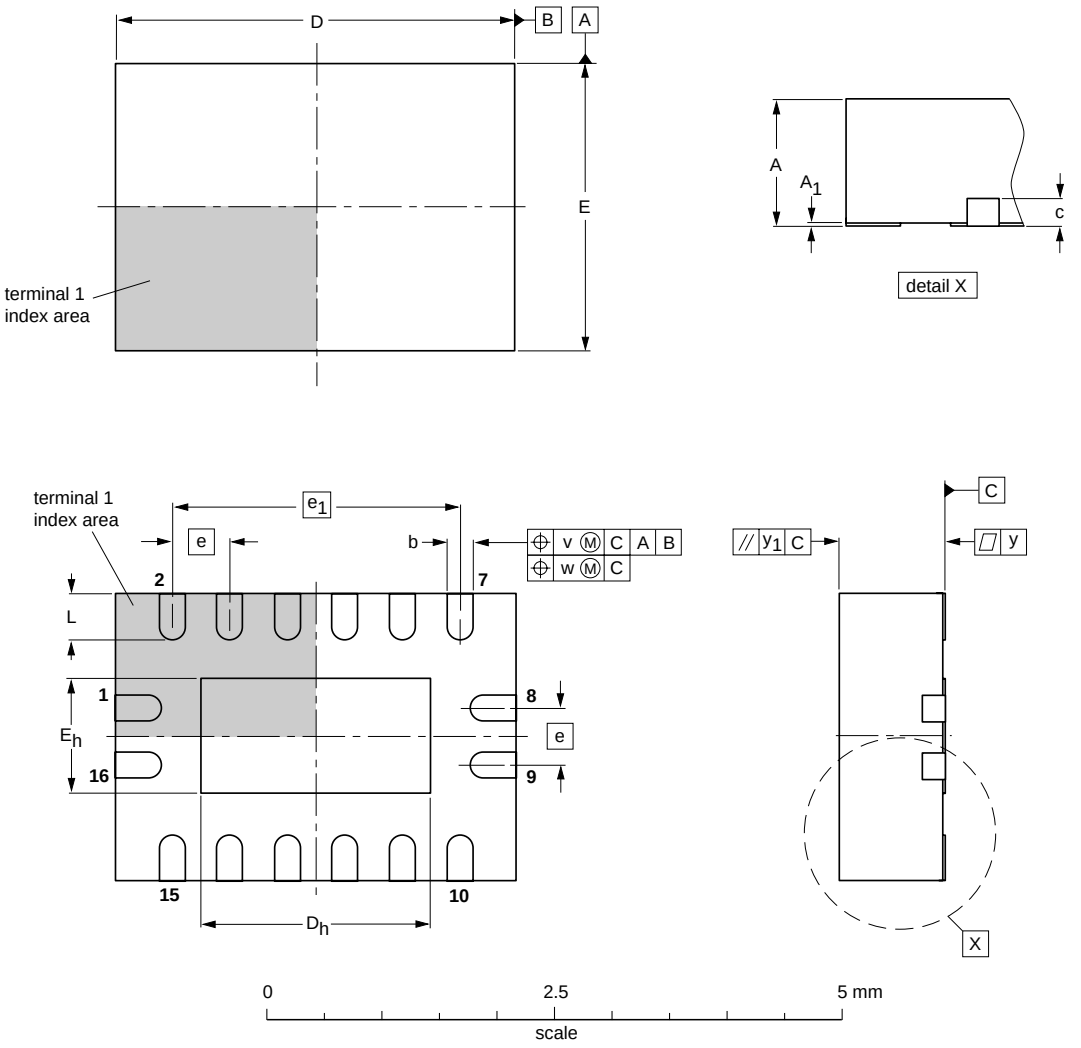
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 17. Package outline SOT763-1 (DHVQFN16)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC590_1	20050330	Product data sheet	-	9397 750 14691	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

17. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

Date of release: 30 March 2005
Document number: 9397 750 14691

Published in The Netherlands