

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4017

Johnson decade counter with 10
decoded outputs

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT4017

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the “4017” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q₀ to Q₉), an active LOW output from the most significant flip-flop (\overline{Q}_{5-9}), active HIGH and active LOW clock inputs (CP₀ and

\overline{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP₀ while \overline{CP}_1 is LOW or a HIGH-to-LOW transition at \overline{CP}_1 while CP₀ is HIGH (see also function table).

When cascading counters, the \overline{Q}_{5-9} output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP₀ input of the next counter.

A HIGH on MR resets the counter to zero (Q₀ = \overline{Q}_{5-9} = HIGH; Q₁ to Q₉ = LOW) independent of the clock inputs (CP₀ and \overline{CP}_1).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP ₀ , \overline{CP}_1 to Q _n	C _L = 15 pF; V _{CC} = 5 V	20	21	ns
f _{max}	maximum clock frequency		77	67	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	35	36	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

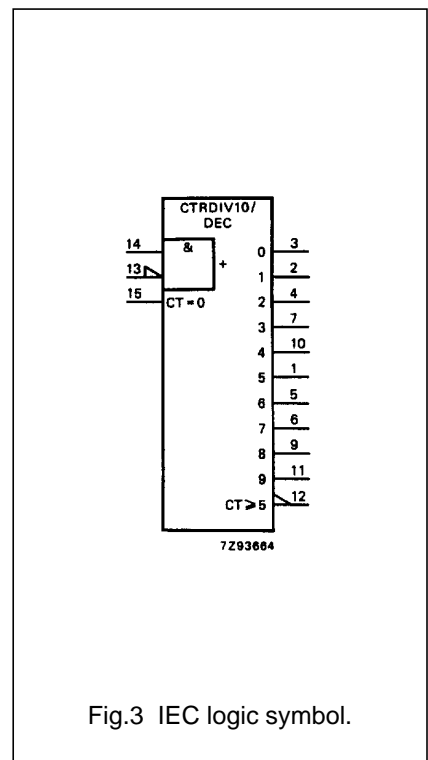
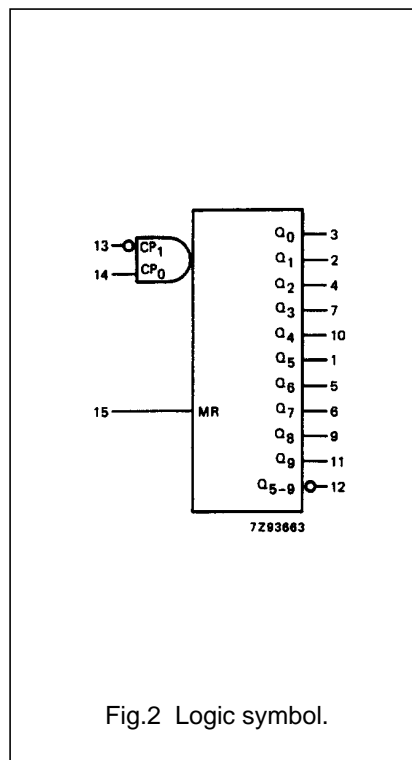
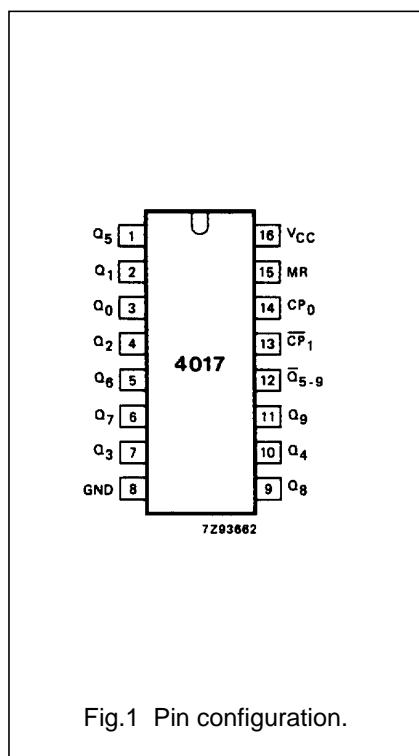
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

Johnson decade counter with 10 decoded outputs

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q ₀ to Q ₉	decoded outputs
8	GND	ground (0 V)
12	\overline{Q}_{5-9}	carry output (active LOW)
13	\overline{CP}_1	clock input (HIGH-to-LOW, edge-triggered)
14	CP ₀	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V _{CC}	positive supply voltage



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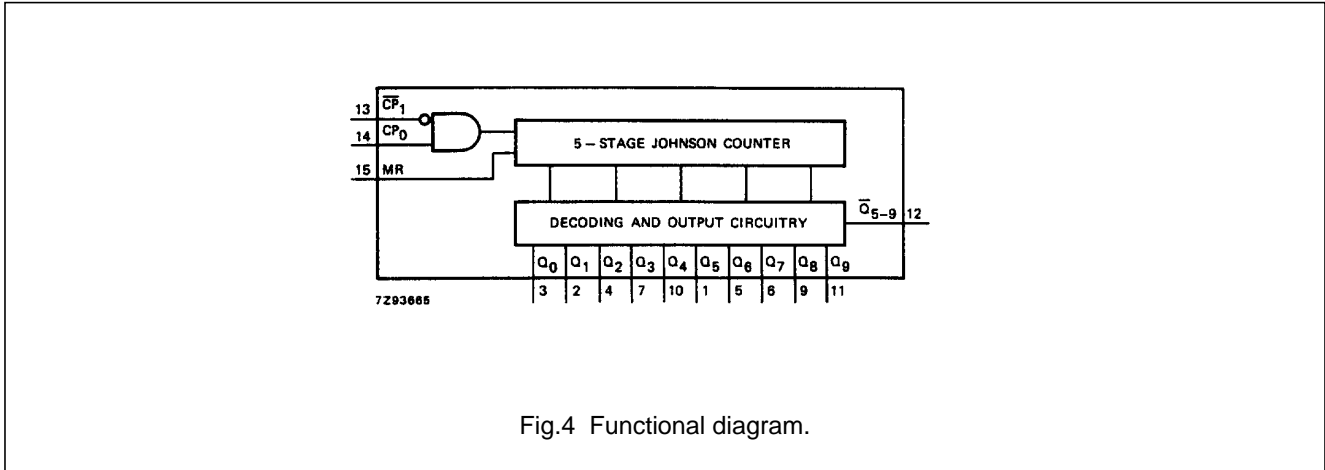


Fig.4 Functional diagram.

FUNCTION TABLE

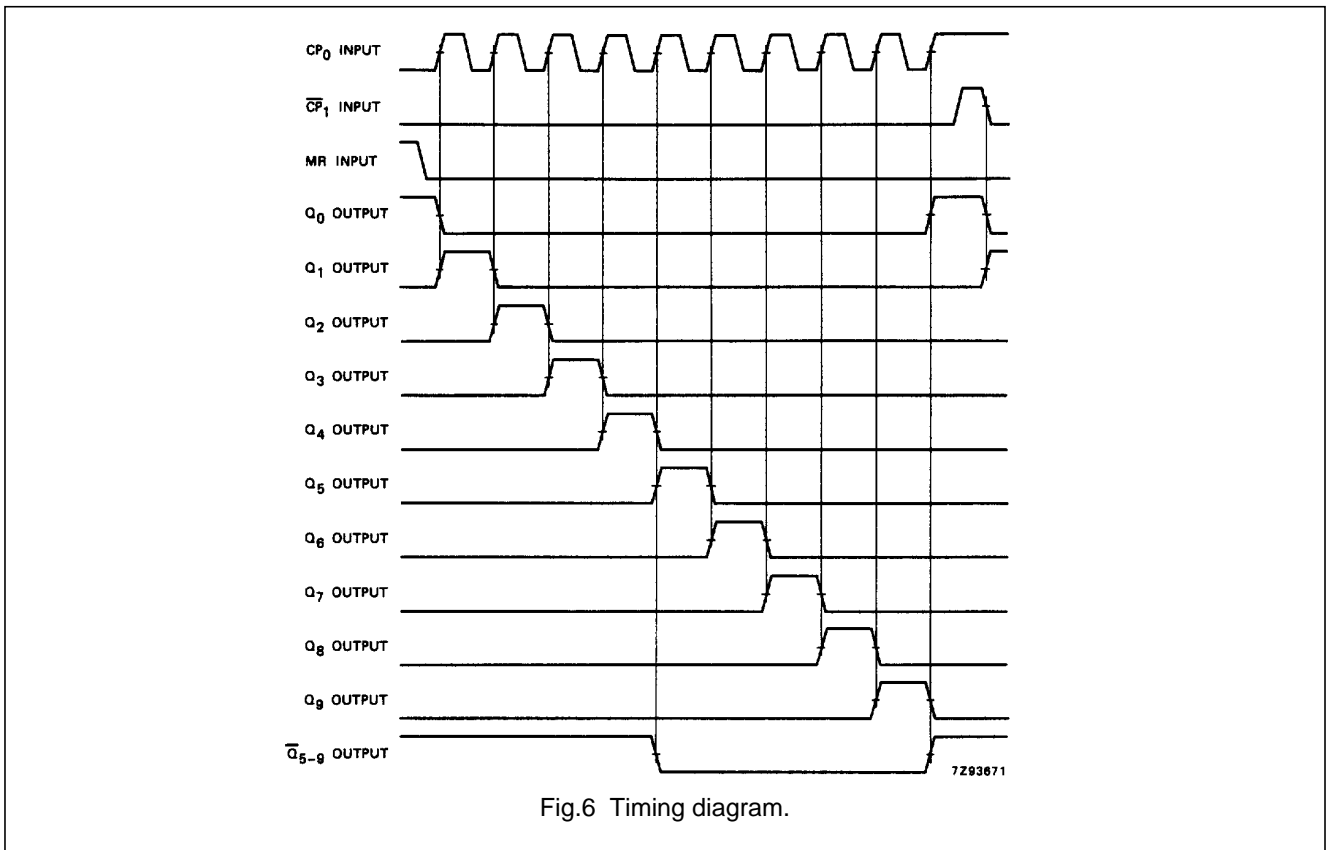
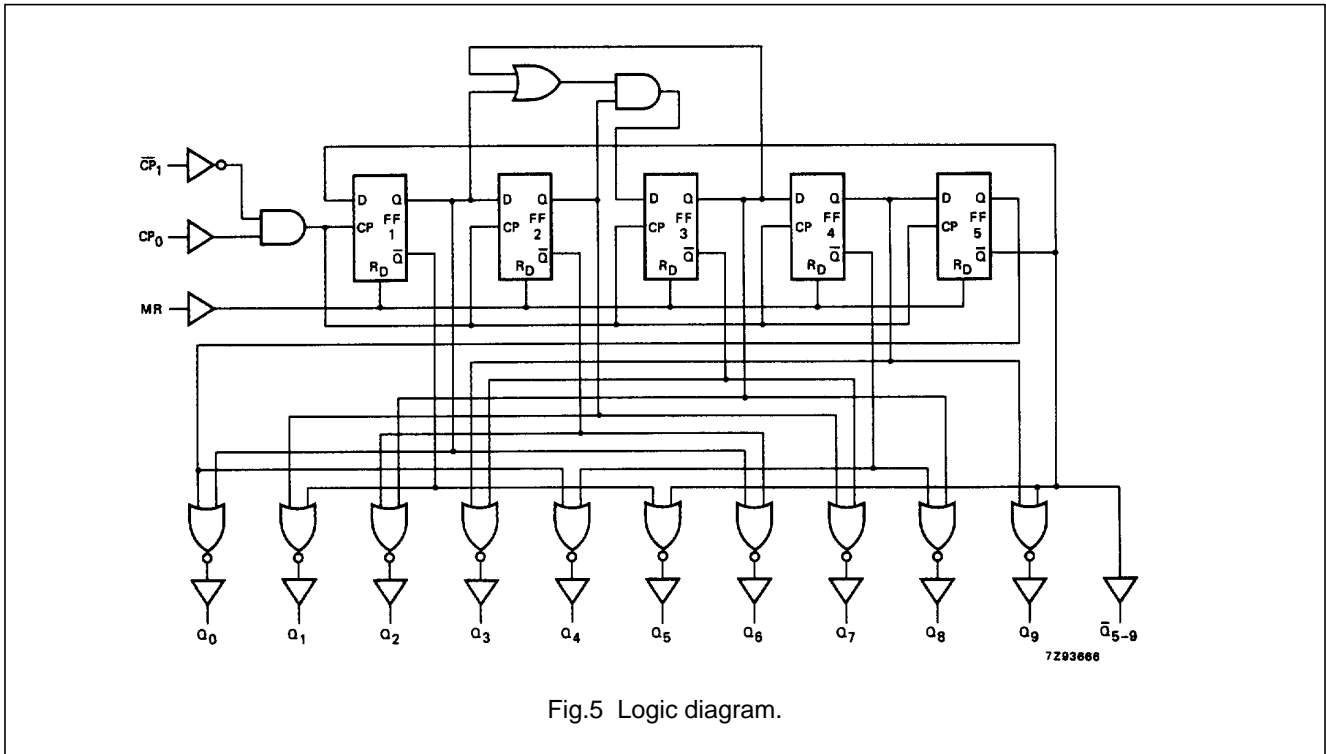
MR	CP ₀	\overline{CP}_1	OPERATION
H	X	X	Q ₀ = Q ₅₋₉ = H; Q ₁ to Q ₉ = L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Notes

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH clock transition
 ↓ = HIGH-to-LOW clock transition

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to+85		-40 to+125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q _n		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q ₅₋₉		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q _n		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₅₋₉		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t _{PHL}	propagation delay MR to Q ₁₋₉		52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8
t _{PLH}	propagation delay MR to Q ₅₋₉ , Q ₀		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t _w	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _w	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{rem}	removal time MR to CP ₀ , CP ₁	5 5 5	-17 -6 -5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time CP ₁ to CP ₀ ; CP ₀ to CP ₁	50 10 9	-8 -3 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
t _h	hold time CP ₀ to CP ₁ ; CP ₁ to CP ₀	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
f _{max}	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.8

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
\overline{CP}_1	0.40
CP ₀	0.25
MR	0.50

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AC CHARACTERISTICS FOR 74HCT

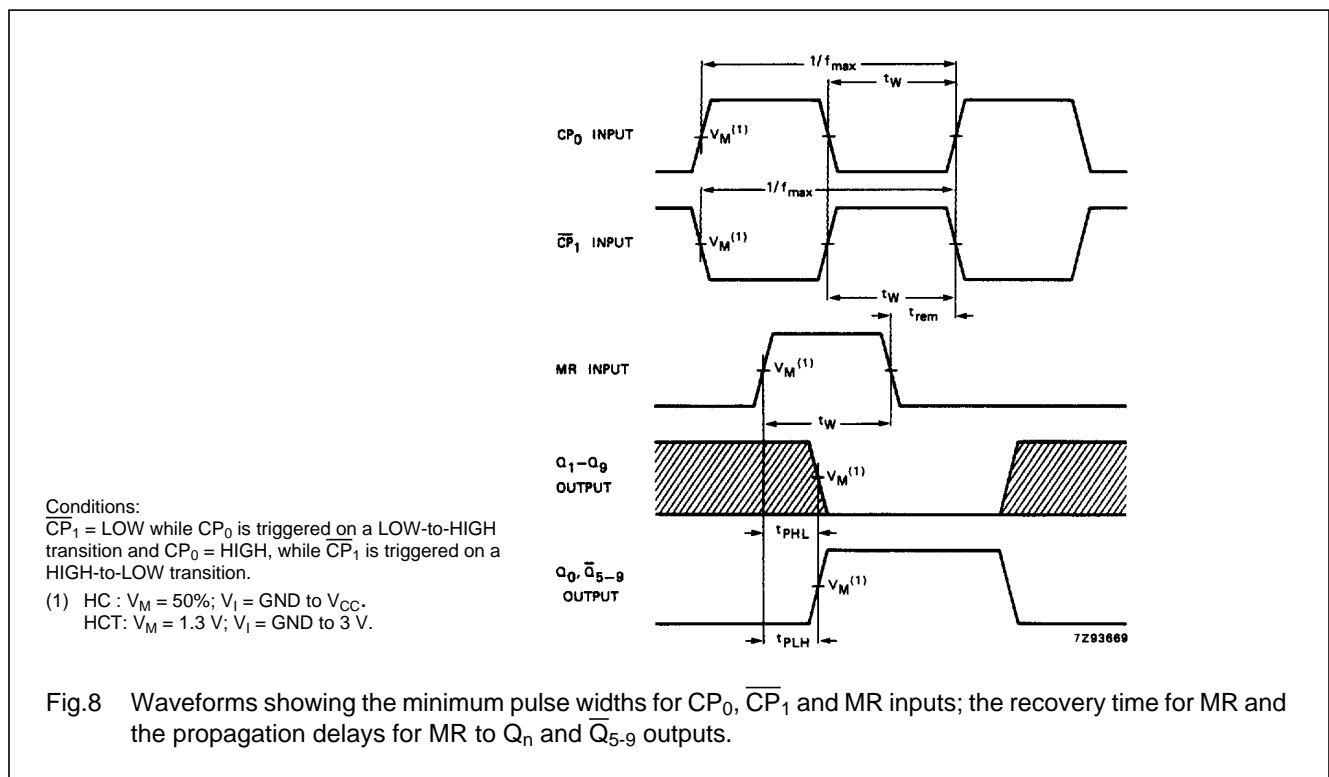
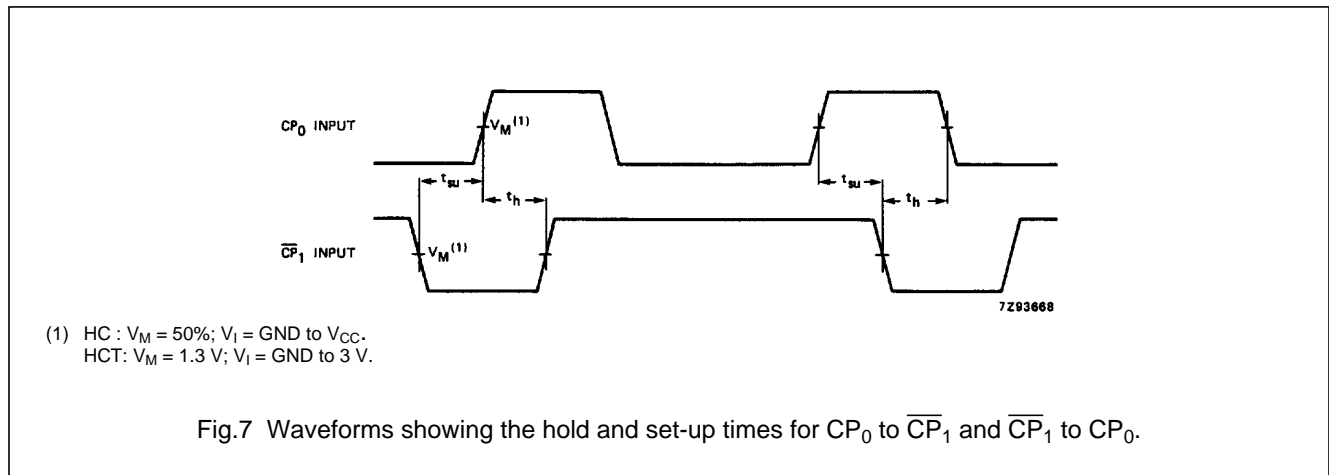
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V_{CC} (V)	WAVEFORMS	
		+25			-40 to+85		-40 to+125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay CP ₀ to Q _n		25	46		58		69	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay CP ₀ to Q ₅₋₉		25	46		58		69	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay \overline{CP}_1 to Q _n		25	50		63		75	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay \overline{CP}_1 to Q ₅₋₉		25	50		63		75	ns	4.5	Fig.9
t_{PHL}	propagation delay MR to Q ₁₋₉		22	46		58		69	ns	4.5	Fig.8
t_{PLH}	propagation delay MR to Q ₅₋₉ , Q ₀		20	46		58		69	ns	4.5	Fig.8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.9
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.8
t_W	master reset pulse width; HIGH	16	4		20		24		ns	4.5	Fig.8
t_{rem}	removal time MR to \overline{CP}_0 , \overline{CP}_1	5	-5		5		5		ns	4.5	Fig.8
t_{su}	set-up time \overline{CP}_1 to \overline{CP}_0 ; CP ₀ to \overline{CP}_1	10	-3		13		15		ns	4.5	Fig.7
t_h	hold time \overline{CP}_0 to \overline{CP}_1 ; \overline{CP}_1 to CP ₀	10	6		13		15		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	61		24		20		ns	4.5	Fig.8

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AC WAVEFORMS



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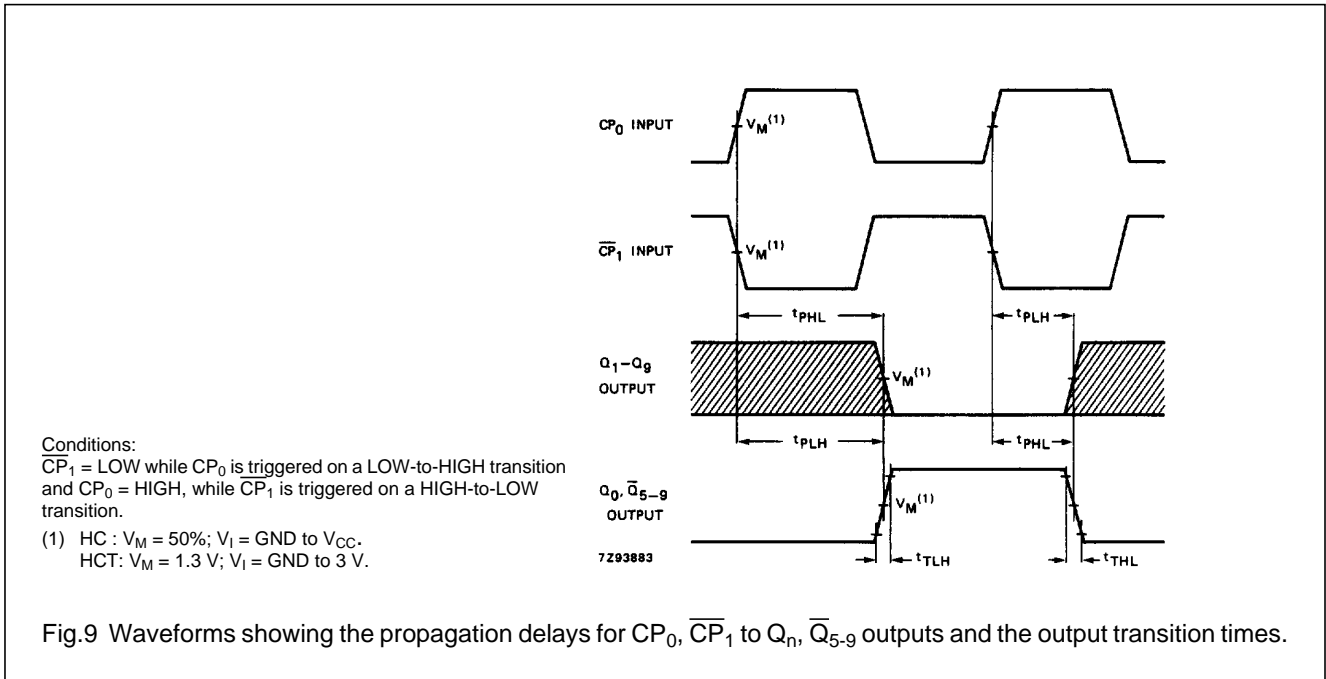


Fig.9 Waveforms showing the propagation delays for CP_0 , \overline{CP}_1 to Q_n , \overline{Q}_{5-9} outputs and the output transition times.

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APPLICATION INFORMATION

Some applications for the “4017” are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the “4017”. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

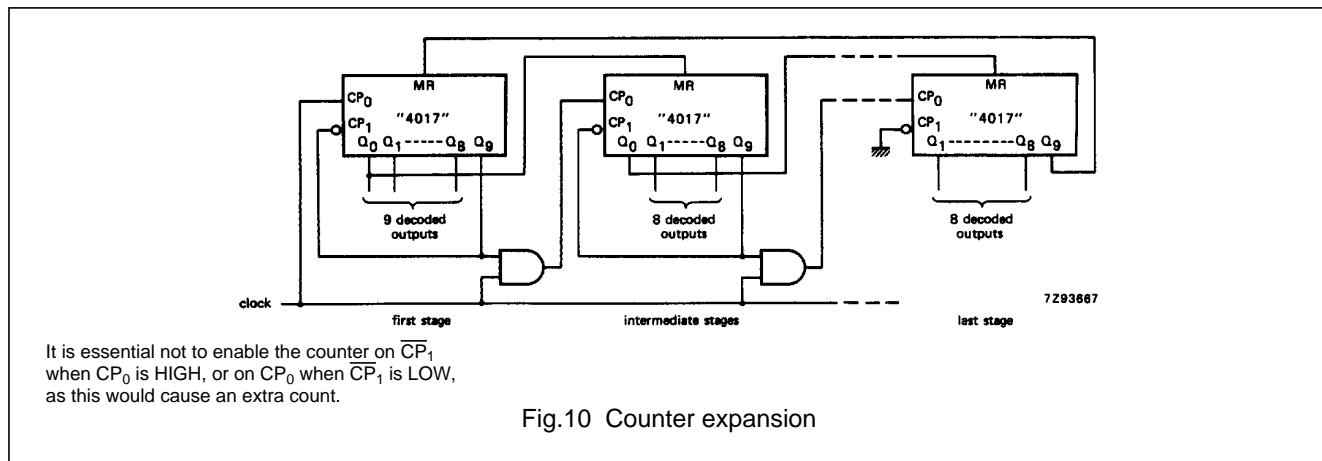
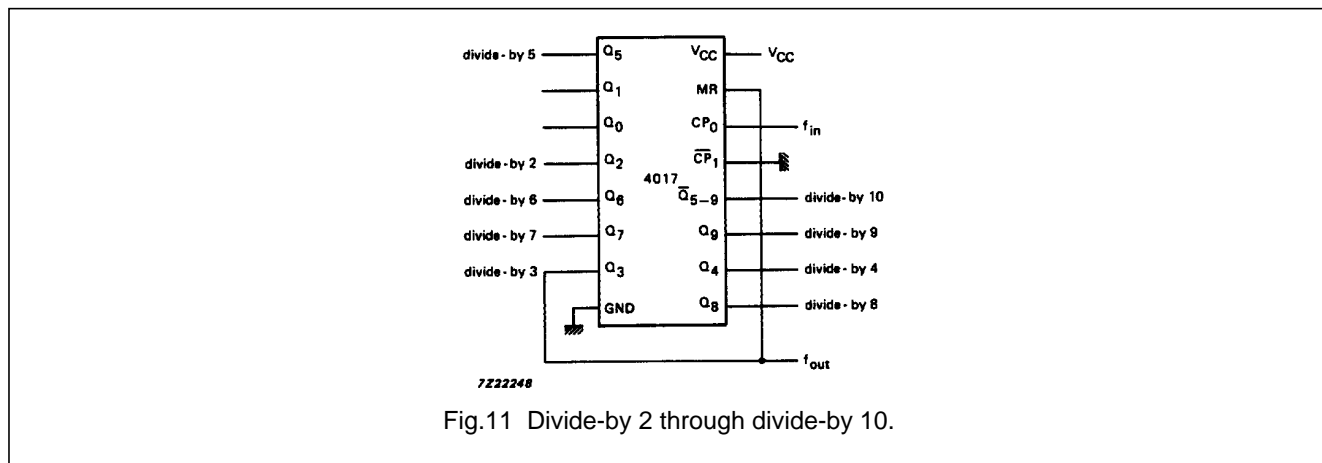


Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one “4017”. Since “4017” has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.



PACKAGE OUTLINES

See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.