MC74AC259, MC74ACT259

8-Bit Addressable Latch

The MC74AC259/74ACT259 is a high–speed 8–bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1–of–8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the ALS259 8–bit addressable latch.

- Serial–to–Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

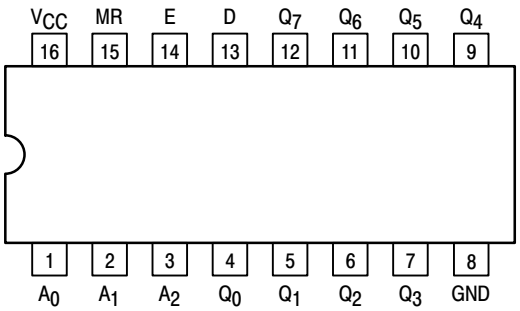

Figure 1. Pinout: 16–Lead Packages Conductors
(Top View)

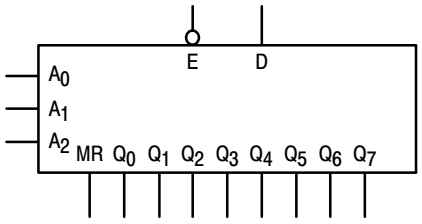

Figure 2. Logic Symbol

MODE SELECT TABLE

$\overline{E}$	$\overline{MR}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8–Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

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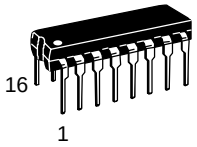
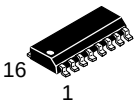
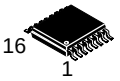


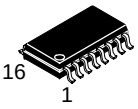
DIP–16
N SUFFIX
CASE 648



SO–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F



EIAJ–16
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
MC74AC259N	PDIP–16	25 Units/Rail
MC74ACT259N	PDIP–16	25 Units/Rail
MC74AC259D	SOIC–16	48 Units/Rail
MC74ACT259D	SOIC–16	48 Units/Rail
MC74AC259DR2	SOIC–16	2500 Tape & Reel
MC74ACT259DR2	SOIC–16	2500 Tape & Reel
MC74AC259DT	TSSOP–16	96 Units/Rail
MC74ACT259DT	TSSOP–16	96 Units/Rail
MC74AC259DTR2	TSSOP–16	2500 Tape & Reel
MC74ACT259DTR2	TSSOP–16	2500 Tape & Reel
MC74AC259M	EIAJ–16	50 Units/Rail

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

MODE SELECT–FUNCTION TABLE

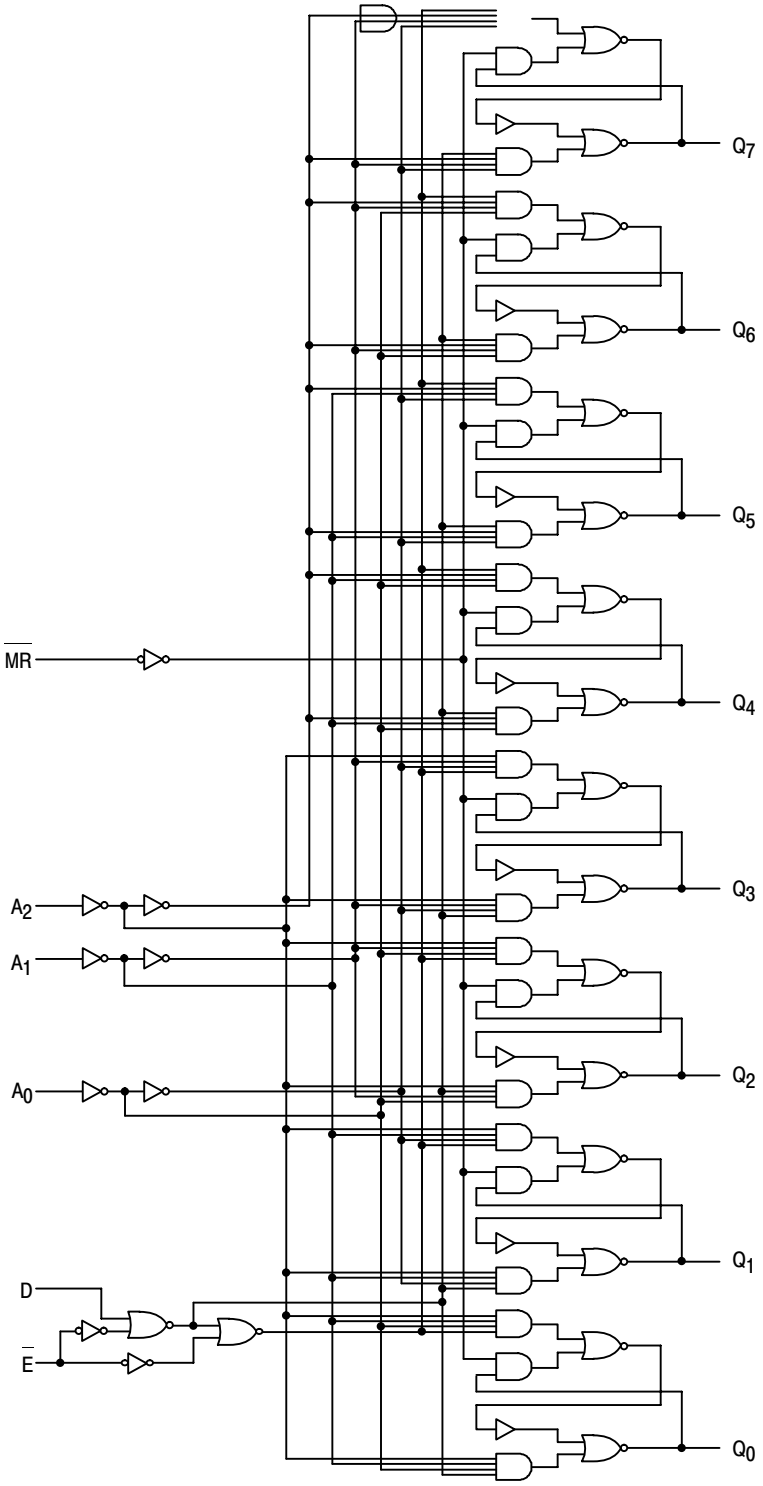
Operating Mode	Inputs						Outputs							
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (Do Nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable Latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW–to–HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

FUNCTIONAL DESCRIPTION

The MC74AC259/74ACT259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non–addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one–of–eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC74AC/ACT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Mode Select Function Table summarizes the operations of the MC74AC/ACT259.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – High		–	–	–24	mA
I_{OL}	Output Current – Low		–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC		74AC	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = –50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = –40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to Q_n	3.3 5.0	2.0 2.0	9.0 6.5	14.5 10.0	1.5 1.5	17.0 11.5	ns	3–5
t_{PHL}	Propagation Delay D_n to Q_n	3.3 5.0	2.0 2.0	9.0 6.0	13.5 9.5	1.5 1.5	16.0 11.0	ns	3–5
t_{PLH}	Propagation Delay E to Q_n	3.3 5.0	2.0 2.0	10.5 7.0	15.0 10.5	1.5 1.5	17.5 12.5	ns	3–6
t_{PHL}	Propagation Delay E to Q_n	3.3 5.0	2.0 2.0	8.0 7.5	12.5 9.0	1.5 1.5	15.0 11.0	ns	3–6
t_{PLH}	Propagation Delay Address to Q_n	3.3 5.0	2.0 2.0	12.0 8.0	19.0 13.0	1.5 1.5	22.5 15.5	ns	3–6
t_{PHL}	Propagation Delay Address to Q_n	3.3 5.0	2.0 2.0	10.0 7.0	16.0 11.0	1.5 1.5	19.0 13.0	ns	3–6
t_{PHL}	Propagation Delay MR to Q	3.3 5.0	2.0 2.0	8.0 6.0	12.0 9.0	1.5 1.5	13.5 10.0	ns	3–7

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = –40°C to +85°C, C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to E	3.3 5.0	– –	3.5 2.5	4.5 3.5	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to E	3.3 5.0	– –	2.5 2.0	2.5 2.0	ns	3–9
t_s	Setup Time Address to E	3.3 5.0	– –	7.0 4.0	9.0 6.0	ns	3–6
t_h	Hold Time Address to E	3.3 5.0	– –	2.0 2.0	2.0 2.0	ns	3–6
t_w	Minimum Pulse Width MR	3.3 5.0	– –	6.0 5.5	6.5 6.0	ns	3–6
t_w	Minimum Pulse Width E	3.3 5.0	– –	6.5 5.5	7.0 6.0	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		74ACT T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –24 mA I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = –40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to Q_n	5.0	2.0	6.5	11.0	1.5	12.5	ns	3–5
t_{PHL}	Propagation Delay D_n or Q_n	5.0	2.0	7.0	10.5	1.5	12.0	ns	3–5
t_{PLH}	Propagation Delay E to Q_n	5.0	2.0	10.5	14.0	1.5	16.5	ns	3–6
t_{PHL}	Propagation Delay E or Q_n	5.0	2.0	9.0	12.0	1.5	14.0	ns	3–6
t_{PLH}	Propagation Delay Address to Q_n	5.0	2.0	8.0	11.5	1.5	13.5	ns	3–6
t_{PHL}	Propagation Delay Address to Q_n	5.0	2.0	6.0	10.0	1.5	12.0	ns	3–6
t_{PHL}	Propagation Delay MR to Q	5.0	2.0		10.0	1.5	11.0	ns	3–7

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT		74ACT	Unit	Fig. No.
			T_A = +25°C C_L = 50 pF		T_A = –40°C to +85°C C_L = 50 pF		
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to E	5.0	–	3.0	4.0	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to E	5.0	–	2.5	2.5	ns	3–9
t_s	Setup Time Address to E	5.0	–	4.5	6.5	ns	3–6
t_h	Hold Time Address to E	5.0	–	2.5	2.5	ns	3–6
t_w	Minimum Pulse Width MR	5.0	–	7.0	7.5	ns	3–6
t_w	Minimum Pulse Width E	5.0	–	7.0	7.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

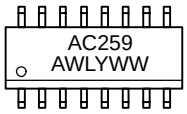
CAPACITANCE

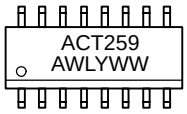
Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0 V

MARKING DIAGRAMS

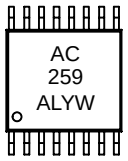
DIP–16

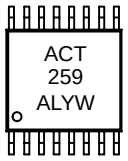
SO–16



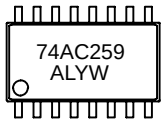


TSSOP–16





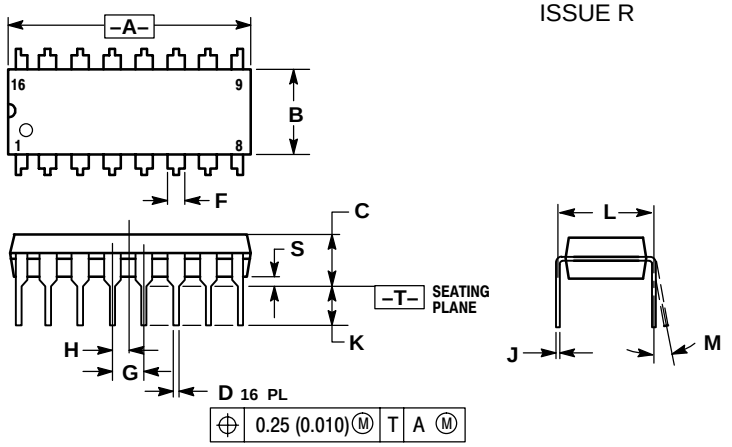
EIAJ–16



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

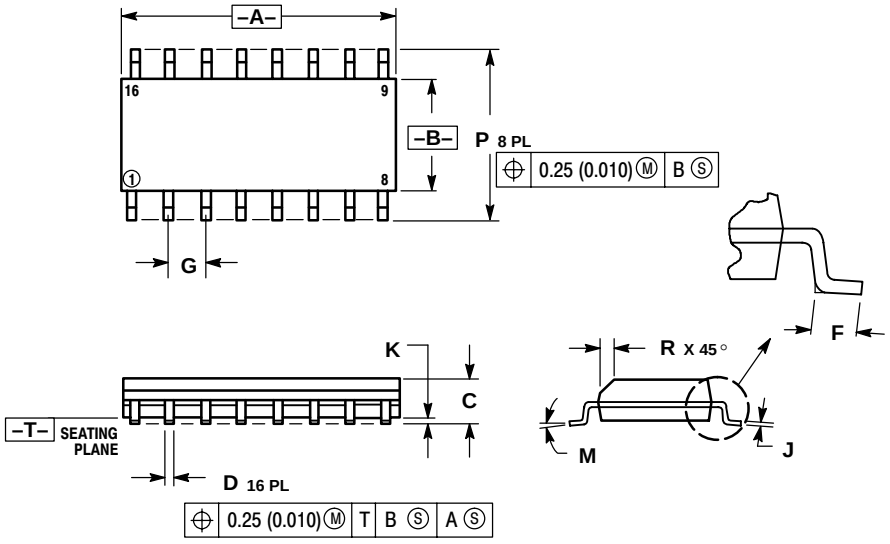
PDIP–16
N SUFFIX
16 PIN PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SO–16
D SUFFIX
16 PIN PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

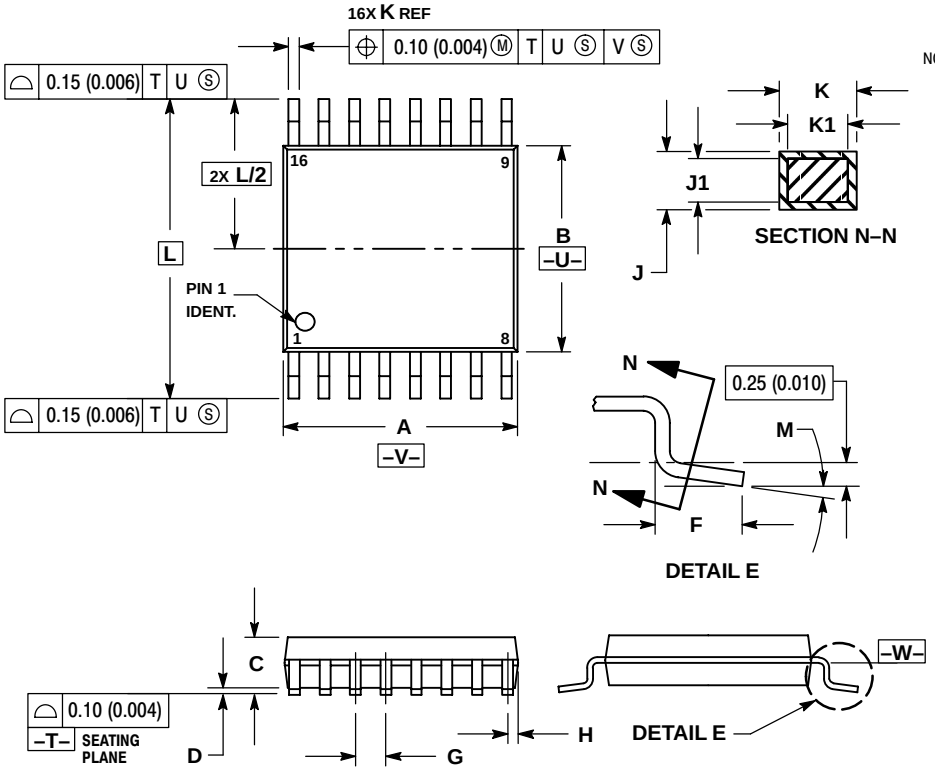


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

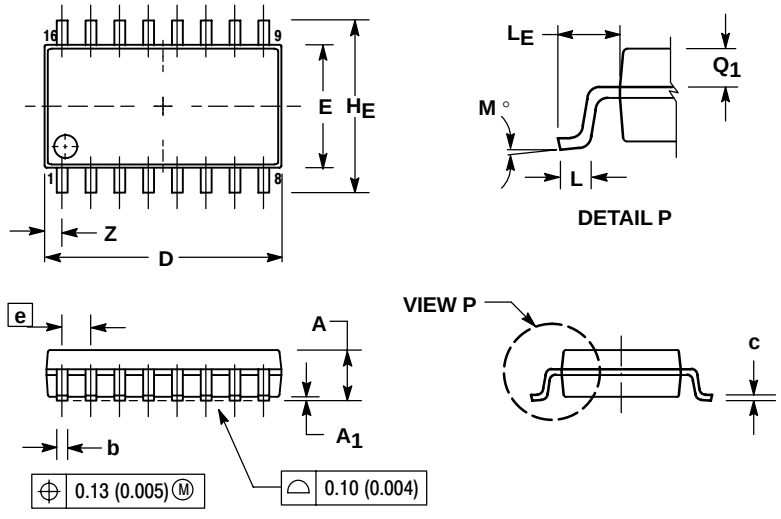
TSSOP–16
DT SUFFIX
16 PIN PLASTIC TSSOP PACKAGE
CASE948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

EIAJ–16
M SUFFIX
16 PIN PLASTIC EIAJ PACKAGE
CASE966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

Notes

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