MC100EL13

5V ECL Dual 1:3 Fanout Buffer

The MC100EL13 is a dual, fully differential 1:3 fanout buffer. The Low Output-Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The $\overline{D}$ input will bias around $V_{CC}/2$ and the Q output will go LOW.

- 500 ps Typical Propagation Delays
- 50 ps Output-Output Skews
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Internal Input Pull-down Resistors on All Inputs, Pull-up Resistors on Inverted Inputs

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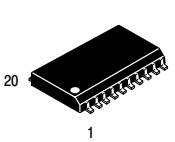
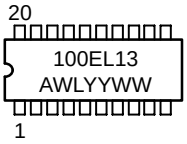
MARKING DIAGRAM*



SO-20L
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION†

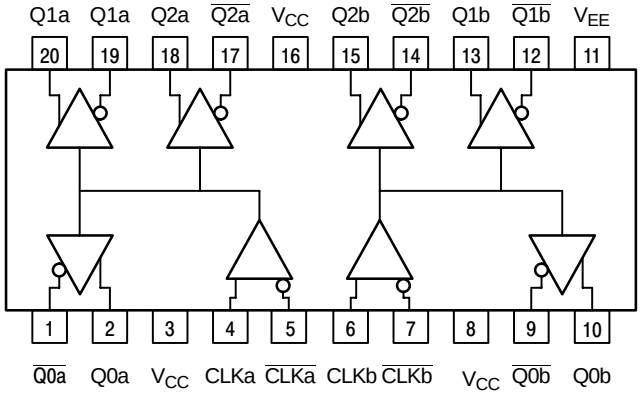
Device	Package	Shipping
MC100EL13DW	SO-20L	38 Units/Rail
MC100EL13DWR2	SO-20L	1000 / Tape & Reel

†For additional tape and reel information, refer to Brochure BRD8011/D.

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 +KΩ
Internal Input Pullup Resistor		75 KΩ
ESD Protection	Human Body Model Machine Model Charge Device Model	> 2 KV > 200 V > 4 KV
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		143 Devices
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout: Assignment

PIN DESCRIPTION

PIN	FUNCTION
Qna, $\overline{Qna}$	ECL Differential Clock Outputs
Qnb, $\overline{Qnb}$	ECL Differential Clock Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
V_{CC}	Positive Supply
VEE	Negative Supply

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		-8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-20L SO-20L	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-20L	30 to 35	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 3)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 3)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 4) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 1.3 1.5		 4.6 4.6	 1.2 1.4		 4.6 4.6	 1.2 1.4		 4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = -5.0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 6)	- 1085	- 1005	- 880	- 1025	- 955	- 880	- 1025	- 955	- 880	mV
V_{OL}	Output LOW Voltage (Note 6)	- 1830	- 1695	- 1555	- 1810	- 1705	- 1620	- 1810	- 1705	- 1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	- 1165		- 880	- 1165		- 880	- 1165		- 880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	- 1810		- 1475	- 1810		- 1475	- 1810		- 1475	mV
V_{BB}	Output Voltage Reference	- 1.38		- 1.26	- 1.38		- 1.26	- 1.38		- 1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 7) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 - 3.7 - 3.5		 - 0.4 - 0.4	 - 3.8 - 3.6		 - 0.4 - 0.4	 - 3.8 - 3.6		 - 0.4 - 0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

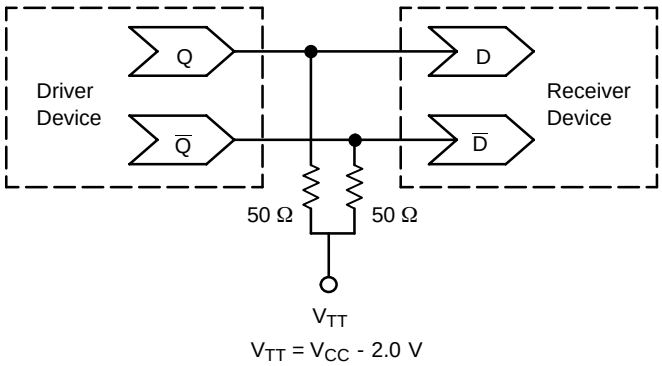
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = -5.0 V (Note 8)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK→Q/$\overline{Q}$	410		600	430		620	450		640	ps
$t_{sk(O)}$	Output-Output Skew Any Qa→Qa, Any Qb→Qb Any Qa→Any Qb			 50 75			 50 75			 50 75	ps
$t_{sk(DC)}$	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			50			50			50	ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 9)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	230		500	230		500	230		500	ps

8. V_{EE} can vary +0.8 V / -0.5 V.
9. V_{PP}min is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.



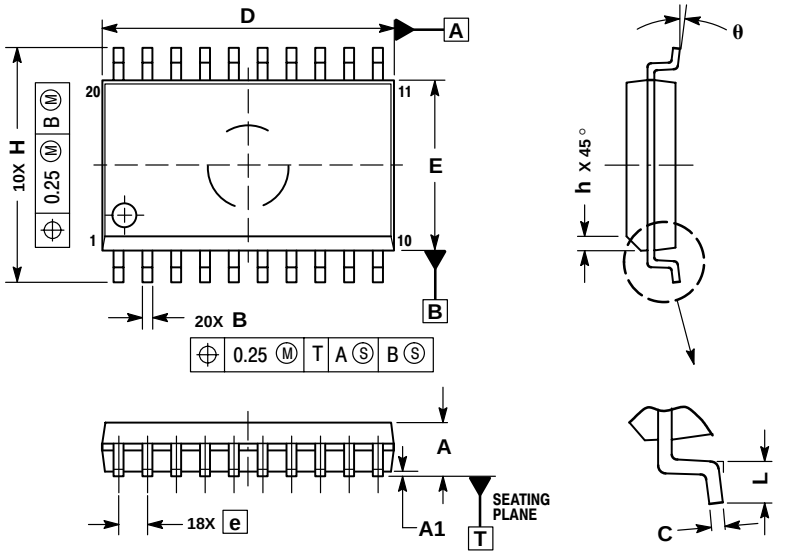
Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	-	ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
AN1405	-	ECL Clock Distribution Techniques
AN1406	-	Designing with PECL (ECL at +5.0 V)
AN1503	-	ECLinPS I/O SPICE Modeling Kit
AN1504	-	Metastability and the ECLinPS Family
AN1560	-	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	-	Interfacing Between LVDS and ECL
AN1596	-	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	-	Using Wire-OR Ties in ECLinPS Designs
AN1672	-	The ECL Translator Guide
AND8001	-	Odd Number Counters Design
AND8002	-	Marking and Date Codes
AND8020	-	Termination of ECL Logic Devices
AND8090	-	AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO-20L
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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