BC857BTT1, BC857CTT1

Preferred Devices

Advance Information

General Purpose Transistor

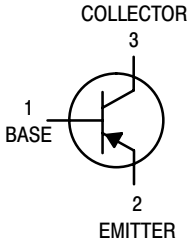
PNP Silicon

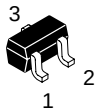
These transistors are designed for general purpose amplifier applications. They are housed in the SOT–416/SC–75 which is designed for low power surface mount applications.

- Device Marking:
  BC857BTT1 = 3F
  BC857CTT1 = 3G

ON Semiconductor

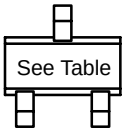
http://onsemi.com





CASE 463
SOT–416/SC–75
STYLE 1

DEVICE MARKING



MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	–45	V
Collector–Base Voltage	V_{CBO}	–50	V
Emitter–Base Voltage	V_{EBO}	–5.0	V
Collector Current — Continuous	I_C	–100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR–4 Board (1) T_A = 25°C Derated above 25°C	P_D	200 1.6	mW mW/°C
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR–4 Board (2) T_A = 25°C Derated above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient (2)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

(1) FR–4 @ Minimum Pad
(2) FR–4 @ 1.0 × 1.0 Inch Pad

ORDERING INFORMATION

Device	Package	Shipping
BC857BTT1	SOT–416	3000 / Tape & Reel
BC857CTT1	SOT–416	3000 / Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = –10 mA)	BC857 Series	$V_{(BR)CEO}$	–45	—	—	V
Collector–Emitter Breakdown Voltage (I_C = –10 μA, V_{EB} = 0)	BC857B Only	$V_{(BR)CES}$	–50	—	—	V
Collector–Base Breakdown Voltage (I_C = –10 μA)	BC857 Series	$V_{(BR)CBO}$	–50	—	—	V
Emitter–Base Breakdown Voltage (I_E = –1.0 μA)	BC857 Series	$V_{(BR)EBO}$	–5.0	—	—	V
Collector Cutoff Current (V_{CB} = –30 V)		I_{CBO}	—	—	–15	nA
(V_{CB} = –30 V, T_A = 150°C)			—	—	–4.0	μA
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = –10 μA, V_{CE} = –5.0 V)	BC857B		—	150	—	
	BC857C		—	270	—	
(I_C = –2.0 mA, V_{CE} = –5.0 V)	BC857B		220	290	475	
	BC857C		420	520	800	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = –10 mA, I_B = –0.5 mA)			—	—	–0.3	
(I_C = –100 mA, I_B = –5.0 mA)			—	—	–0.65	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				V
(I_C = –10 mA, I_B = –0.5 mA)			—	–0.7	—	
(I_C = –100 mA, I_B = –5.0 mA)			—	–0.9	—	
Base–Emitter On Voltage		$V_{BE(on)}$				V
(I_C = –2.0 mA, V_{CE} = –5.0 V)			–0.6	—	–0.75	
(I_C = –10 mA, V_{CE} = –5.0 V)			—	—	–0.82	
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = –10 mA, V_{CE} = –5.0 Vdc, f = 100 MHz)		f_T	100	—	—	MHz
Output Capacitance (V_{CB} = –10 V, f = 1.0 MHz)		C_{ob}	—	—	4.5	pF
Noise Figure (I_C = –0.2 mA, V_{CE} = –5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)		NF	—	—	10	dB

TYPICAL CHARACTERISTICS

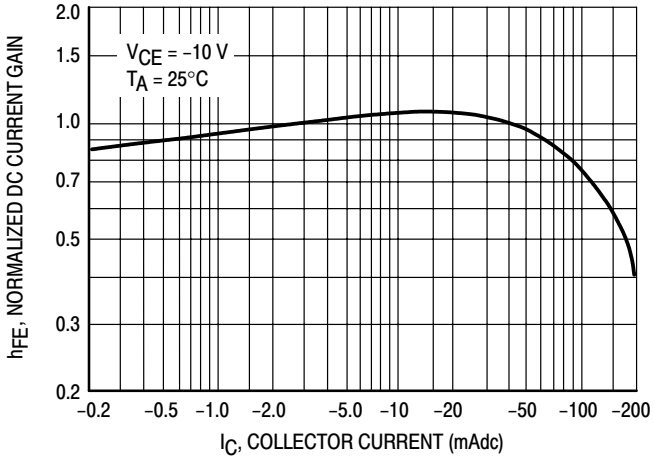


Figure 1. Normalized DC Current Gain

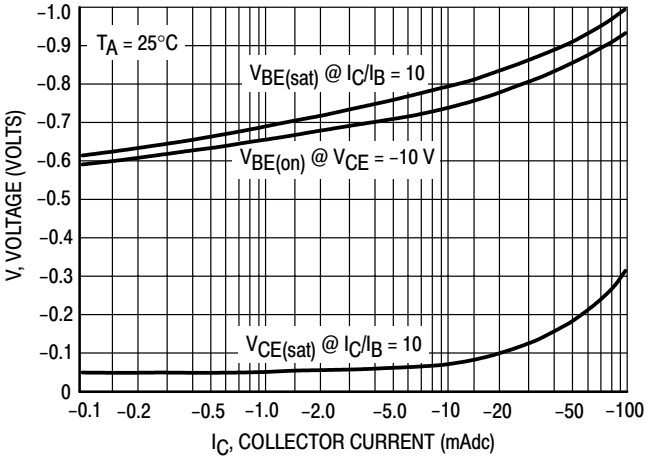


Figure 2. “Saturation” and “On” Voltages

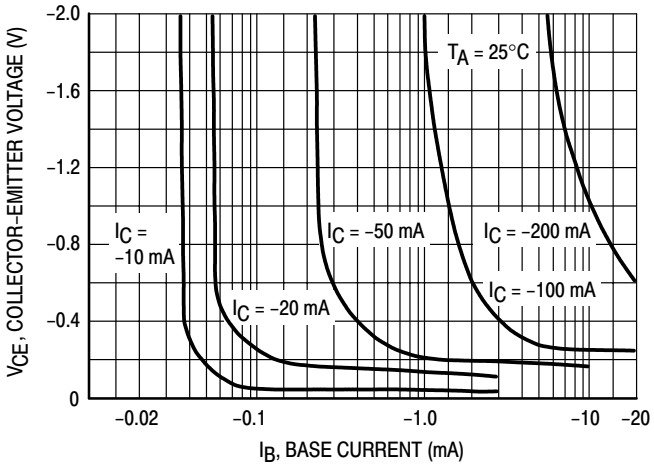


Figure 3. Collector Saturation Region

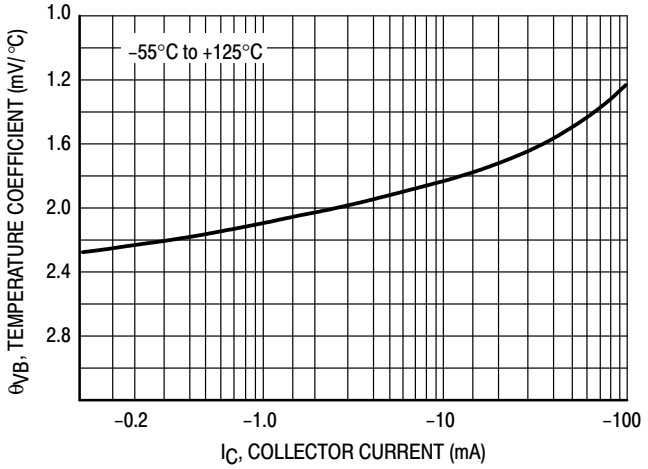


Figure 4. Base−Emitter Temperature Coefficient

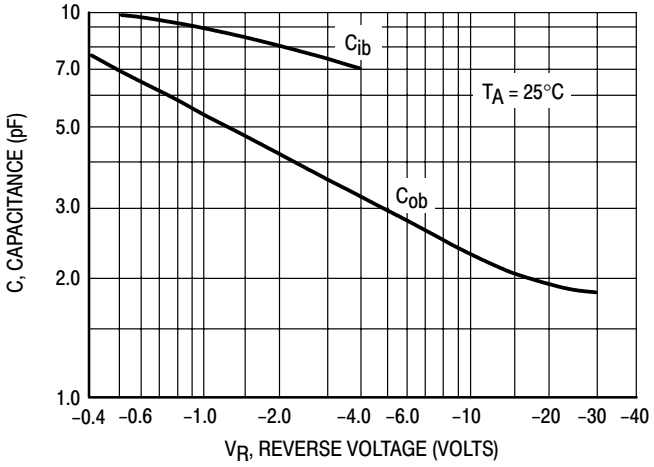


Figure 5. Capacitances

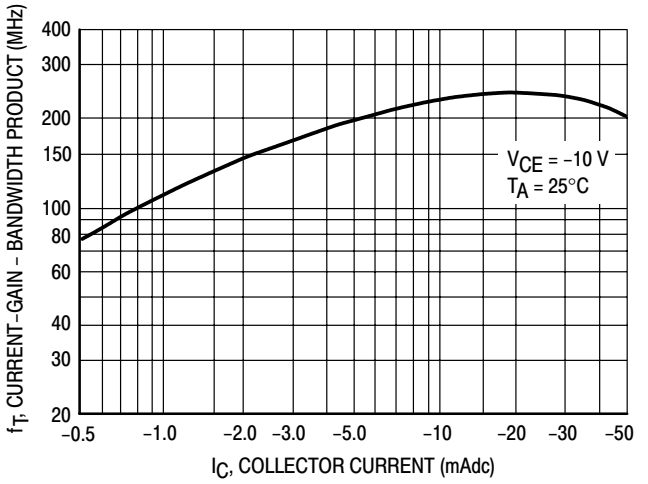


Figure 6. Current−Gain − Bandwidth Product

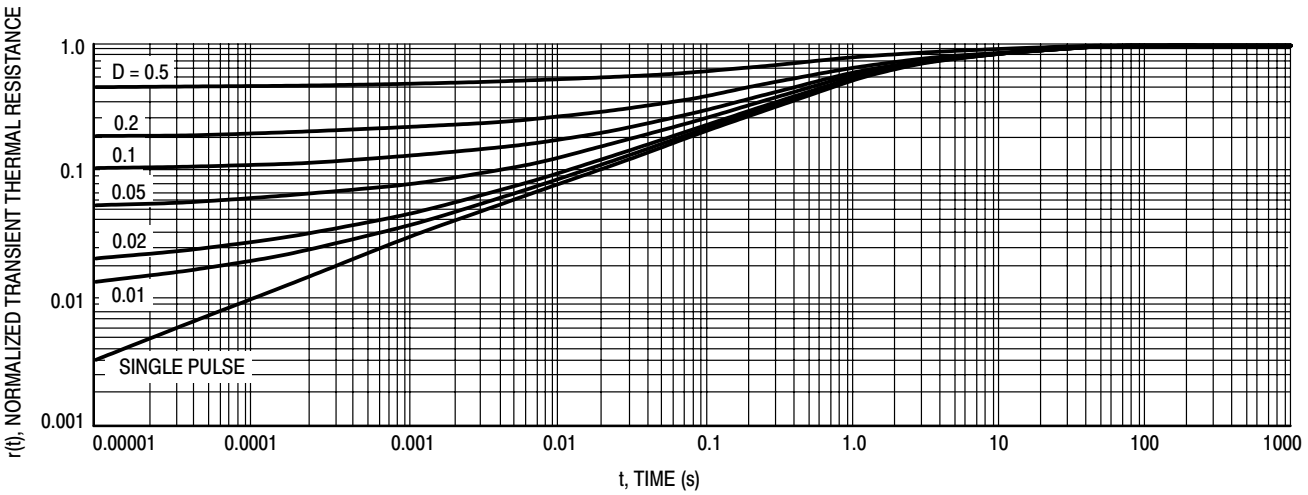


Figure 7. Thermal Response

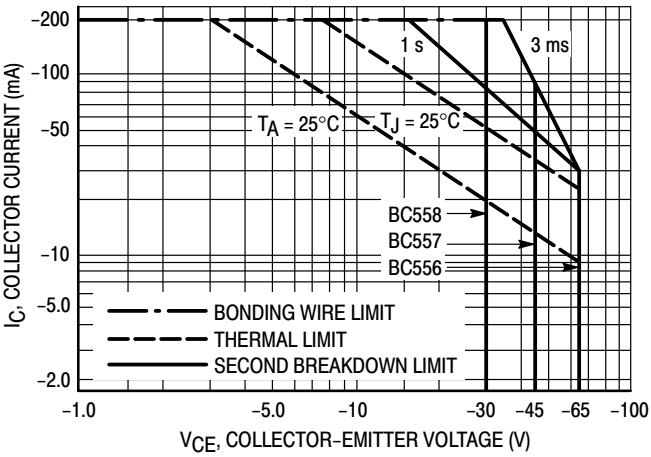


Figure 8. Active Region Safe Operating Area

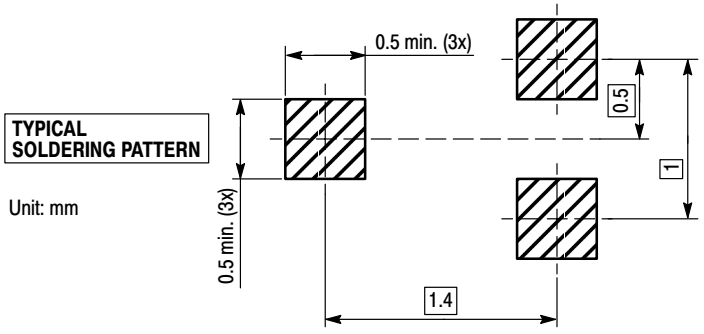
The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 8 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

INFORMATION FOR USING THE SOT–416 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–416/SC–90 POWER DISSIPATION

The power dissipation of the SOT–416/SC–90 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R\theta_{JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 125 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, a higher power dissipation can be achieved using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 7 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

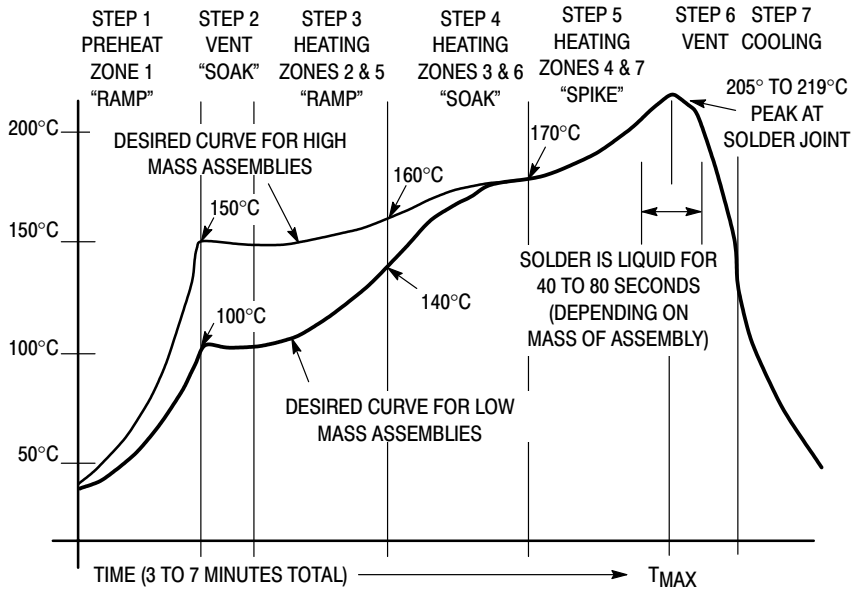
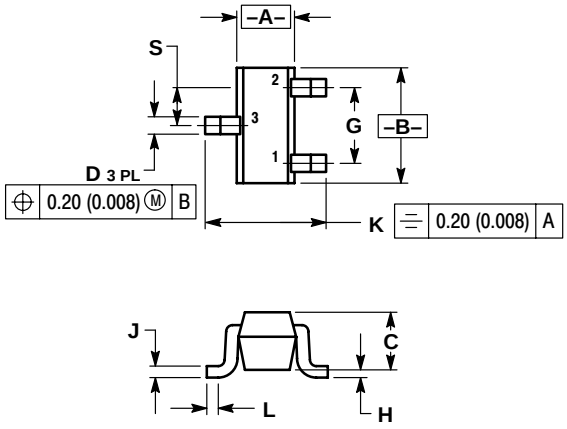


Figure 9. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT–416/SC–75
CASE 463–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
B	1.40	1.80	0.055	0.071
C	0.60	0.90	0.024	0.035
D	0.15	0.30	0.006	0.012
G	1.00 BSC		0.039 BSC	
H	---	0.10	---	0.004
J	0.10	0.25	0.004	0.010
K	1.45	1.75	0.057	0.069
L	0.10	0.20	0.004	0.008
S	0.50 BSC		0.020 BSC	

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

Thermal Clad is a trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.