National Semiconductor

PRELIMINARY
July 1994

TP3404
Quad Digital Adapter for Subscriber Loops (QDASL)

General Description

The TP3404 is a combination 4-line transceiver for voice and data transmission on twisted pair subscriber loops, typically in PBX line card applications. It is a companion device to the TP3401/2/3 DASL single-channel transceivers. In addition to 4 independent transceivers, a time-slot assignment circuit is included to support interfacing to the system backplane.

Each QDASL line operates as an ISDN "U" Interface for short loop applications, typically in a PBX environment, providing transmission for 2 B channels and 1 D channel.

Full-duplex transmission at 144 kb/s is achieved on single twisted wire pairs using a burst-mode technique (Time Compression Multiplexed). All timing sequences necessary for loop activation and de-activation are generated on-chip.

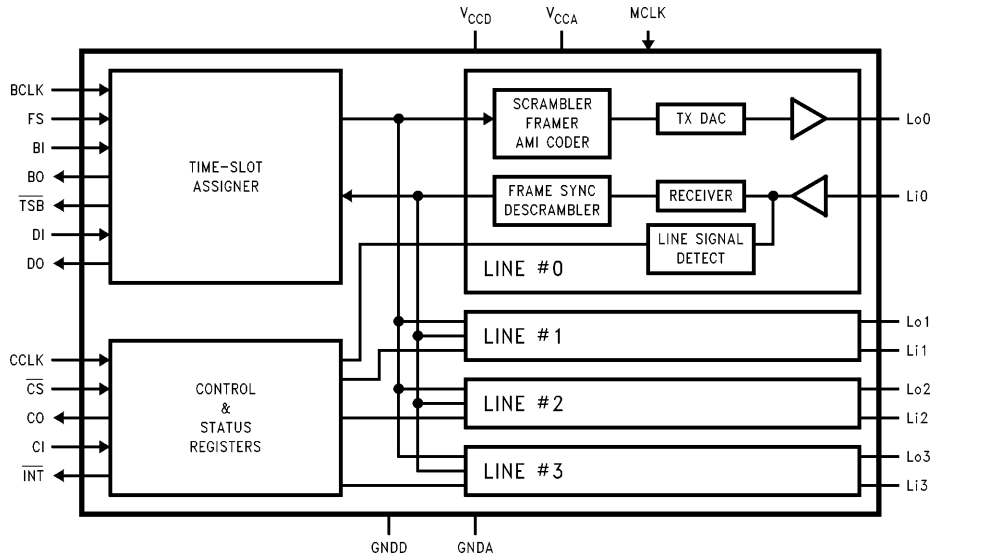
Alternate Mark Inversion (AMI) line coding is used to ensure low error rates in the presence of noise with lower emi radiation than other codes such as Biphase (Manchester). On #24 AWG cable the range is at least 1.8 km (6k ft).

Features

4 COMPLETE ISDN PBX 2-WIRE DATA TRANSCEIVERS INCLUDING:

- Quad 2 B plus D channel interface for PBX "U" interface
- 144 kb/s full-duplex on 1 twisted pair using Burst Mode Transmission Technique
- Loop range up to 6 kft (#24AWG)
- Alternate Mark Inversion coding with transmit Pulse Shaping DAC, Smoothing Filter, and scrambler for low emi radiation
- Adaptive line equalizer
- On-chip timing recovery, no external components
- Programmable Time-Slot Assignment TDM interface for B channels
- Separate interface for D channel with Programmable Sub-Slot Assignment
- 4.096 MHz master clock
- 4 loop-back test modes
- MICROWIRE™ compatible serial control interface
- 5V operation
- 28-pin PLCC package

Block Diagram



TL/H/11924–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
MICROWIRE™ is a trademark of National Semiconductor Corporation.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{DDA}/V_{DDD} to GNDA/GNDD	7V
Voltage at Any Li, Lo Pin	V_{CC} + 1V to GND − 1V
Current at Any Lo	±100 mA
Voltage at Any Digital Input	V_{CC} + 1V to GND − 1V
Current at Any Digital Output	±50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise specified, limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $T_A = 0°C$ to $+70°C$. Typical characteristics are specified at $V_{DDA} = V_{DDD} = 5.0V$, $T_A = 25°C$. All signals are referenced to GND, which is the common of GNDA and GNDD

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IH}	Input High Voltage	All Digital Inputs (DC)	**2**			V
V_{IL}	Input Low Voltage	All Digital Inputs (DC)			**0.8**	V
V_{OH}	Output High Voltage	$I_L = +1$ mA	**2.4**			V
V_{OL}	Output Low Voltage	$I_L = -1$ mA			**0.4**	V
I_{IL}	Input Low Current	All Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	μA
I_{IH}	Input High Current	All Digital Input, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance (TRI-STATE®)	BO, CO, and DO	−10		10	μA
LINE INTERFACES						
R_{Li}	Input Resistance	0V < V_{Li} < V_{CC}	20			kΩ
C_{LLo}	Load Capacitance	From Lo to GND			200	pF
ROLS	Output Resistance	Load = 60Ω in Series with 2 μF to GND			3	Ω
V_{DC}	Mean DC Voltage at Lo Voltage at LS+, LS−	Load = 200Ω in Series with 2 μF to GND	1.75		2.25	V
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	BCLK = 0 Hz; MCLK = 0 Hz, CCLK = 0 Hz			10	mA
$I_{CC}1$	Power Up Current	All 4 Channels Activated			**75**	mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude at Lo	R_L = 200Ω in Series with 2 μF to GND	1.1	1.3	1.5	Vpk
	Input Pulse Amplitude at Li		**±60**			mVpk

TIMING SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK INPUT SPECIFICATIONS						
f_{MCLK}	Frequency of MCLK			**4.096**		MHz
	Master Clock Tolerance	Relative 2X MCLK in Slave	−100		+100	ppm
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH}	**70**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL}	**70**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			15	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			15	ns

Electrical Characteristics

Unless otherwise specified, limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $T_A = 0°C$ to $+70°C$. Typical characteristics are specified at $V_{DDA} = V_{DDD} = 5.0V$, $T_A = 25°C$. All signals are referenced to GND, which is the common of GNDA and GNDD (Continued)

TIMING SPECIFICATIONS (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE TIMING						
f_{BCLK}	BCLK Frequency			**4.096**	4.1	MHz
t_{WBH}, t_{WBL}	Clock Pulse Width High and Low for BCLK	Measured from V_{IH} to V_{IH} Measured from V_{IL} to V_{IL}	**70** **70**			ns
t_{RB}, t_{FB}	Rise Time and Fall Time of BCLK	Measured from V_{IL} to V_{IH} Measured from V_{IH} to V_{IL}			15 15	ns
t_{HBM}	BCLK Transition to MCLK High or Low		**−30**		**30**	ns
t_{SFC}	Set up Time, FS Valid to BCLK Invalid		**20**	4		ns
t_{HCF}	Hold Time, BCLK Low to FS Invalid		**40**	30		ns
t_{SBC}	Setup Time, BI Valid to BCLK Invalid		**30**	11		ns
t_{HCB}	Hold Time, BCLK Valid to BI Invalid		**40**	7		ns
t_{SDC}	Setup Time, DI Valid to BCLK Low		**30**			ns
t_{HCD}	Hold Time, BCLK Low to DI Invalid		**40**			ns
t_{DCB}	Delay Time, BCLK High to BO Valid	Load = 2 LSTTL + 100 pF			**80**	ns
t_{DCBZ}	Delay Time, BCLK Low to BO High-Z		**80**		**120**	ns
t_{DCD}	Delay Time, BCLK High to DO valid	Load = 2 LSTTL + 100 pF			**80**	ns
t_{DCZ}	Delay Time, BCLK Low to DO High Impedance		**40**		**120**	ns
t_{DCT}	Delay Time, BCLK High to $\overline{TSB}$ Low				**120**	ns
t_{ZBT}	Disable Time, BCLK Low to $\overline{TSB}$ High-Z				**120**	ns
MICROWIRE CONTROL INTERFACE TIMING						
f_{CCLK}	Frequency of CCLK				2.1	MHz
t_{CH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**150**			ns
t_{CL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	**150**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Low to CCLK High		**50**			ns
t_{HCS}	Hold Time, CCLK High to $\overline{CS}$ Transition		**40**			ns
t_{SIC}	Setup Time, CI Valid to CCLK High		**50**			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		**20**			ns
t_{DCO}	Delay Time, CCLK Low to CO Valid				**80**	ns
t_{DSOZ}	Delay Time, $\overline{CS}$ High to CO High-Z				80	ns
t_{DCIZ}	Delay Time, CCLK to INT High-Z				100	ns

Notes: For the purposes of this specification the following conditions apply

a. All input signals are defined as $V_{IL} = 0.4V$, $V_{IH} = 2.7V$, $t_r < 10$ ns, $t_f < 10$ ns.

b. Delay times are measured from the input signal Valid to the output signal Valid.

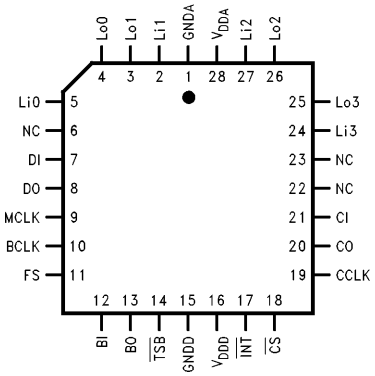
c. Setup times are measured from the Data input Valid to the clock input Invalid.

d. Hold times are measured from the clock signal Valid to the Data input Invalid.

Pin Descriptions

Pin No.	Pin Name	Description
1	GNDA	Analog Ground or 0V. All analog signals are referenced to this pin.
15	GNDD	Digital Ground 0V. It must connect to GNDA with a shortest possible trace. This can be done directly underneath the part.
28	VDDA	Positive power supply input to QDASL analog section. It must be 5V ±5%.
16	VDDD	Positive power supply input to QDASL digital section. It must be 5V ±5%, and connect to VDDA with the shortest possible trace. This can be done directly underneath the part.
11	FS	Frame Sync input: this signal is the 8 kHz clock which defines the start of the transmit and receive frames at the digital interfaces.
9	MCLK	This pin is the 4.096 MHz Master Clock input, which requires a CMOS logic level clock from a stable source. MCLK must be synchronous with BCLK.
10	BCLK	Bit Clock logic input, which determines the data shift rate for B and D channel data at the BI, BO, DI and DO pins. BCLK may be any multiple of 8 kHz from 256 kHz to 4.096 MHz, but must be synchronous with MCLK.
12	BI	Time-division multiplexed input for B1 and B2 channel data to be transmitted to the 4 lines. Data on this pin is shifted in on the failing edge of BCLK into the B1 and B2 channels during the selected transmit time-slots.
13	BO	Time-division multiplexed receive data output bus. B1 and B2 channel data from all 4 lines is shifted out on the rising edge of BCLK on this pin during the assigned receive time-slots. At all other times this output is TRI-STATE (high impedance).
14	$\overline{\text{TSB}}$	This pin is an open-drain output which is normally high impedance but pulls low during any active B channel receive time slots at the BO pin.
7	DI	Time-division multiplexed input for D channel data to be transmitted to the 4 lines. Data on this pin is shifted in on the failing edge of BCLK into the D channel during the selected transmit sub-time-slots.
8	DO	Time-division multiplexed output for D channel data received from the 4 lines. Data on this pin is shifted out on the rising edge of BCLK during the selected receive sub-time-slot.
19	CCLK	Microwire Control Clock input. This clock shifts serial control information into CI and out from CO when the $\overline{\text{CS}}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
21	CI	Control data Input. Serial control information is shifted into the QDASL on this pin on the rising edges of CCLK when $\overline{\text{CS}}$ is low.
17	$\overline{\text{INT}}$	Interrupt request output, a latched output signal which is normally high impedance and goes low to indicate a change of status of any of the 4 loop transmission systems. This latch is cleared when the Status Register is read by the microprocessor. Bipolar Violation does not effect this output.
20	CO	Control data Output. Serial control/status information is shifted out from the QDASL on this pin on the falling edges of CCLK when $\overline{\text{CS}}$ is low.
18	$\overline{\text{CS}}$	Chip Select input. When this pin is pulled low, the Microwire interface is enabled to allow control information to be written in to and out from the device via the CI and CO ins. When high, this pin inhibits the Microwire interface.
4 3 26 25	Lo0 Lo1 Lo2 Lo3	Line driver transmit outputs for the 4 transmission channels. Each output is an amplifier intended to drive a transformer.
5 2 27 24	Li0 Li1 Li2 Li3	Line receive amplifier inputs for the 4 transmission channels. Each Li pin is a self-biased high impedance input which should be connected to the transformer via the recommended line interface circuit.

Connection Diagram



TL/H/11924–2

Top View

Order Number TP3404V
See NS Package Number V28A

Functional Description

The QDASL contains 4 transceivers, each of which can interoperate with any of the TP340X family of single-channel DASL transceivers. Each QDASL transceiver has its own independent line transmit and receive section, timing recovery circuit, scrambler/descrambler and loop activation controller. Functions which are shared by the 4 transceivers include the Microwire control port and the digital interface with time-slot assignment.

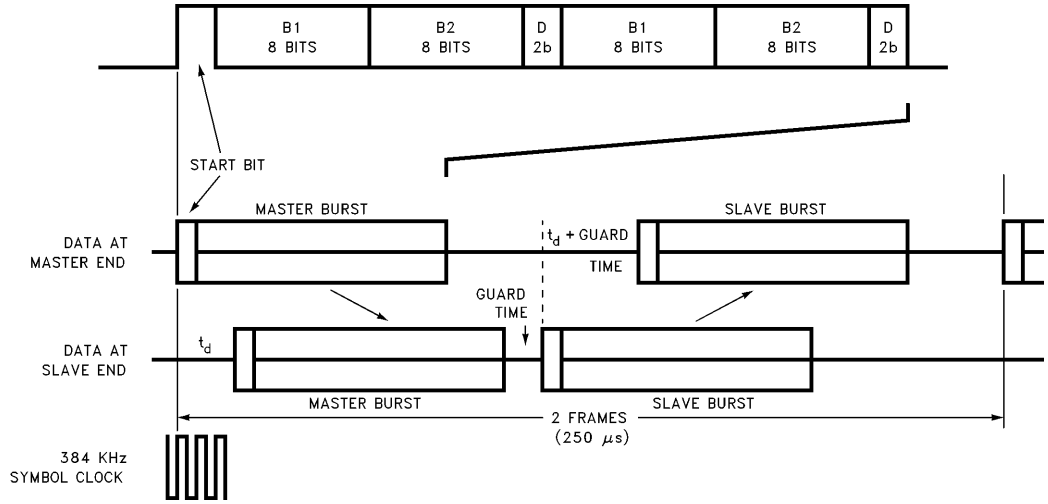
BURST MODE OPERATION

For full-duplex operation over a single twisted-pair, burst mode timing is used, with the QDASL end of each line acting as the loop timing master, and the DASL at the terminal being the timing slave (the QDASL transceivers cannot operate in loop timing slave mode).

Each burst within a DASL line is initiated by the QDASL Master transmitting a startbit, for burst framing, followed by the B1, B2 and D channel data from 2 consecutive 8 kHz frames, combined in the format shown in *Figure 1.* During transmit bursts the receiver input for that channel is inhibited to avoid disturbing the adaptive circuits. The slave's receiver is enabled at this time and it synchronizes to the start bit of the burst, which is always an unscrambled ''1'' (of the opposite polarity to the last ''1'' sent in the previous burst). When the slave detects that 36 bits following the start bit have been received, it disables the received input, waits 6 line symbol periods to match the other end settling guard time, and then begins to transmit its burst back towards the master, which by this time has enabled its receiver input. The burst repetition rate is thus 4 KHz.

LINE TRANSMIT SECTIONS

Alternate Mark Inversion (AMI) line coding, in which binary ''1''s are alternately transmitted as a positive pulse then a negative pulse, is used on each DASL line because of its spectral efficiency and null DC energy content. All transmitted bits, excluding the start bit, are scrambled by a 9-bit scrambler to provide good spectral spreading with a strong timing content. The scrambler feedback polynomial is: $X^9 + X^5 + 1$.



TL/H/11924–3

FIGURE 1. Burst Mode Timing on the Line

Functional Description (Continued)

Pulse shaping is obtained by means of a Digital to Analog Converter followed by a Continuous Smoothing Filter, in order to limit RF energy and crosstalk while minimizing Inter-Symbol Interference (ISI). *Figure 2* shows the pulse shape at the Lo output, while a template for the typical power spectrum transmitted to the line with random data is shown in *Figure 3*.

Each line-driver output, Lo0−Lo3, is designed to drive a transformer through a capacitor and termination resistor. A 1:1 transformer, terminated in 100Ω, results in signal amplitude of typically 1.3 Vpk on the line. Over-voltage protection must be included in each interface circuit.

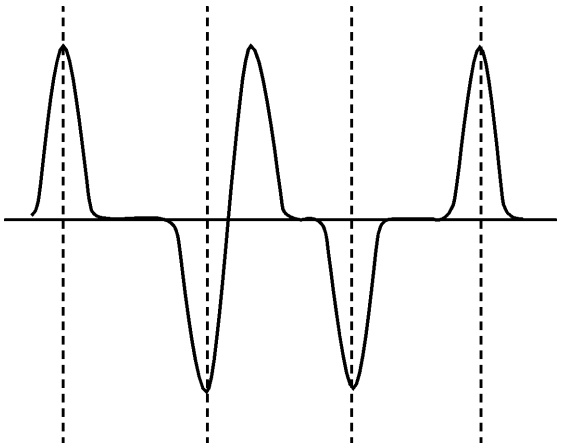
LINE RECEIVE SECTIONS

The input of each receive section, Li0−Li3, consists of a continuous anti-alias filter followed by a switched-capacitor low-pass filter designed to limit the noise bandwidth with minimum intersymbol interference. To correct pulse attenuation and distortion caused by the transmission line an AGC circuit and first-order equalizer adapt to the received pulse shape, thus restoring a ''flat'' channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

From the equalized output a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 4.096 MHz.

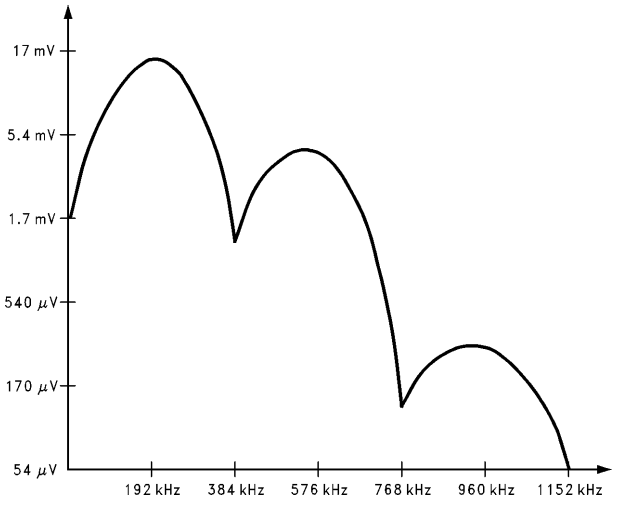
Following detection of the recovered symbols, the received data is de-scrambled by the same $X^9 + X^5 + 1$ polynomial and presented to the digital system interface circuit.

When a transmission line is de-activated, a Line-Signal Detect Circuit is enabled to detect the presence of incoming bursts if the far-end starts to activate the loop.



TL/H/11924–4

FIGURE 2. Typical AMI Waveform at Lo



TL/H/11924–5

FIGURE 3. Typical AMI Transmit Spectrum Measured at LO Output (With RGB = 100 Hz)

Functional Description (Continued)

ACTIVATION AND LOOP SYNCHRONIZATION

Activation (i.e. power-up and loop synchronization) may be initiated from either end of the loop. If the master (QDASL) end is activating the loop, it sends normal bursts of scrambled ''1''s which are detected by the slave's line-signal-detect circuitry. The slave then replies with bursts of scrambled ''1''s synchronized to the received bursts, and the Framing Detection circuit at each end searches for 4 consecutive correctly formatted receive bursts to acquire full loop synchronization. The QDASL receiver indicates when it is correctly in sync with received bursts by setting an indication in the Status Register and pulling the $\overline{INT}$ pin low.

For the slave end to initiate activation, it begins transmission of alternate bursts i.e., the burst repetition rate is 2 KHz, not 4 KHz. At this point the slave is running from its local oscillator and is not receiving any sync information from the master. When the master's Line-Signal Detect Circuit recognizes this ''wake-up'' signal, the appropriate QDASL line must be activated by writing to the Control Register. The master begins to transmit bursts synchronized, as normal, to the FS input with a 4 KHz repetition rate. This enables the slave's receiver to correctly identify burst timing from the master and to re-synchronize its own burst transmissions to those it receives. The Framing Detection Circuits then acquire full loop sync as described earlier.

Loop synchronization is considered to be lost if the Framing Detection Circuit does not find four framing marks of the four consecutive 4 KHz line frames. At this point an indication is set in the Status Register, the $\overline{INT}$ output is pulled low, and the receiver searches to re-acquire loop sync.

MICROWIRE CONTROL INTERFACE

A serial interface, which can be clocked independently from the B and D channel system interfaces, is provided for microcontroller access to the time-slot assignment, Control and Status Registers in the QDASL. The microcontroller is normally the timing master of this interface, and it supplies the CCLK and $\overline{CS}$ signals.

All data transfers consist of simultaneous read and write cycles, in which 2 continuous bytes are sampled on the CI pin, at the same time as 2 bytes are shifted out from the CO pin, see *Figure 6.* The first byte is a register address and the second is the data. To initiate a Microwire read/write cycle, $\overline{CS}$ must be pulled low for 16 cycles of CCLK. Data on CI is sampled on rising edges of CCLK, and shifted out from CO on failing edges. When $\overline{CS}$ is high, the CO pin is in the high-impedance TRI-STATE, enabling the CO pins of many devices to be multiplexed together.

Whenever a change (except Bipolar Violation) in any of the QDASL status conditions occurs, the Interrupt output $\overline{INT}$ is pulled low to alert the microprocessor to initiate a read cycle of the Status Register. This latched output is cleared when the read cycle is initiated.

Table 1 lists the address map of control functions and status indicators. Table 2 lists the addresses for the Control Registers for each QDASL line. Even-numbered addresses are read-write cycles, in which the data returned by the CO pin is previous contents of the addressed register. Odd-numbered addresses are readback commands only.

TABLE I. Global Register Address Map

Address (Hex)	Registers
00–0F	LINE 0 Control (TSX,TSR,CTRL)
10–1F	LINE 1 Control (TSX,TSR,CTRL)
20–2F	LINE 2 Control (TSX,TSR,CTRL)
30–3F	LINE 3 Control (TSX,TSR,CTRL)
40–CF	Not used
FF	Common Status Register for all lines (0–3). See Table VI

TABLE II. Per Line Control Register Address Map

Function	Byte 1								Byte 2 (Note 2)
	MSB Nibble (Note 1)				LSB Nibble				
	7	6	5	4	3	2	1	0	
Write TSXD Register	N				0	0	0	0	See Table V
Read TSXD Register	N				0	0	0	1	See Table V
Write TSXB1 Register	N				0	0	1	0	See Table IV
Read TSXB1 Register	N				0	0	1	1	See Table IV
Write TSXB2 Register	N				0	1	0	0	See Table IV
Read TSXB2 Register	N				0	1	0	1	See Table IV
Write TSRD Register	N				0	1	1	0	See Table V
Read TSRD Register	N				0	1	1	1	See Table V
Write TSRB1 Register	N				1	0	0	0	See Table IV
Read TSRB1 Register	N				1	0	0	1	See Table IV
Write TSRB2 Register	N				1	0	1	0	See Table IV
Read TSRB2 Register	N				1	0	1	1	See Table IV
Write Line Control Register (CTR L)	N				1	1	1	0	See Table III
Read Line Control Register (CTRL)	N				1	1	1	1	See Table III

Note 1: N = 0, 1, 2, or 3 in straight Binary notation for Line 0, 1, 2, or 3 respectively.

Note 2: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI and CO pins.

Functional Description (Continued)

LINE CONTROL REGISTERS CTRLN

Each of the 4 transceivers has a Line Control Register, CTRL0−CTRL3, which provides for control of loop activation, loopbacks, Interrupt enabling and D channel interface enabling. Table 3 lists the functions.

POWER ON INITIALIZATION

Following the initial application of power, the QDASL enters the power-down (de-activated) state, in which all the internal circuits are inactive and in a low power state except for a Line-Signal Detect Circuit for each of the 4 lines, and the necessary bias circuits. The 4 line outputs, Lo0−Lo3, are in a high impedance state and all digital outputs are inactive. All bits in the Line Control Registers power-up initially set to ''0''. While powered-down, each Line-Signal Detect Circuit continually monitors its line, to detect if the far-end initiates loop transmission.

POWER-UP/DOWN CONTROL

To power-up the device and initiate activation, bit C7 in any of the 4 Line Control Registers must be set high, see Table III. Setting C7 low de-activates the loop, or puts the channel in power-down state. During power-down state, internal register data is retained, and still can be accessed.

LOOPBACKS

Four different loopbacks can be set for each line. They are enabled and disabled by setting the corresponding bits in the Control Register, see Table III. In addition, a line must be activated to see the effect of loopback commands.

1. 2B + D Line Loopback

   When bit 5 is set to 1, this loop will transfer all three channels, B1, B2 and D, that are received at the Li pin back to the Lo pin. Data out on BO/DO is still the same as received at the Li input.

2. B1 Line Loopback

   When bit 4 is set high, the loop path is the same as (1) but only data on the B1 channel is looped back to the line. Transmit data in the B2 and D channels is from the Bi/DI pins.

3. B2 Line Loopback

   As (2) but for the B2 channel.

4. 2B + D Digital Loopback

   This loop will transfer all data (2B + D) received at BI/DI back to BO/DO. The data is also transmitted to the line.

TIME-SLOT ASSIGNMENT

The digital interface of the QDASL uses time-division multiplexing, with data framed in up to 64 possible 8-bit timeslots per 125 μs frame. Channels B1 and B2 for all 4 lines are clocked in (towards the line) at the BI pin and clocked out (from the line) at the BO pin. A separate port is provided for the D channel data for all 4 lines, which is clocked in on DI and out on DO. In addition to time-slot assignment, D channel data may be assigned into 2-bit sub-slots within each time slot, with up to 256 sub-slots per frame (with BCLK = 4.096 MHz). Each frame starts with the first positive edge of BCLK after the FS signal goes high, and counting of timeslots starts from zero at the beginning of the frame. *Figure 4* shows the timing, with some example timeslot assignments.

For each of the 4 QDASL lines there are 6 Time-Slot Assignment control registers, one each for transmit and receive B1, B2 and D channels. Selection of time-slots for transmit data into the BI or DI pin is made by writing the timeslot number (in Hex notation) into the appropriate TSX register. TSXB1 is the time-slot assignment for the transmit B1, TSXB2 is the time-slot assignment register for the transmit B2 channel and TSXD is the sub-slot assignment register for the transmit D channel.

TABLE III. Byte 2 of Control Register (CTRLN)

Bit Number								Function
7	6	5	4	3	2	1	0	
0 1								Deactivate Line Activate Line
	0 1							Disable Digital Loopback Enable 2B + D Digital Loopback
		0 1						Disable Line Loopback Enable 2B + D Line Loopback
			0 1					Disable B1 Line Loopback Enable B1 Line Loopback
				0 1				Disable B2 Line Loopback Enable B2 Line Loopback
					0 1			Disable Interrupt from this Line Enable Interrupt from this Line
						0 1		D Channel enabled from DO to Line D Channel disabled from DO to Line
							0 1	D Channel enabled from Line to DI D Channel disabled from Line to DI

Functional Description (Continued)

In the same manner the time-slot number should be written into the appropriate TSR registers for receive data at the BO and DO pins. TSRB1 is the time-slot assignment for the receive B1 channel, TSRB2 is the time-slot assignment register for the receive B2 channel and TSRD is the sub-slot assignment register for the receive D channel.

Whenever any receive time-slot is active at BO, the $\overline{TSB}$ output is also pulled low.

REGISTERS TSXB1, TSXB2, TSRB1, TSRB2

The data format for all B channel time-slot assignment registers is shown in Table IV.

Bit 7 Transparency Control: EB

This bit enables or disables data transparency between the digital interface and the line interface for the selected channel.

EB = 0 disables the channel.

EB = 1 enables the channel.

When the transmit direction (towards the line) is disabled there will be all ''ONE's'' (scrambled) as data for this channel at the Lo pin. If the receive direction (from the line) is disabled, BO will stay high impedance for the programmed time slot while, if it is enabled, data out on BO in the assigned time slot is the data from Li.

Bits 5–0: TS5–TS0

These bits define the binary number of the time-slot selected. Time-slots are numbered from 0–63. The frame sync signal is used as marker pulses for the beginning of time slot 0.

TABLE IV. Byte 2 of Register TSXB1, TSXB2, TSRB1 or TSRB2 for B Channel Time-Slot Assignment

Bit Number and Name								Function
7	6	5	4	3	2	1	0	
EB	X	TS5	TS4	TS3	TS2	TS1	TS0	
0	X	X	X	X	X	X	X	Disable B1 and/or B2
1	X	Assign One Binary Coded Time-Slot from 0–63						Enable B1 and/or B2

Note: If two B channels are erroneously assigned to the same time-slot, data out on Bo is not valid while data out on Lo is valid.

REGISTERS TXD, TRD

The data format for all D channel time-slot assignment registers is as follows:

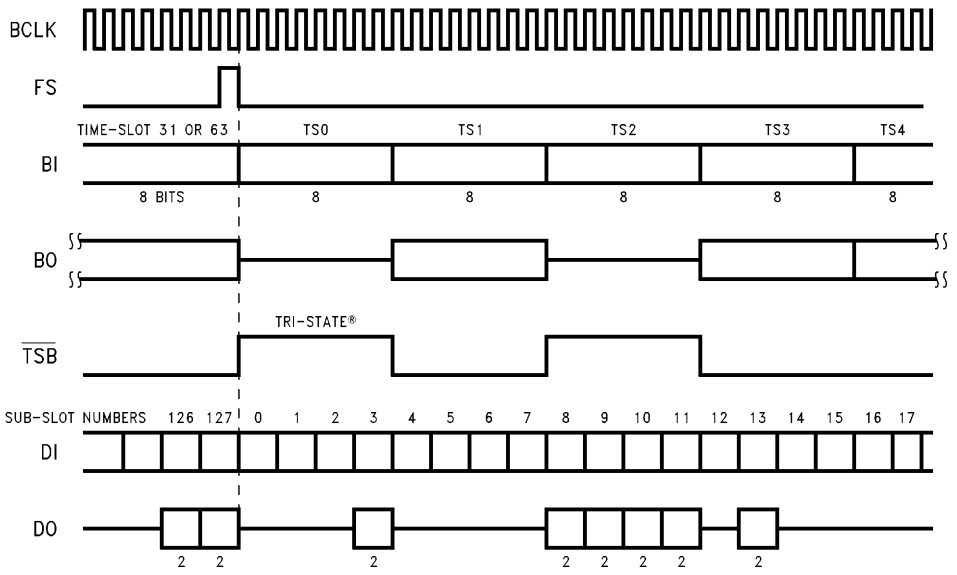
Data transparency between the digital interface and the line interface for the D channels can be controlled via the Channel Control Register, see Table III.

Bits 7–0: TS7–TS0

These bits define the binary number of the sub-slot selected. Sub-slots are numbered from 0–255. The frame sync signal is used as marker pulses for the beginning of Sub-slot 0.

TABLE V. Byte 2 of Register TSXD or TSRD for D Channel Time-Slot Assignment

Bit Number and Name							
7	6	5	4	3	2	1	0
SS 7	SS 6	SS 5	SS 4	SS 3	SS 2	SS 1	SS 0
Assign One Binary Coded Sub-Slot from 0–255 for D Channel							



TL/H/11924–6

FIGURE 4. QDASL Digital Interface Timing

Functional Description (Continued)

TABLE VI. Status Register Functions

Byte 2								Indication
7	6	5	4	3	2	1	0	
0	0							Line 3: deactivated
0	1							Line 3: line signal present but not in sync
1	0							Line 3: activated, bipolar violation (Note 1)
1	1							Line 3: activated, no bipolar violation
		0	0					Line 2: deactivated
		0	1					Line 2: line signal present but not in sync
		1	0					Line 2: activated, bipolar violation (Note 1)
		1	1					Line 2: activated, no bipolar violation
				0	0			Line 1: deactivated
				0	1			Line 1: line signal present but not in sync
				1	0			Line 1: activated, bipolar violation (Note 1)
				1	1			Line 1: activated, no bipolar violation
						0	0	Line 0: deactivated
						0	1	Line 0: line signal present but not in sync
						1	0	Line 0: activated, bipolar violation (Note 1)
						1	1	Line 0: activated, no bipolar violation

Note 1: Bipolar Violation does not cause an Interrupt.

STATUS REGISTER

Status information for all 4 channels may be read from the common Status Register by addressing location X'FF. 2 bits per line are coded as shown in Table VI. A change in the status of 1 or more lines is indicated by the $\overline{INT}$ pin being pulled low, provided bit 2 of the corresponding control register is set to ''ONE'' to enable the interrupt for that line.

BIPOLAR VIOLATION DETECTOR

On an activated line, whenever a line error is received there will be a violation of the AMI coding rule. This is reported by setting the code 10 for that line. The violation indication is cleared to 11 after a read of the Status Register.

As an example of the interpretation of the Status Register contents, if the byte 2 read back from the Status Register = 00111001 (= X'39), this indicates the following status of the 4 lines: line 3 is deactivated; line 2 is in sync with no error since the last read cycle; line 1 is in sync but there has been 1 or more errors since the last read cycle of the Status Register; line 0 is receiving a line signal but the line transmission is not synchronized.

Applications Information

POWER SUPPLIES

While the pins of the TP3404 QDASL device are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, the VDDA and VDDD pins should be connected together via the shortest possible trace; likewise the GNDA and GNDD pins must be connected together. These two connections can be done directly underneath the part. All other ground connections to each device should meet at a common point as close as possible to the GNDD pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 μF should be connected from this common point to VDDD as close as possible to the device pins.

Figure 5 shows a typical 4 line application of the QDASL. The current list of suitable commercial transformers is:

Schott Corporation (Nashville);
Phone 615-889-8800.

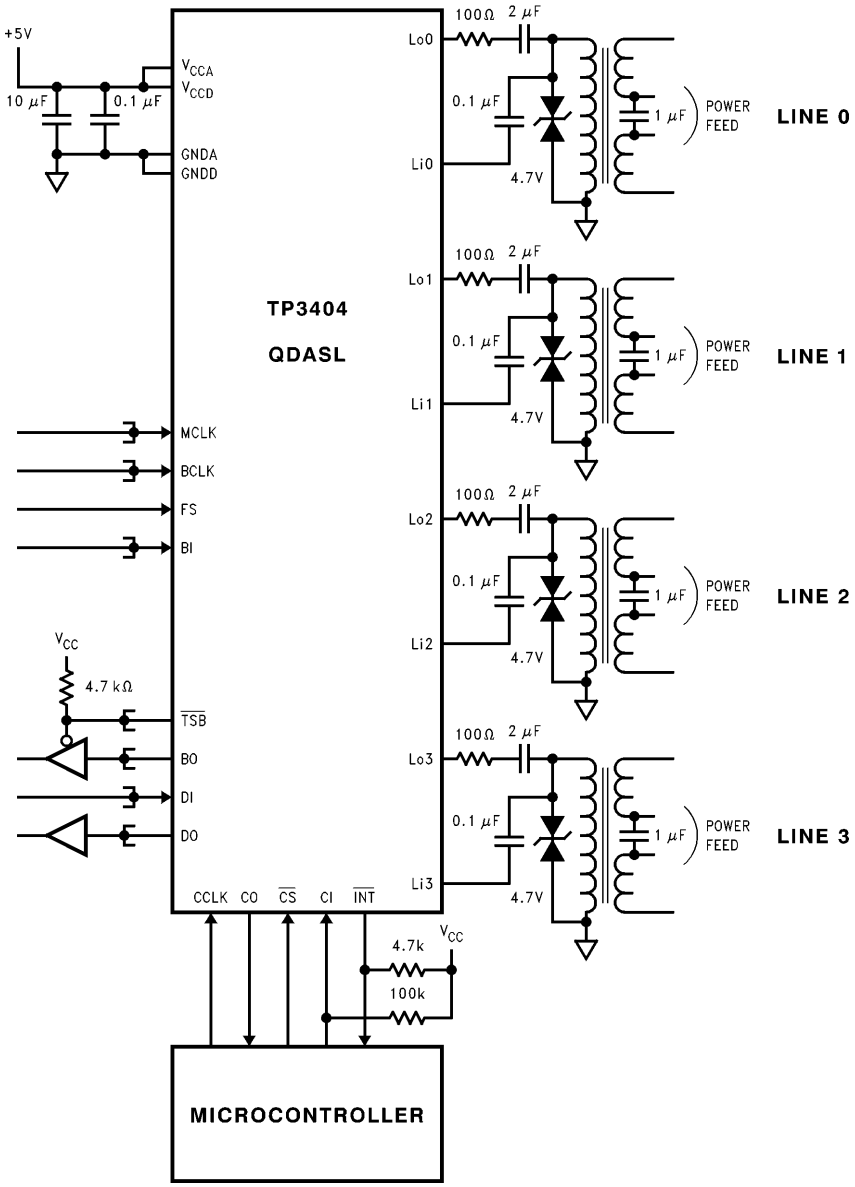
Part numbers: 67110850 (dry);
67110860 (50 mA DC).

Pulse Engineering (San Diego);
Phone 619-674-8100.

Part number: TBD.

Note that the zener diode protection shown in *Figure 8* is only intended as secondary protection for inside wiring applications; primary protection is also necessary. Further information can be found in the datasheet for the TP3401/2/3 DASL devices and in Application Note AN-509 ''Using the TP3401/2/3 ISDN PBX Transceivers''.

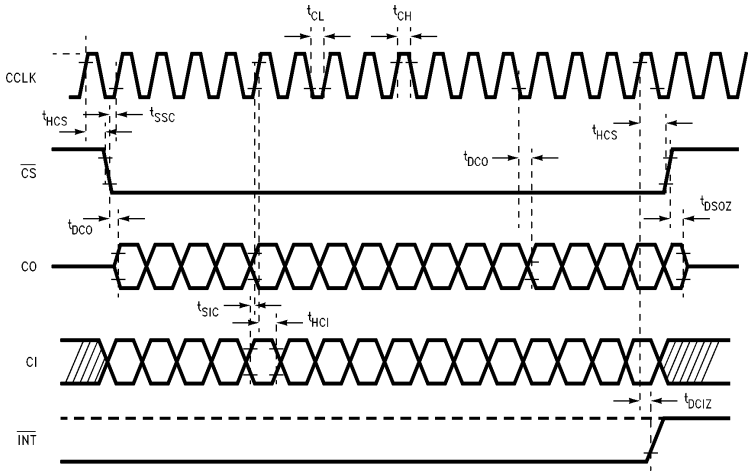
Applications Information (Continued)



TL/H/11924–7

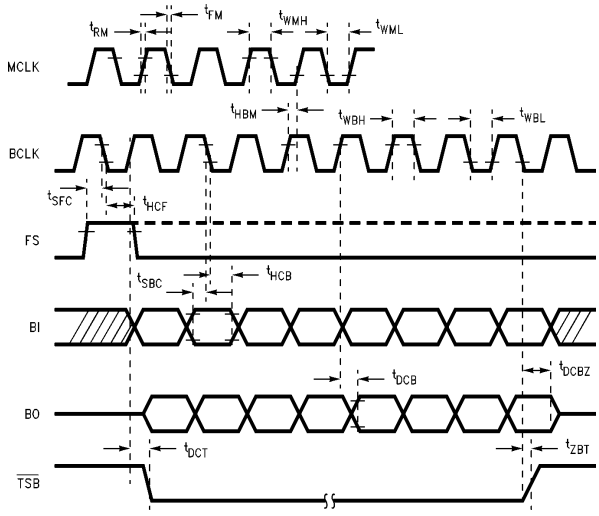
FIGURE 5. Typical Application

Applications Information (Continued)



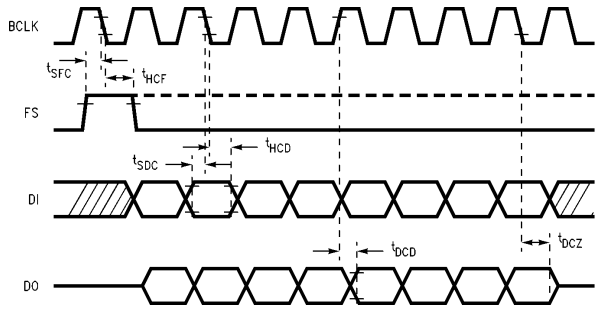
TL/H/11924–8

FIGURE 6. Microwire Control Interface Timing Details



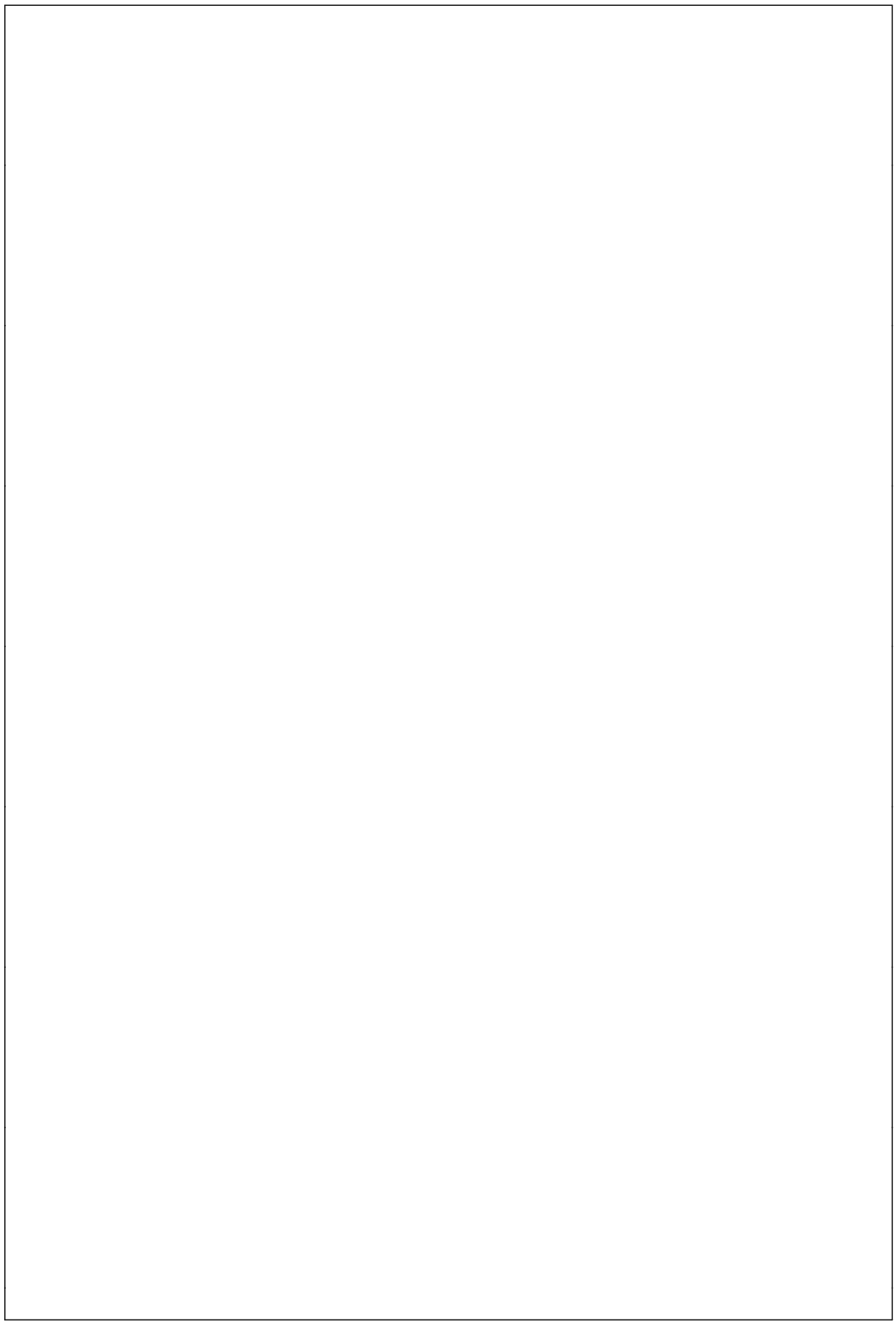
TL/H/11924–9

FIGURE 7. B Channel Digital Interface Details

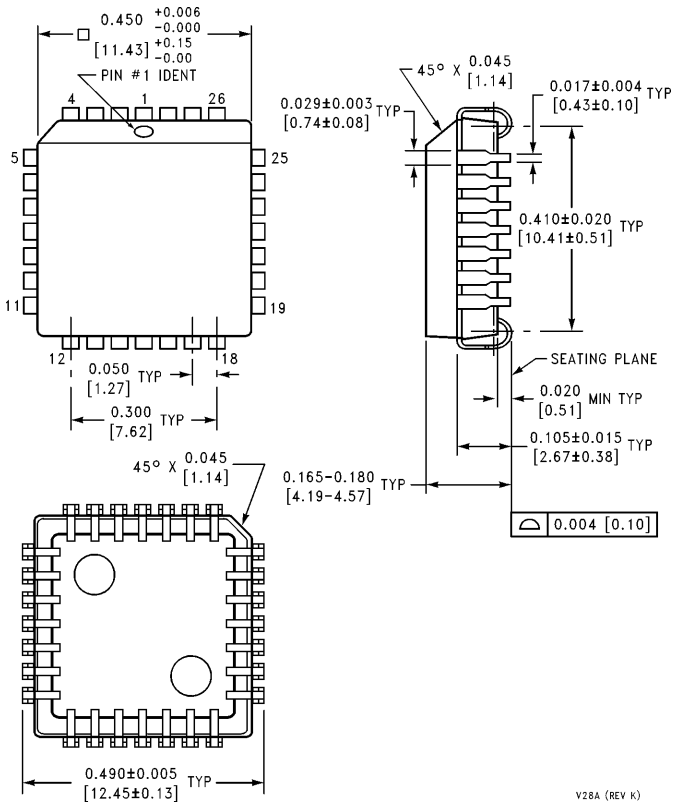


TL/H/11924–10

FIGURE 8. D-Channel Digital Interface Timing Details



Physical Dimensions inches (millimeters)



Plastic Chip Carrier (V)
Order Number TP3404V
NS Package Number V28A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408