National Semiconductor

CLC450
Single Supply, Low-Power, High Output, Current Feedback Amplifier

General Description

The CLC450 has a new output stage that delivers high output drive current (100mA), but consumes minimal quiescent supply current (1.5mA) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3dB frequency.

The CLC450 offers superior dynamic performance with a 100MHz small-signal bandwidth, 280V/µs slew rate and 6.1ns rise/fall times ($2V_{step}$). The combination of low quiescent power, high output current drive, and high-speed performance make the CLC450 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC450 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC450 will drive a 100Ω load with only -75/-64dBc second/third harmonic distortion (A_V = +2, V_{out} = $2V_{pp}$, f = 1MHz). With a 25Ω load, and the same conditions, it produces only -70/-60dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution A/D converters, the CLC450 provides excellent -79/-75dBc second/third harmonic distortion (A_V = +2, V_{out} = $2V_{pp}$, f = 1MHz, R_L = 1kΩ) and fast settling time.

Available in SOT23-5, the CLC450 is ideal for applications where space is critical.

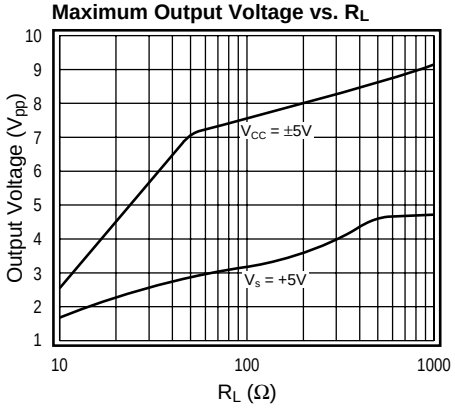
Features

- 100mA output current
- 1.5mA supply current
- 100MHz bandwidth (A_V = +2)
- -79/-75dBc HD2/HD3 (1MHz)
- 20ns settling to 0.05%
- 280V/µs slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V to ±5V supplies
- Available in Tiny SOT23-5 package

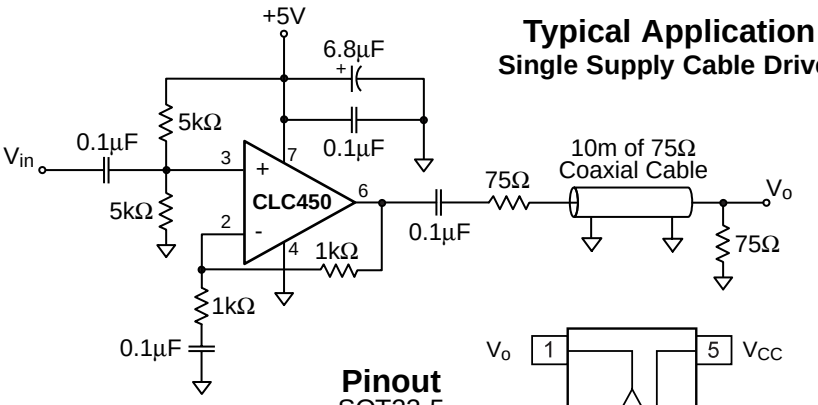
Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery-powered applications
- A/D driver

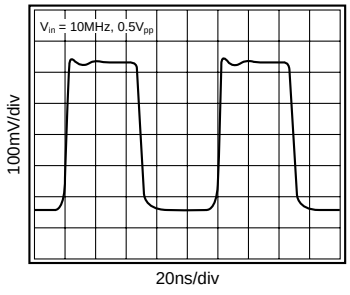
Maximum Output Voltage vs. R_L



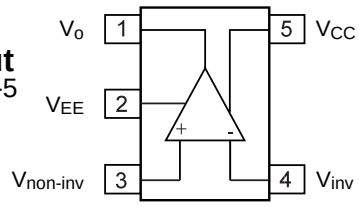
Typical Application
Single Supply Cable Driver



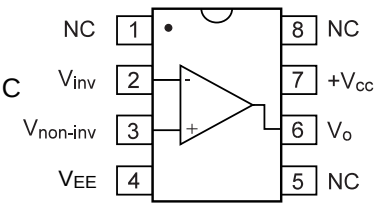
Response After 10m of Cable



Pinout
SOT23-5



Pinout
DIP & SOIC



+5V Electrical Characteristics (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_s = +5V[1], V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC450AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_o < 0.5V_{pp}	100	85	75	70	MHz	
	V_o < 2.0V_{pp}	75	60	55	50	MHz	
-0.1dB bandwidth	V_o < 0.5V_{pp}	30	25	20	20	MHz	
gain peaking	<200MHz, V_o = 0.5V_{pp}	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, V_o = 0.5V_{pp}	0.1	0.3	0.4	0.5	dB	
linear phase deviation	<30MHz, V_o = 0.5V_{pp}	0.2	0.4	0.5	0.5	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	6.1	8.5	9.2	10.0	ns	
settling time to 0.05%	1V step	20	30	50	80	ns	
overshoot	2V step	16	20	22	22	%	
slew rate	2V step	280	200	185	170	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-75	–	–	–	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-79	–	–	–	dBc	
	2V_{pp}, 5MHz	-62	-58	-57	-56	dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-64	–	–	–	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-75	–	–	–	dBc	
	2V_{pp}, 5MHz	-52	-48	-46	-46	dBc	
equivalent input noise							
voltage (e_{ni})	>1MHz	3.0	3.7	4.0	4.0	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	6.9	9	10	10	pA/√Hz	
inverting current (i_{bi})	>1MHz	8.5	11	12	12	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1	4	5	6	mV	A
average drift		7	–	15	15	µV/°C	
input bias current (non-inverting)		5	12	15	16	µA	A
average drift		25	–	60	60	nA/°C	
input bias current (inverting)		3	10	12	13	µA	A
average drift		10	–	20	20	nA/°C	
power supply rejection ratio	DC	54	50	48	48	dB	
common-mode rejection ratio	DC	51	47	45	45	dB	
supply current	R_L = ∞	1.5	1.7	1.8	1.8	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.46	0.37	0.33	0.33	MΩ	
input capacitance (non-inverting)		1.5	2.3	2.3	2.3	pF	
input voltage range, High		4.2	4.1	4.1	4.0	V	
input voltage range, Low		0.8	0.9	0.9	1.0	V	
output voltage range, High	R_L = 100Ω	4.0	3.9	3.9	3.8	V	
output voltage range, Low	R_L = 100Ω	1.0	1.1	1.1	1.2	V	
output voltage range, High	R_L = ∞	4.1	4.0	4.0	3.9	V	
output voltage range, Low	R_L = ∞	0.9	1.0	1.0	1.1	V	
output current		100	80	65	40	mA	B
output resistance, closed loop	DC	55	90	90	120	mΩ	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

A) J-level: spec is 100% tested at +25°C.
B) The short circuit current can exceed the maximum safe output current.
1) $V_s = V_{CC} - V_{EE}$

Reliability Information

Transistor Count	49
MTBF (based on limited test data)	31Mhr

Absolute Maximum Ratings

supply voltage (V_{CC} - V_{EE})	+14V
output current (see note C)	140mA
common-mode input voltage	V_{EE} to V_{CC}
maximum junction temperature	+150°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	500V

±5V Electrical Characteristics (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_{CC} = ±5V, unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC450AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_o < 1.0V_{pp}	135	115	105	100	MHz	
	V_o < 4.0V_{pp}	55	45	42	40	MHz	
-0.1dB bandwidth	V_o < 1.0V_{pp}	40	30	25	25	MHz	
gain peaking	<200MHz, V_o = 1.0V_{pp}	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, V_o = 1.0V_{pp}	0.1	0.3	0.4	0.5	dB	
linear phase deviation	<30MHz, V_o = 1.0V_{pp}	0.1	0.3	0.4	0.4	deg	
differential gain	NTSC, R_L=150Ω	0.03	–	–	–	%	
differential phase	NTSC, R_L=150Ω	0.3	–	–	–	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	4.4	5.8	6.2	6.8	ns	
settling time to 0.05%	2V step	15	25	40	60	ns	
overshoot	2V step	15	20	22	22	%	
slew rate	2V step	370	280	260	240	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-86	–	–	–	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-85	–	–	–	dBc	
	2V_{pp}, 5MHz	-68	-64	-61	-60	dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-65	–	–	–	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-74	–	–	–	dBc	
	2V_{pp}, 5MHz	-52	-48	-46	-46	dBc	
equivalent input noise							
voltage (e_{ni})	>1MHz	3.0	3.7	4.0	4.0	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	6.9	9	10	10	pA/√Hz	
inverting current (i_{bi})	>1MHz	8.5	11	12	12	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		2	6	7	8	mV	
average drift		8	–	20	20	µV/°C	
input bias current (non-inverting)		5	12	16	17	µA	
average drift		40	–	70	70	nA/°C	
input bias current (inverting)		5	13	15	16	µA	
average drift		20	–	45	45	nA/°C	
power supply rejection ratio	DC	56	51	49	49	dB	
common-mode rejection ratio	DC	53	48	46	46	dB	
supply current	R_L= ∞	1.6	1.9	2.0	2.0	mA	
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.62	0.50	0.45	0.45	MΩ	
input capacitance (non-inverting)		1.2	1.8	1.8	1.8	pF	
common-mode input range		±4.2	±4.1	±4.1	±4.0	V	
output voltage range	R_L = 100Ω	±3.8	±3.6	±3.6	±3.5	V	
output voltage range	R_L = ∞	±4.0	±3.8	±3.8	±3.7	V	
output current		130	100	80	50	mA	B
output resistance, closed loop	DC	40	70	70	90	mΩ	

Notes

B) The short circuit current can exceed the maximum safe output current.

Package Thermal Resistance

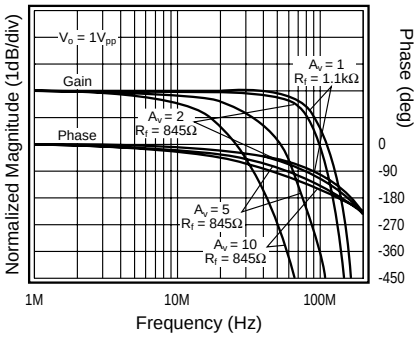
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	115°C/W	125°C/W
Surface Mount (AJE)	130°C/W	150°C/W
Surface Mount (AJM5)	140°C/W	210°C/W
Dice (ALC)	25°C/W	–

Ordering Information

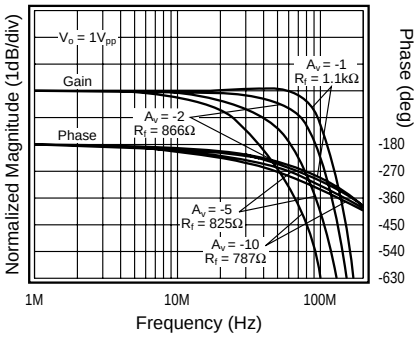
Model	Temperature Range	Description
CLC450AJP	-40°C to +85°C	8-pin PDIP
CLC450AJE	-40°C to +85°C	8-pin SOIC
CLC450AJM5	-40°C to +85°C	5-pin SOT
CLC450ALC	-40°C to +85°C	dice

+5V Typical Performance (A_V = +2, R_f = 1kΩ, R_L = 100Ω, V_s = +5V[1], V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

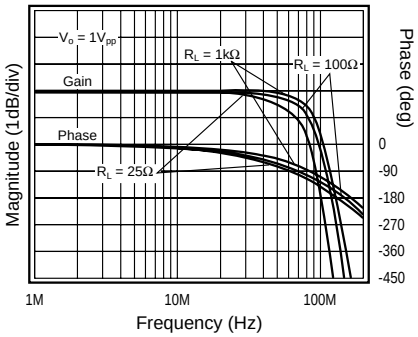
Non-Inverting Frequency Response



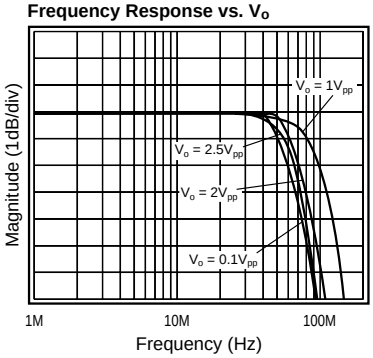
Inverting Frequency Response



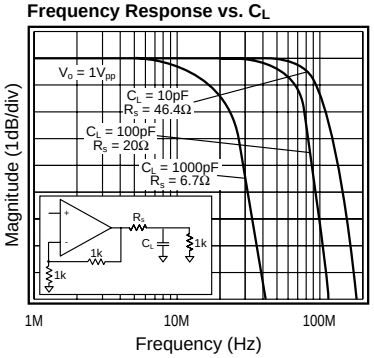
Frequency Response vs. R_L



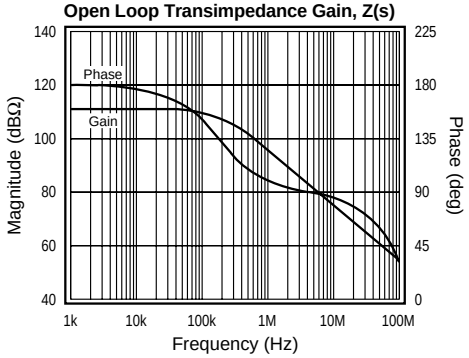
Frequency Response vs. V_o



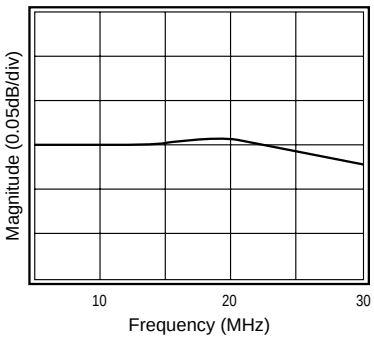
Frequency Response vs. C_L



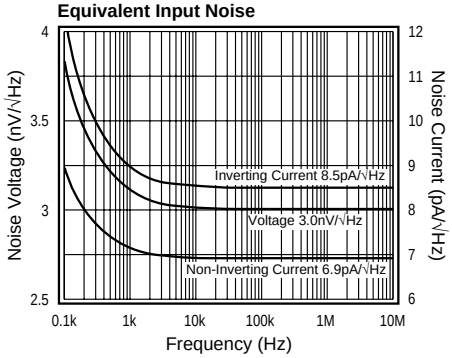
Open Loop Transimpedance Gain, Z(s)



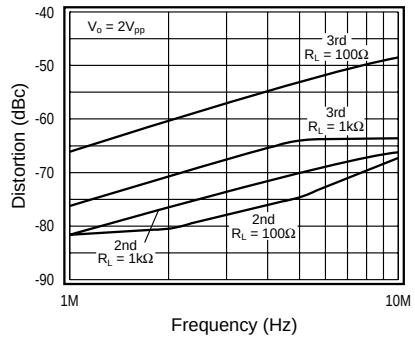
Gain Flatness



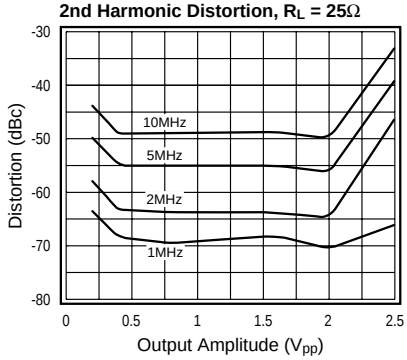
Equivalent Input Noise



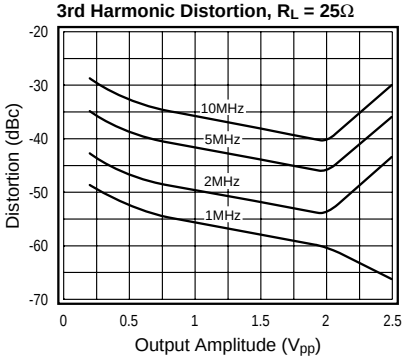
2nd & 3rd Harmonic Distortion



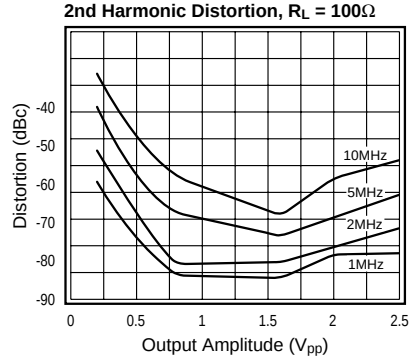
2nd Harmonic Distortion, R_L = 25Ω



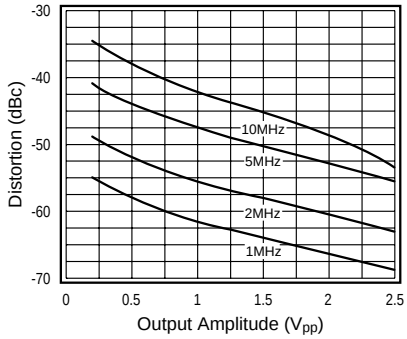
3rd Harmonic Distortion, R_L = 25Ω



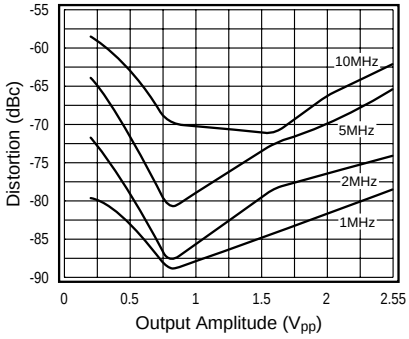
2nd Harmonic Distortion, R_L = 100Ω



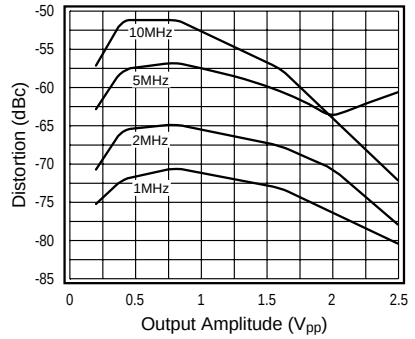
3rd Harmonic Distortion, R_L = 100Ω



2nd Harmonic Distortion, R_L = 1kΩ

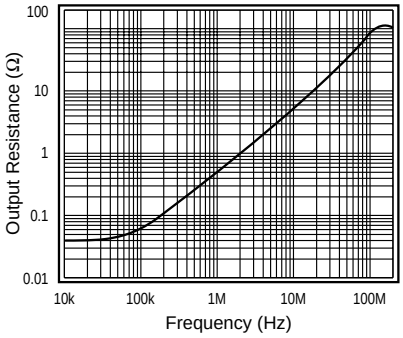


3rd Harmonic Distortion, R_L = 1kΩ

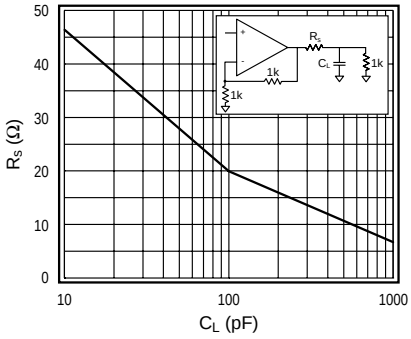


+5V Typical Performance (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_s = + 5V[1], V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

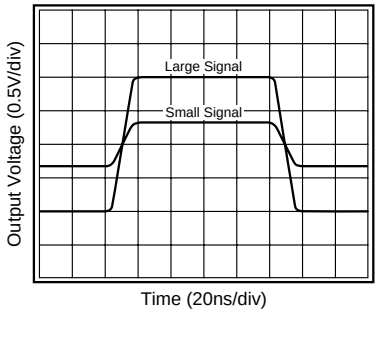
Closed Loop Output Resistance



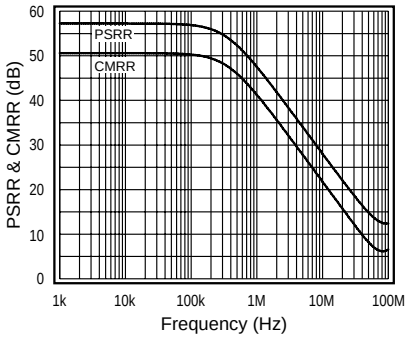
Recommended R_S vs. C_L



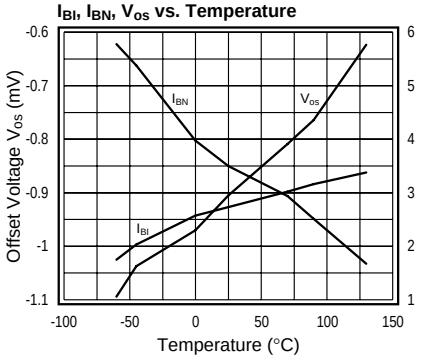
Large & Small Signal Pulse Response



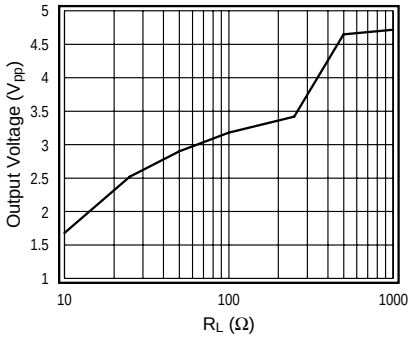
PSRR & CMRR



I_{BI}, I_{BN}, V_{os} vs. Temperature

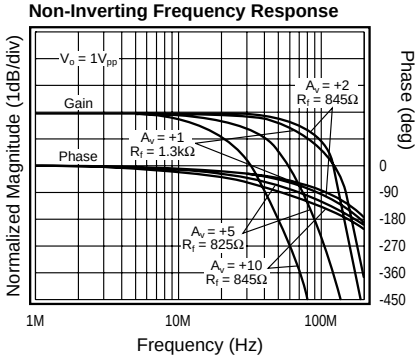


Maximum Output Voltage vs. R_L

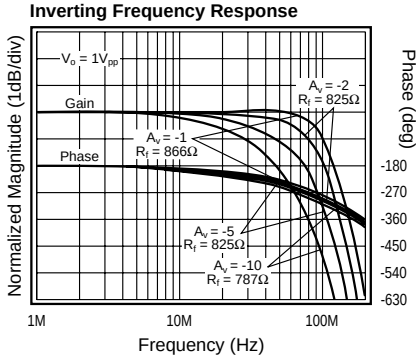


±5V Typical Performance (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_{CC} = ± 5V, unless specified)

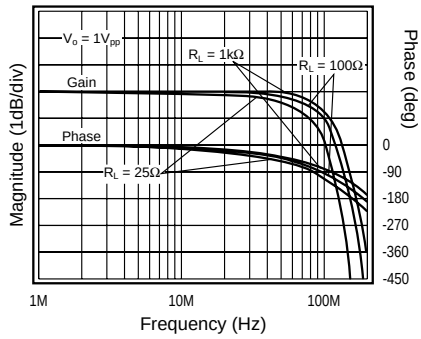
Non-Inverting Frequency Response



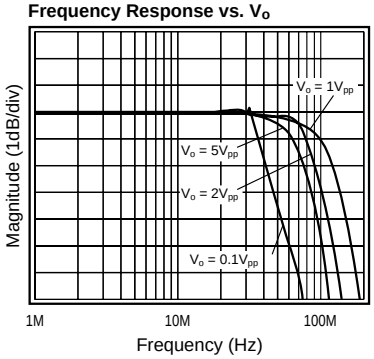
Inverting Frequency Response



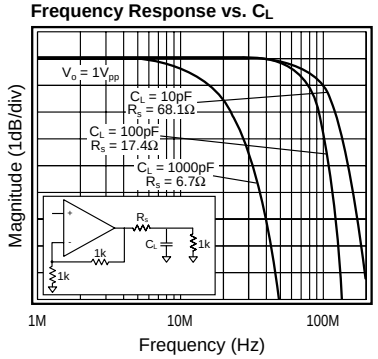
Frequency Response vs. R_L



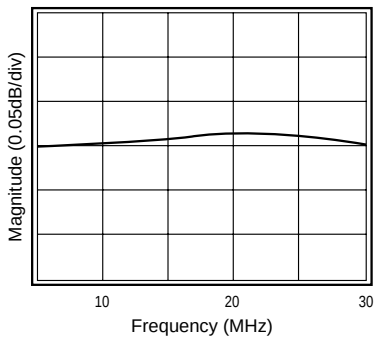
Frequency Response vs. V_o



Frequency Response vs. C_L

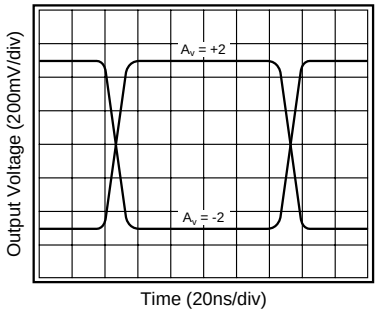


Gain Flatness

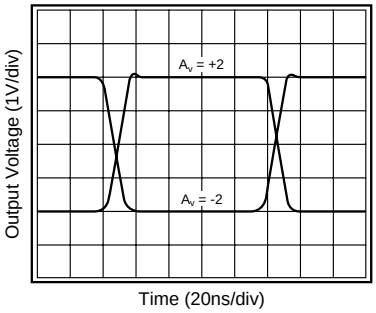


±5V Typical Performance (A_V = +2, R_f = 1kΩ, R_L = 100Ω, V_s = +5V[1], V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

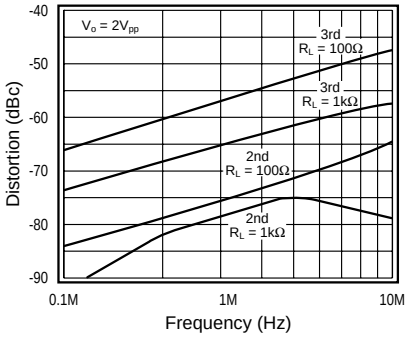
Small Signal Pulse Response



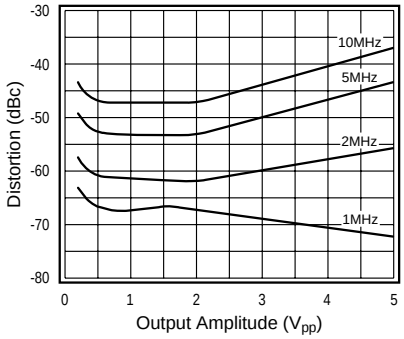
Large Signal Pulse Response



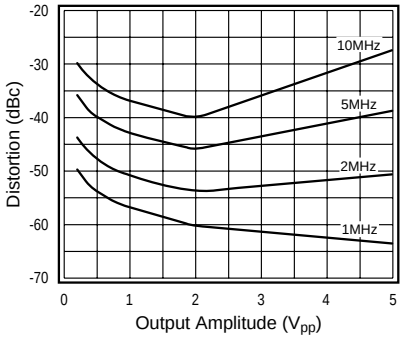
2nd & 3rd Harmonic Distortion



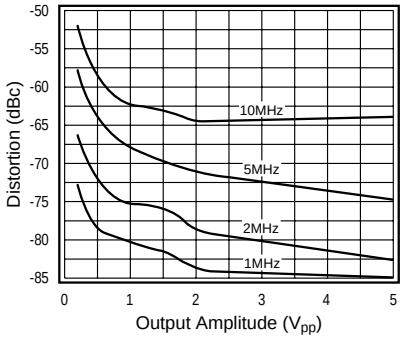
2nd Harmonic Distortion, R_L = 25Ω



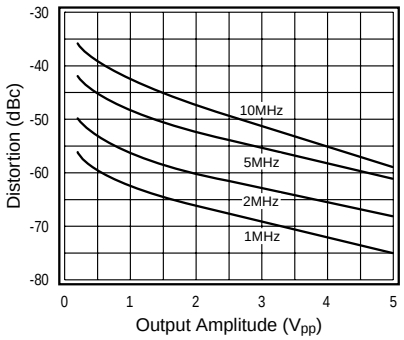
3rd Harmonic Distortion, R_L = 25Ω



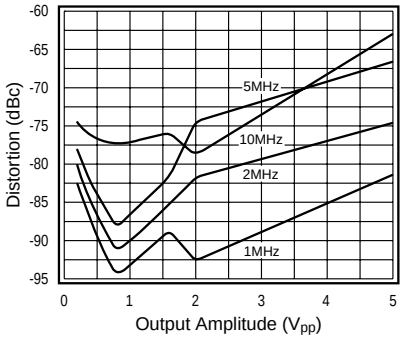
2nd Harmonic Distortion, R_L = 100Ω



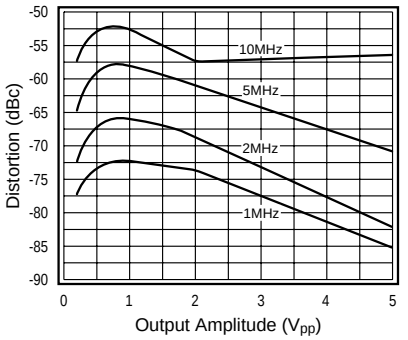
3rd Harmonic Distortion, R_L = 100Ω



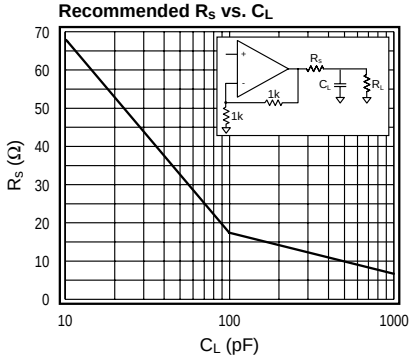
2nd Harmonic Distortion, R_L = 1kΩ



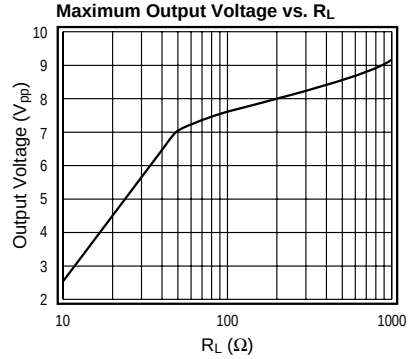
3rd Harmonic Distortion, R_L = 1kΩ



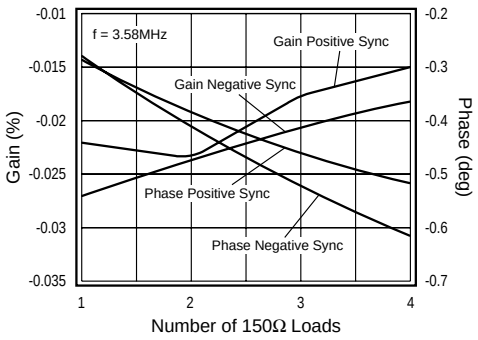
Recommended R_S vs. C_L



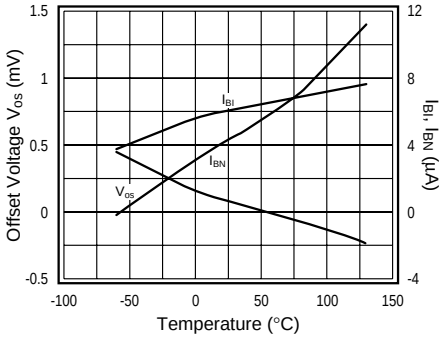
Maximum Output Voltage vs. R_L



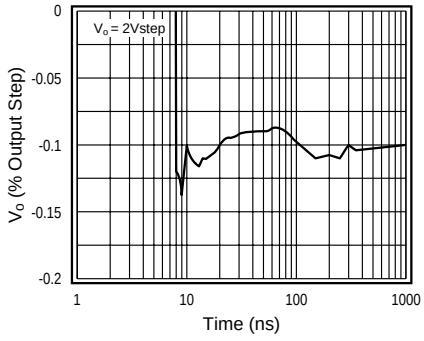
Differential Gain & Phase



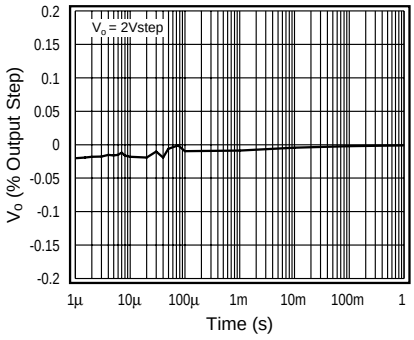
I_{BI}, I_{BN}, V_{OS} vs. Temperature



Short Term Settling Time



Long Term Settling Time



CLC450 OPERATION

The CLC450 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC450 operates from a single 5V supply or dual ±5V supplies. Operating from a single supply, the CLC450 has the following features:

- Provides 100mA of output current while consuming 7.5mW of power
- Offers low -79/-75dB 2nd and 3rd harmonic distortion
- Provides BW > 60MHz and 1MHz distortion < -65dBc at $V_o = 2.5V_{pp}$

The CLC450 performance is further enhanced in ±5V supply applications as indicated in the ***±5V Electrical Characteristics*** table and ***±5V Typical Performance*** plots.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \qquad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC450's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the ***Feedback Resistor Selection*** section for more details on selecting a feedback resistor value.

CLC450 DESIGN INFORMATION

Single Supply Operation (V_{CC} = +5V, V_{EE} = GND)

The specifications given in the ***+5V Electrical Characteristics*** table for single supply operation are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC450 is typically +0.8V to +4.2V. The typical output range with R_L=100Ω is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figures 1 and 2 show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

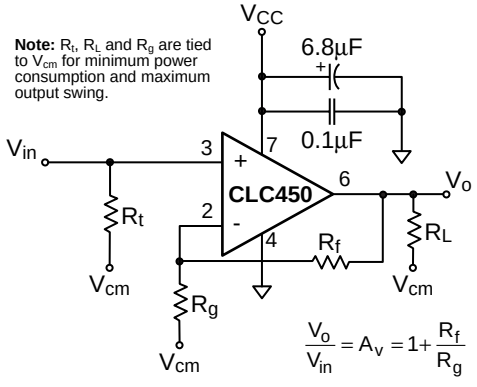


Figure 1: Non-Inverting Configuration

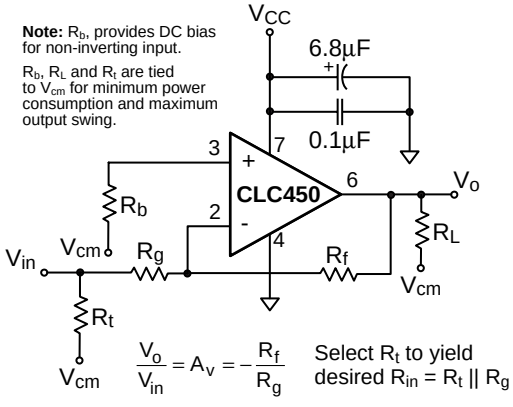
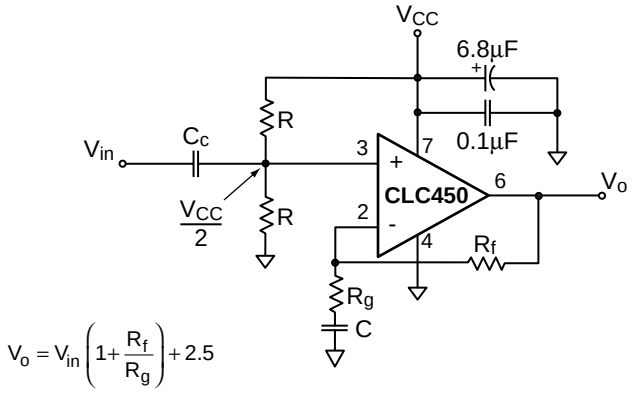


Figure 2: Inverting Configuration

AC Coupled Single Supply Operation

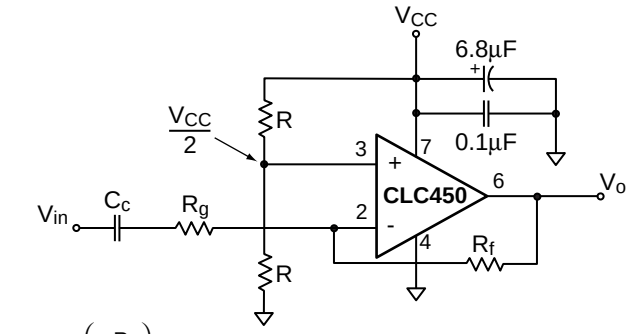
Figures 3 and 4 show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For $V_{CC} = +5V$).



$$V_o = V_{in}\left(1+\frac{R_f}{R_g}\right)+2.5$$

$$\text{low frequency cutoff} = \frac{1}{2\pi R_{in} C_c}, \text{ where: } R_{in} = \frac{R}{2} \qquad R >> R_{source}$$

Figure 3: AC Coupled Non-Inverting Configuration



$$V_o = V_{in}\left(-\frac{R_f}{R_g}\right)+2.5$$

$$\text{low frequency cutoff} = \frac{1}{2\pi R_g C_c}$$

Figure 4: AC Coupled Inverting Configuration

Dual Supply Operation

The CLC450 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 5 and 6.

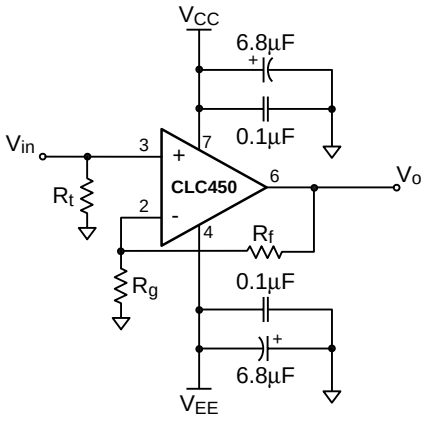


Figure 5: Dual Supply Non-Inverting Configuration

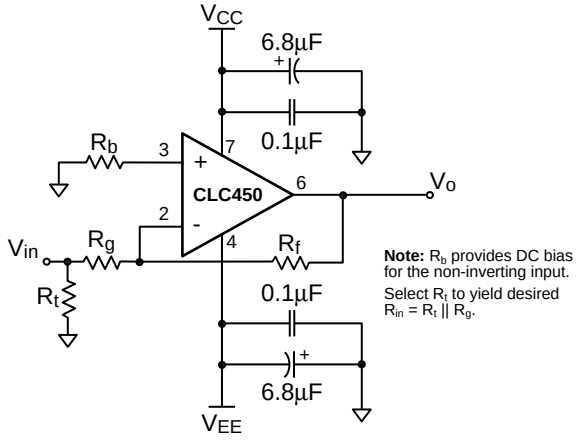


Figure 6: Dual Supply Inverting Configuration

Feedback Resistor Selection

The feedback resistor, R_f, affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC450, at a gain of +2V/V, is achieved with R_f equal to 1kΩ. The frequency response plots in the ***Typical Performance*** sections illustrate the recommended R_f for several gains. These recommended values of R_f provide the maximum bandwidth with minimal peaking. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increase R_f to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended R_f is doubled, then the bandwidth will be cut in half.

Unity Gain Operation

The recommended R_f for unity gain (+1V/V) operation is 1.5kΩ. R_g is left open. Parasitic capacitance at the inverting node may require a slight increase in R_f to maintain a flat frequency response.

Bandwidth vs. Output Amplitude

The bandwidth of the CLC450 is at a maximum for output voltages near $1V_{pp}$. The bandwidth decreases for smaller and larger output amplitudes. Refer to the ***Frequency Response vs. V_o*** plots.

Load Termination

The CLC450 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm}.

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC450 will improve stability and settling performance. The ***Frequency Response vs. C_L*** and ***Recommended R_s vs. C_L*** plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 7 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

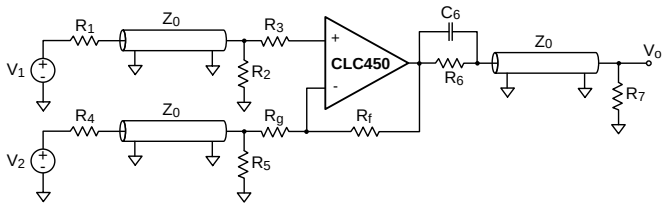


Figure 7: Transmission Line Matching

Non-inverting gain applications:

- Connect R_g directly to ground.
- Make R_1, R_2, R_6, and R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_o.
- Make R_5 II $R_g = Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Power Dissipation

Follow these steps to determine the power consumption of the CLC450:

1. Calculate the quiescent (no-load) power: $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage: $P_o = (V_{CC} - V_{load}) (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power: $P_t = P_{amp} + P_o$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in Figure 8. The power derating curve for any CLC450 package can be derived by utilizing the following equation:

$$\frac{(175° - T_{amb})}{\theta_{JA}}$$

where

T_{amb} = Ambient temperature (°C)

θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

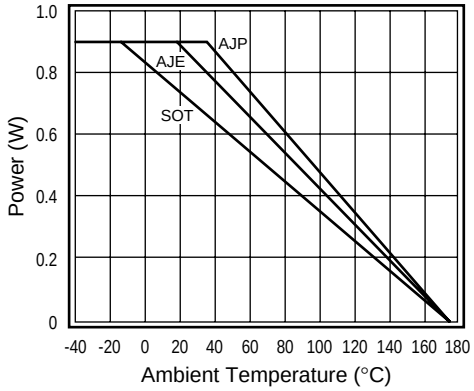


Figure 8: Power Derating Curves

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC450 (730013-DIP, 730027-SOIC, 730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information

Data sheets are available for the CLC730013/ CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of National's high speed amplifiers. This table for the CLC450 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

Components Needed to Evaluate the CLC450 on the Evaluation Board:

- R_f, R_g - Use this product data sheet to select values
- R_{in}, R_{out} - Typically 50Ω (Refer to the ***Basic Operation*** section of the evaluation board data sheet for details)

- R_t - Optional resistor for inverting gain configurations (Select R_t to yield desired input impedance = $R_g \parallel R_t$)
- C_1, C_2 - 0.1µF ceramic capacitors
- C_3, C_4 - 6.8µF tantalum capacitors

Components not used:

- C_5, C_6, C_7, C_8
- R_1 thru R_8

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

Single Supply Cable Driver

The typical application shown on the front page shows the CLC450 driving 10m of 75Ω coaxial cable. The CLC450 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o.

Single Supply Lowpass Filter

Figures 9 and 10 illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine R_1, R_2, C_1, and C_2 based on the desired Q and corner frequency.

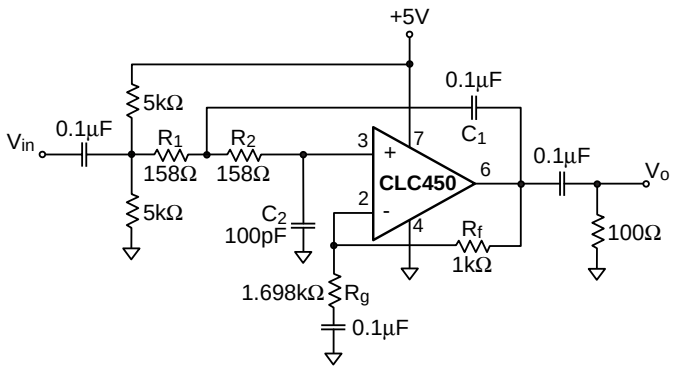


Figure 9: Lowpass Filter Topology

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1-K)\sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3-K)}$$

Figure 10: Design Equations

This example illustrates a lowpass filter with Q = 0.707 and corner frequency f_c = 10MHz. A Q of 0.707 was chosen to achieve a maximally flat, Butterworth response. Figure 11 indicates the filter response.

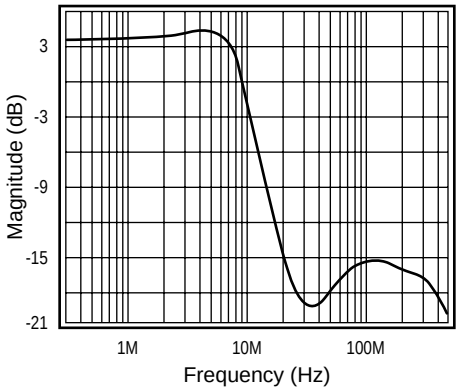


Figure 11: Lowpass Response

Twisted Pair Driver

The high output current and low distortion, of the CLC450, make it well suited for driving transformers. Figure 12 illustrates a typical twisted pair driver utilizing the CLC450 and a transformer. The transformer provides the signal and its inversion for the twisted pair.

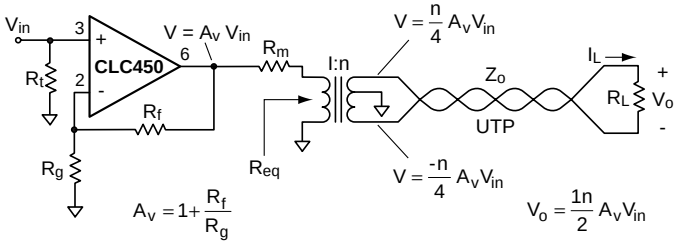


Figure 12: Twisted Pair Driver

To match the line's characteristic impedance (Z_o) set:

- $R_L = Z_o$
- $R_m = R_{eq}$

Where R_{eq} is the transformed value of the load impedance, (R_L), and is approximated by:

$$R_{eq} = \frac{R_L}{n^2}$$

Select the transformer so that it loads the line with a value close to Z_o, over the desired frequency range. The output impedance, R_o, of the CLC450 varies with frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of R_o.

$$\text{Return Loss(dB)} \approx -20\log_{10}\left|n^2 \cdot \frac{R_o}{Z_o}\right|$$

The load current (I_L) and voltage (V_o) are related to the CLC450's maximum output voltage and current by:

$$|V_o| \leq n \cdot V_{max}$$

$$|I_L| \leq \frac{I_{max}}{n}$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

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1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
2501 Miramar Tower
1-23 Kimberley Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408