National Semiconductor

October 1995

74LVX4245
8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

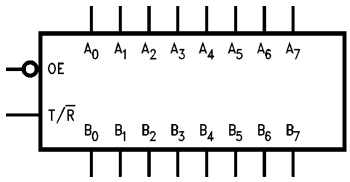
The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

Features

- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A port and 3V data flow at B port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Functionally compatible with the 74 series 245

Logic Symbol



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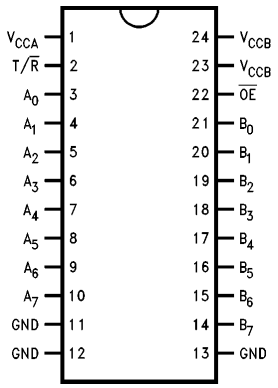
Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



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	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX4245WM 74LVX4245WMX	74LVX4245QSC 74LVX4245QSCX	74LVX4245MTC 74LVX4245MTCX
See NS Package Number	M24B	MQA24	MTC24

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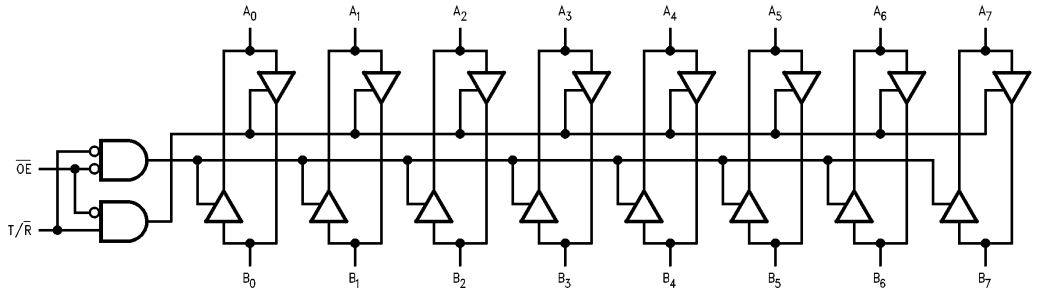
Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A(n)	−0.5V to V_{CCA} + 0.5V
@ B(n)	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±200 mA
@ I_{CCB}	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage	
V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 3.6V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@ A(n)	0V to V_{CCA}
@ B(n)	0V to V_{CCB}
Free Air Operating Temperature (T_A)	
74LVX	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVX4245 T_A +25°C	74LVX4245 T_A = −40°C to +85°C		Units	Conditions
					Typ	Guaranteed Limits			
V_{IHA}	Minimum High Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.3		2.0	2.0	V	$V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ − 0.1V
			4.5	3.3		2.0	2.0		
V_{IHB}		B(n)	5.0	3.6		2.0	2.0		
			5.0	2.7		2.0	2.0		
V_{ILA}	Maximum Low Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.3		0.8	0.8	V	$V_{OUT} \leq$ 0.1V or $\geq V_{CC}$ −0.1V
			4.5	3.3		0.8	0.8		
V_{ILB}		B(n)	5.0	2.7		0.8	0.8		
			5.0	3.6		0.8	0.8		
V_{OHA}	Minimum High Level Output Voltage		4.5	3.0	4.5	4.4	4.4	V	I_{OUT} = −100 μA
			4.5	3.0	4.25	3.86	3.76		I_{OH} = −24 mA
V_{OHB}			4.5	3.0	2.99	2.9	2.9	V	I_{OUT} = −100 μA
			4.5	3.0	2.8	2.4	2.4		I_{OH} = −12 mA
			4.5	2.7	2.5	2.4	2.4		I_{OL} = −8 mA
V_{OLA}	Maximum Low Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	I_{OUT} =100 μA
			4.5	3.0	0.18	0.36	0.44		I_{OL} = 24 mA
V_{OLB}			4.5	3.0	0.002	0.1	0.1	V	I_{OUT} = 100 μA
			4.5	3.0	0.1	0.31	0.4		I_{OL} = 12 mA
			4.5	2.7	0.1	0.31	0.4		I_{OL} = 8 mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		5.5	3.6		±0.1	±1.0	μA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A(n)		5.5	3.6		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	74LVX4245 $T_A = +25°C$	74LVX4245 $T_A = -40°C$ to $+85°C$		Units	Conditions
				Typ	Guaranteed Limits			
I_{OZB}	Maximum TRI-STATE Output Leakage @ B(n)	5.5	3.6		±0.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CCT}/Input @ A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.6	1.0	1.35	1.5	mA	$V_I = V_{CCA} - 2.1V$
	Input @ B(n)	5.5	3.6		0.35	0.5	mA	$V_I = V_{CCB} - 0.6V$
I_{CCA}	Quiescent V_{CCA} Supply Current	5.5	3.6		8	80	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current	5.5	3.6		5	50	μA	A(n) = V_{CCA} or GND B(n) = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = V_{CCA}
V_{OLPA} V_{OLPB}	Quiet Output Maximum Dynamic V_{OL}	5.0 5.0	3.3 3.3		1.5 0.8		V	(Notes 1, 2)
V_{OLVA} V_{OLVB}	Quiet Output Minimum Dynamic V_{OL}	5.0 5.0	3.3 3.3		−1.2 −0.8		V	(Notes 1, 2)
V_{IHDA} V_{IHDB}	Minimum High Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		2.0 2.0		V	(Notes 1, 3)
V_{ILDA} V_{ILDB}	Maximum Low Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		0.8 0.8		V	(Notes 1, 3)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), OV to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameters	74LVX4245 $T_A = +25°C$, $C_L = 50$ pF, $*V_{CCA} = 5V$, $**V_{CCB} = 3.3V$			74LVX4245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $*V_{CCA} = 5V$, $**V_{CCB} = 3.3V$		74LVX4245 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $*V_{CCA} = 5V$, $V_{CCB} = 2.7V$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	5.1 5.3	8.5 8.5	1.0 1.0	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	5.4 5.5	8.5 8.5	1.0 1.0	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	6.5 6.7	10.0 10.0	1.0 1.0	10.5 10.5	1.0 1.0	11.5 11.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.2 5.8	9.0 9.0	1.0 1.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	6.0 3.3	9.5 6.5	1.0 1.0	10.0 7.0	1.0 1.0	10.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	3.9 2.9	7.0 6.5	1.0 1.0	7.5 7.0	1.0 1.0	7.5 7.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew*** Data to Output		1.0	1.5		1.5		1.5	ns

*Voltage Range 5.0V is 5.0V ±0.5V.
**Voltage Range 3.3V is 3.3V ±0.3V.
***Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

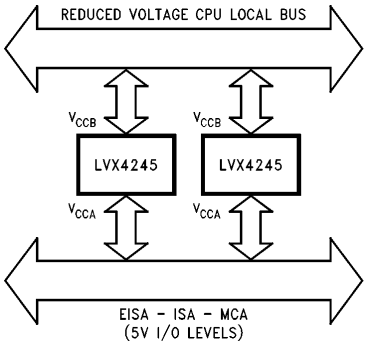
Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		15	pF	$V_{CCA} = 5.0V$ $V_{CCB} = 3.3V$
C_{PD}	Power Dissipation Capacitance	B ⟶ A	55	pF	$V_{CCA} = 5.0V$
		A ⟶ B	40	pF	$V_{CCB} = 3.3V$

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



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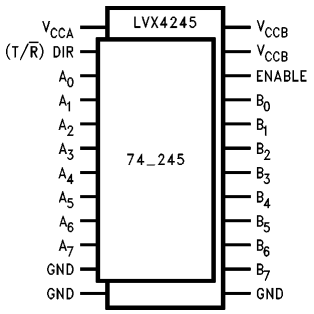
Applications: Mixed Mode Dual Supply Interface Solution

LVX4245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latch-up effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The ''A'' port is a dedicated 5V port to interface 5V ICs. The ''B'' port is a dedicated port to interface 3V ICs. *Figure 1* shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

This device is also configured as an 8-bit 245 transceiver, giving the designer TRI-STATE capabilities and the ability to select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 74 series 245, as shown in *Figure 2*, the designer could use this device in either a 3V system or a 5V system without any further work to re-layout the board.



TL/F/11540–4

FIGURE 2. LVX4245 Pin Arrangment is Compatible to 20-Pin 74 Series 245

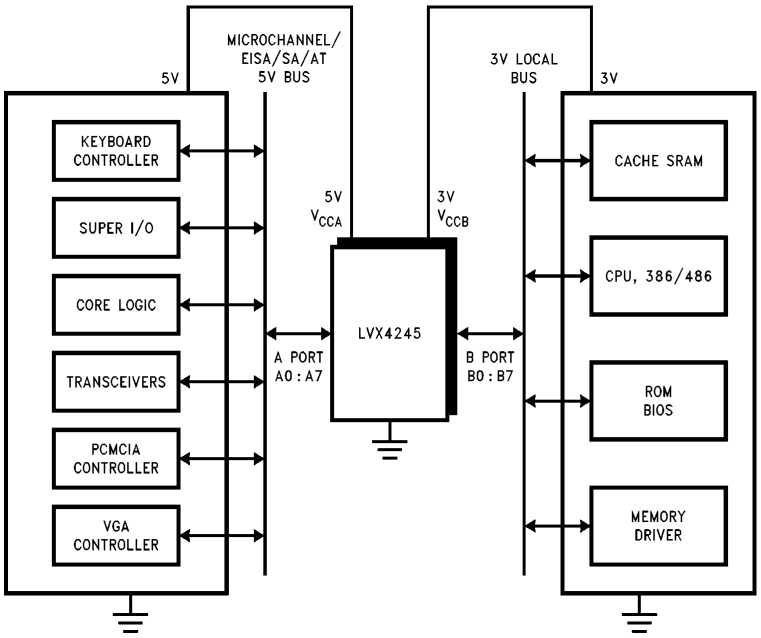


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FIGURE 1. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem

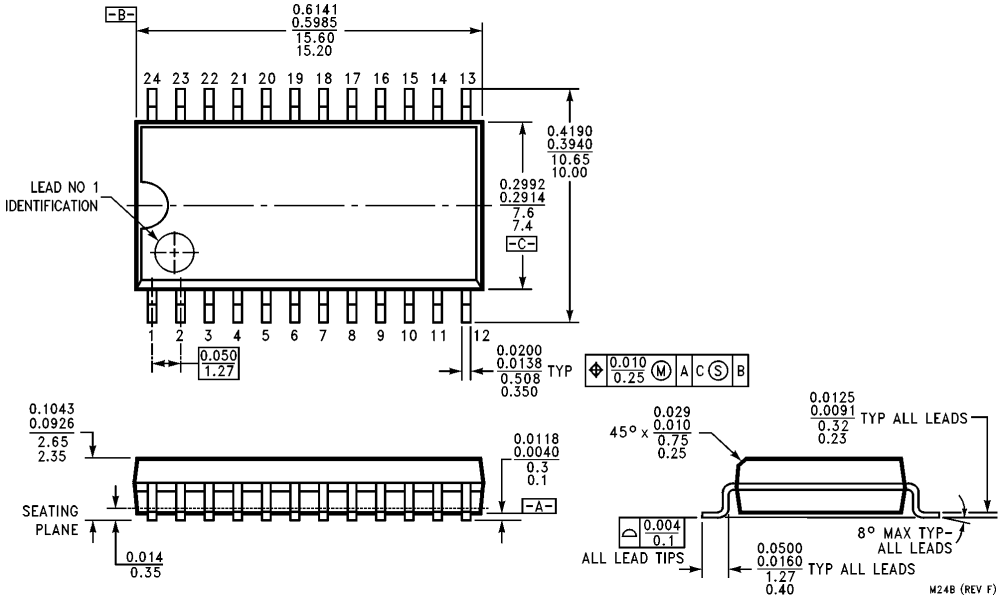
74LVX4245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74LVX 4245 MW X

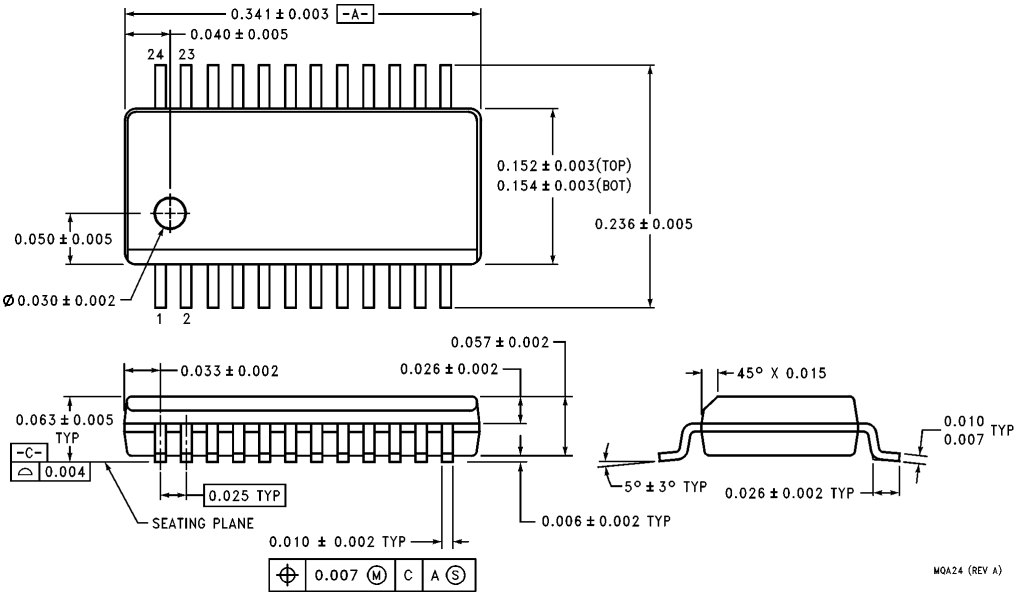
- 74LVX — Temperature Range Family
  - 74 = Commercial
- 4245 — Device Type
- MW — Package Code
  - WM = Small Outline JEDEC SOIC (0.300″ Wide)
  - QSC = Molded Shrink Small Outline Package, JEDEC (also known as QSOP)
- X — Special Variations
  - "X" = Tape and Reel
  - " " = Rail/Tube

Physical Dimensions inches / millimeters



24-Lead (0.300″ Wide) Small Outline Package (WM)
Order Number 74LVX4245WM or 74LVX4245WMX
NS Package Number M24B

Physical Dimensions inches (Continued)



24-Lead, Molded Shrink Small Outline Package, JEDEC (QSC)
(also known as: QSOP)
Order Number 74LVX4245QSC or 74LVX4245QSCX
NS Package Number MQA24

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408