

## 54F/74F676 16-Bit Serial/Parallel-In, Serial-Out Shift Register

### General Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data ( $P_0$ - $P_{15}$ ) inputs is entered on the falling edge of the Clock Pulse ( $\overline{CP}$ ) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents both parallel and serial operations.

### Features

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

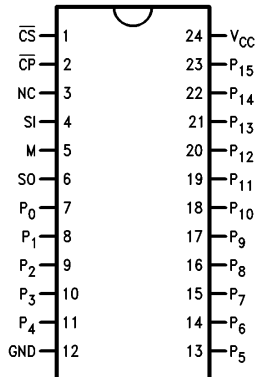
Commercial	Military	Package Number	Package Description
74F676PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F676SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F676DM (Note 2)	J24A	24-Lead (0.600" Wide) Ceramic Dual-In-Line
	54F676SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F676SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F676FM (Note 2)	W24C	24-Lead Cerpack
	54F676LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMOB and LMOB.

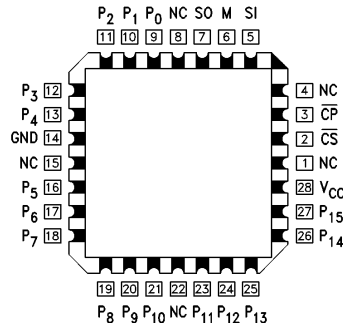
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9588-2

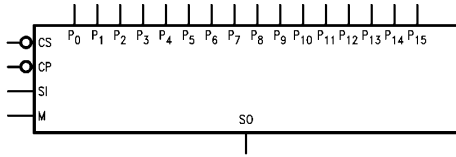
Pin Assignment  
for LCC



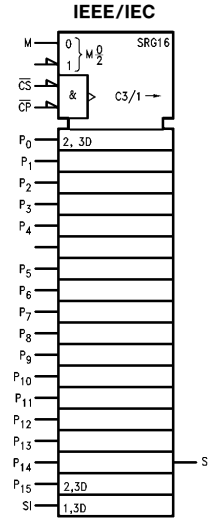
TL/F/9588-3

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## Logic Symbols



TL/F/9588-1



TL/F/9588-4

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$P_0$ – $P_{15}$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
M	Mode Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
SI	Serial Data Input	1.0/1.0	20 $\mu$ A/–0.6 mA
SO	Serial Output	50/33.3	–1 mA/20 mA

## Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

**HOLD**—a HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents clocking, and data is stored in the sixteen registers.

**Shift/Serial Load**—data present on the SI pin shifts into the register on the falling edge of  $\overline{CP}$ . Data enters the  $Q_0$  position and shifts toward  $Q_{15}$  on successive clocks, finally appearing on the SO pin.

**Parallel Load**—data present on  $P_0$ – $P_{15}$  are entered into the register on the falling edge of  $\overline{CP}$ . The SO output represents the  $Q_{15}$  register output.

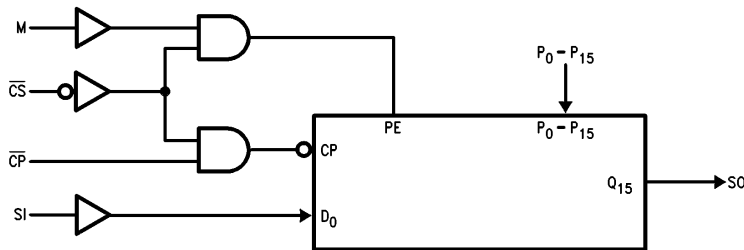
To prevent false clocking,  $\overline{CP}$  must be LOW during a LOW-to-HIGH transition of  $\overline{CS}$ .

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	$\sim$	Shift/Serial Load
L	H	$\sim$	Parallel Load

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $\sim$  = HIGH-to-LOW Transition

## Block Diagram



TL/F/9588-5

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions	
		Min	Typ	Max				
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA	
		74F 10% V <sub>CC</sub>	2.5					
		74F 5% V <sub>CC</sub>	2.7					
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA	
		74F 10% V <sub>CC</sub>		0.5				
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V	
		74F		5.0				
I <sub>BVI</sub>	Input HIGH Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V	
		74F		7.0				
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
		74F		50				
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded	
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV, All Other Pins Grounded	
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V	
I <sub>OS</sub>	Output Short-Circuit Current			-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current				72	mA	Max	

## AC Electrical Characteristics

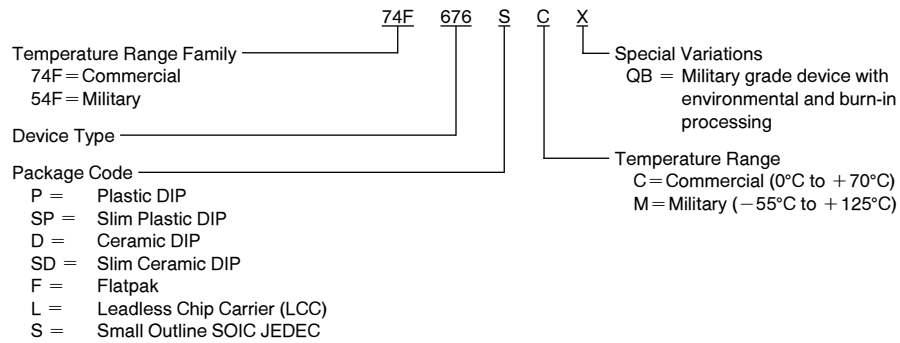
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	100	110		45		90		MHz
t <sub>PLH</sub>	Propagation Delay CP to SO	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns
t <sub>PHL</sub>		5.0	9.0	12.5	5.0	14.5	5.0	13.5	

## AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		
		Min	Max	Min	Max	Min	Max	
t <sub>s</sub> (H)	Setup Time, HIGH or LOW SI to CP	4.0		4.0		4.0		ns
t <sub>s</sub> (L)		4.0		4.0		4.0		
t <sub>h</sub> (H)	Hold Time, HIGH or LOW SI to CP	4.0		4.0		4.0		ns
t <sub>h</sub> (L)		4.0		4.0		4.0		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW P <sub>n</sub> to CP	3.0		3.0		3.0		ns
t <sub>s</sub> (L)		3.0		3.0		3.0		
t <sub>h</sub> (H)	Hold Time, HIGH or LOW P <sub>n</sub> to CP	4.0		4.0		4.0		ns
t <sub>h</sub> (L)		4.0		4.0		4.0		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW M to CP	8.0		8.0		8.0		ns
t <sub>s</sub> (L)		8.0		8.0		8.0		
t <sub>h</sub> (H)	Hold Time, HIGH or LOW M to CP	2.0		2.0		2.0		ns
t <sub>h</sub> (L)		2.0		2.0		2.0		
t <sub>s</sub> (L)	Setup Time, LOW CS to CP	10.0		12.0		10.0		ns
t <sub>h</sub> (H)	Hold Time, HIGH CS to CP	10.0		10.0		10.0		
t <sub>w</sub> (H)	CP Pulse Width HIGH or LOW	4.0		5.0		4.0		ns
t <sub>w</sub> (L)		6.0		9.0		6.0		

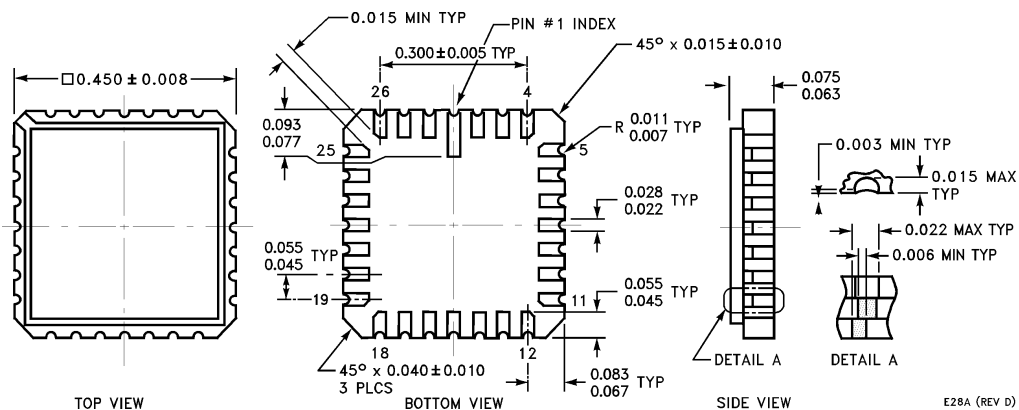
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



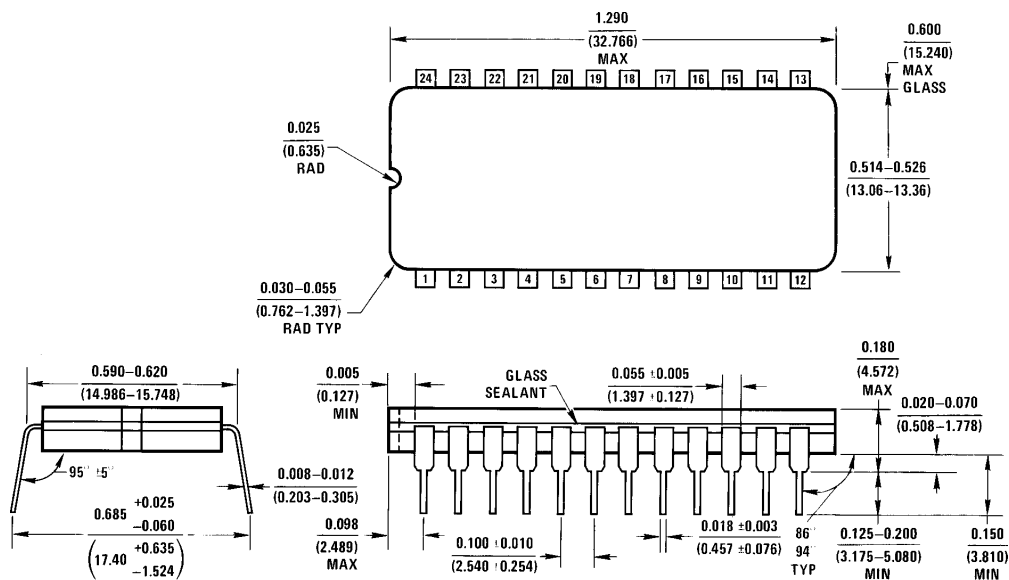


**Physical Dimensions** inches (millimeters)



**28-Lead Ceramic Leadless Chip Carrier (L)**  
NS Package Number E28A

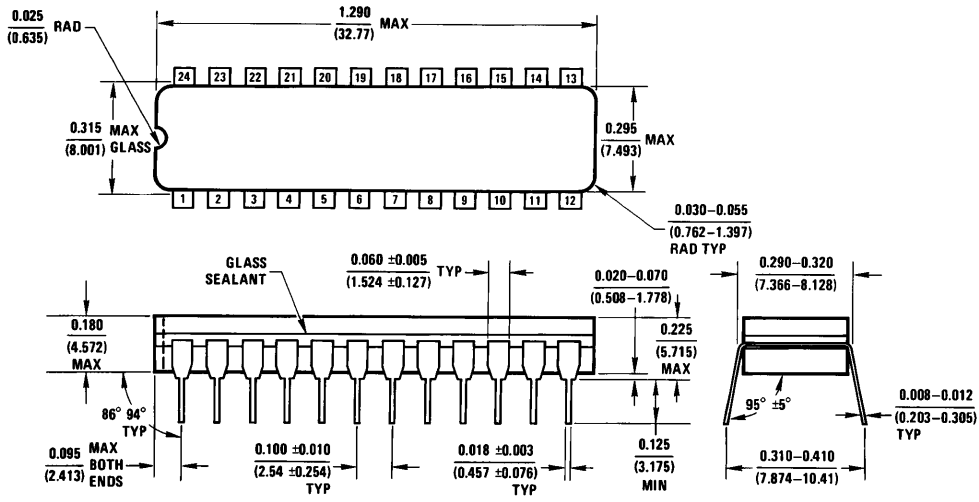
E28A (REV D)



**24-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J24A

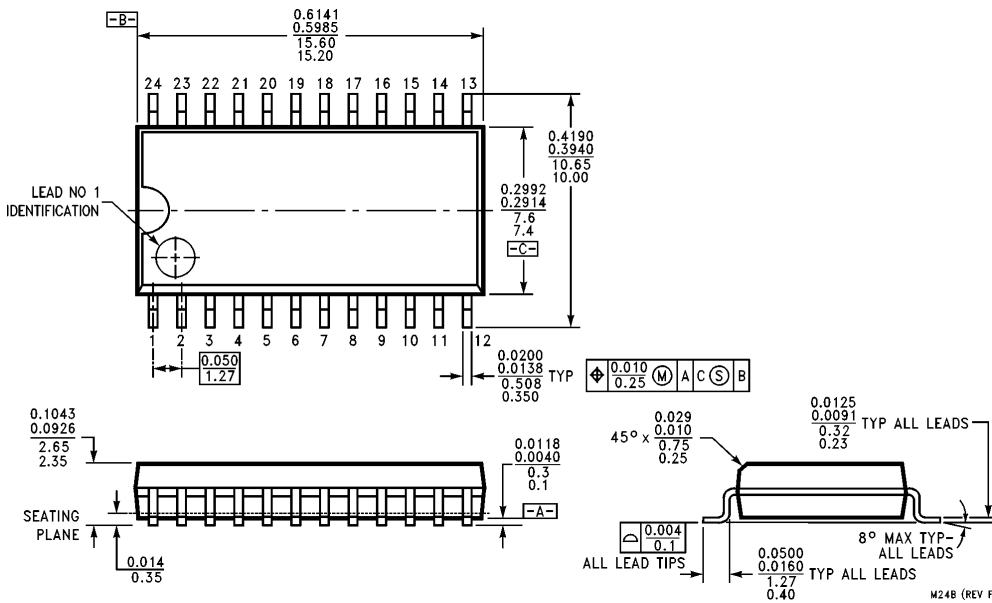
J24A (REV H)

**Physical Dimensions** inches (millimeters) (Continued)



**24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)**  
NS Package Number J24F

J24F (REV G)

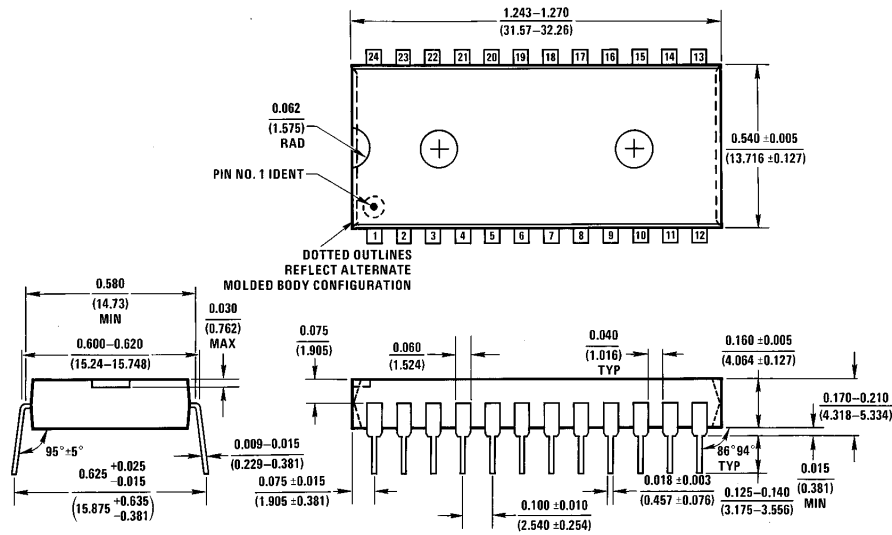


**24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC**  
NS Package Number M24B

M24B (REV F)

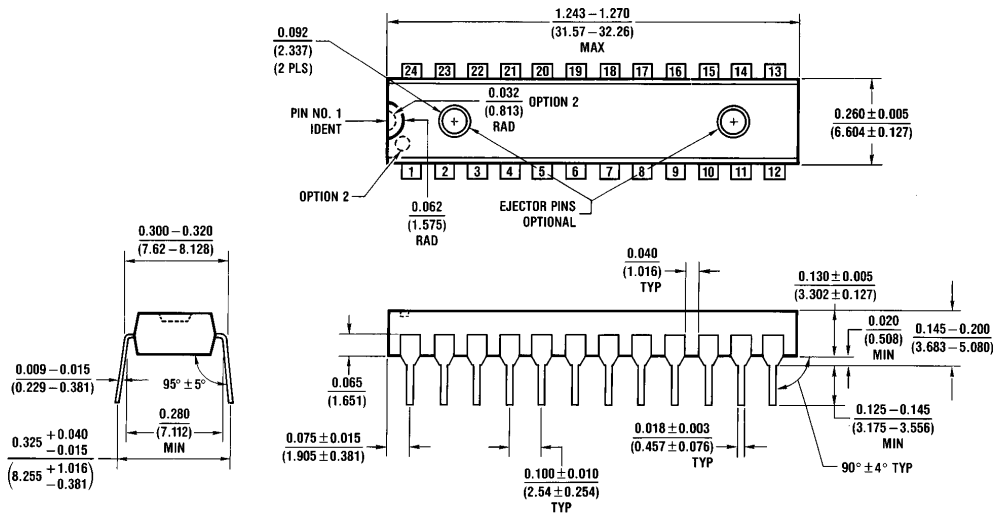


**Physical Dimensions** inches (millimeters) (Continued)



N24A (REV E)

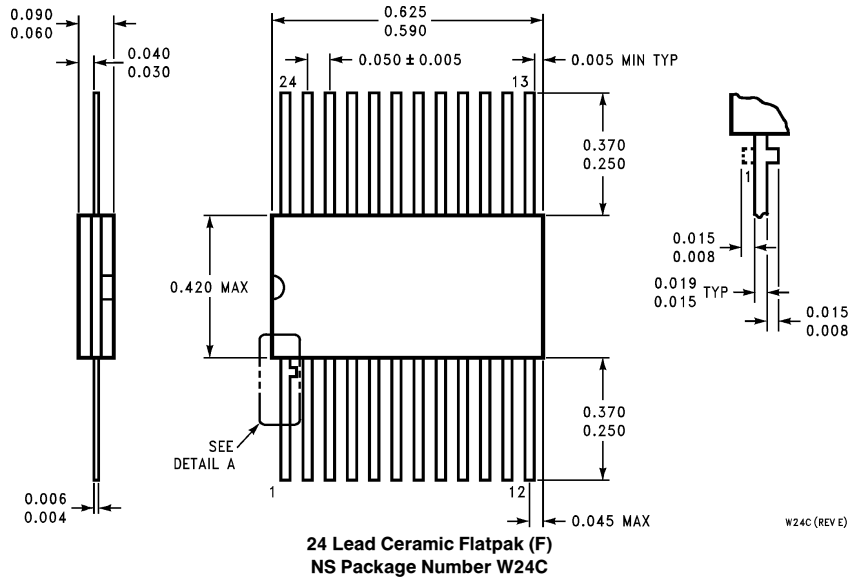
**24-Lead (0.600" Wide) Molded Dual-In-Line Package (P)**  
**NS Package Number N24A**



N24C (REV F)

**24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)**  
**NS Package Number N24C**

**Physical Dimensions** inches (millimeters) (Continued)



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