NEC

MOS INTEGRATED CIRCUIT
μPD720110A

USB2.0 HUB CONTROLLER

The μPD720110A is an USB 2.0 hub device that comply with the Universal Serial Bus (USB) Specification Revision 2.0 and work up to 480 Mbps. USB2.0 compliant transceivers are integrated for upstream and all downstream ports. The μPD720110A works backward compatible either when any one of downstream ports is connected to an USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD720110A User's Manual: S15738E

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- Certified by USB implementers forum and granted with USB 2.0 high-Speed Logo
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction at downstream facing ports when Hub controller is working at high-speed mode.
- One Transaction Translator per Hub and supports 4 non-periodic buffers
- Supports self-powered mode only
- Supports Over-current detection and Individual power control
- Supports configurable vendor ID and product ID with external Serial ROM
- Supports "non-removable" attribution on individual port
- Uses 30 MHz X'tal, 30 MHz clock input, or 48 MHz clock input
- Supports downstream port status with LED
- HS detection indicator output
- 3.3 V power supply

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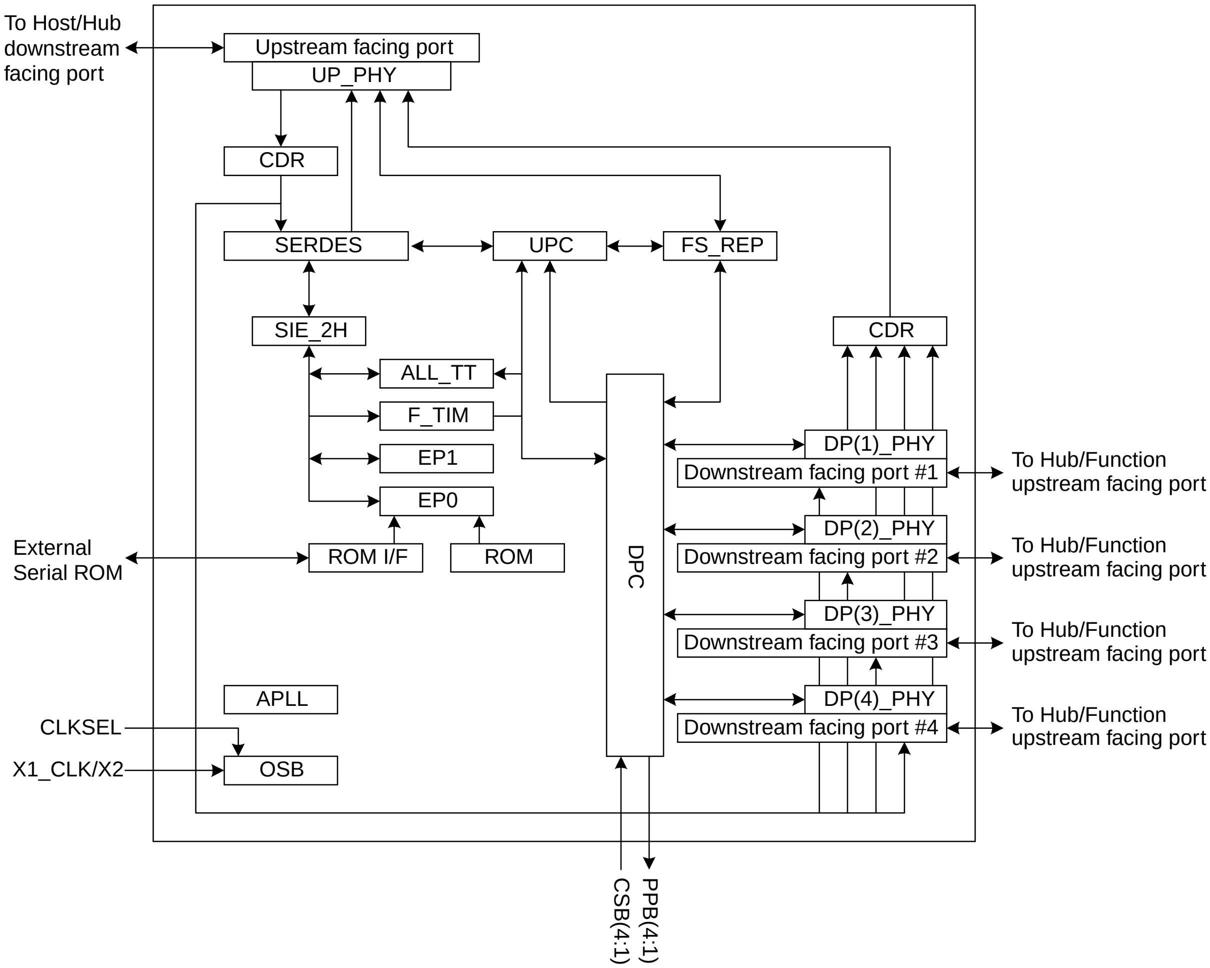
ORDERING INFORMATION

Part Number	Package
μPD720110AGC-8EA	100-pin plastic LQFP (Fine pitch) (14 × 14)

BLOCK DIAGRAM

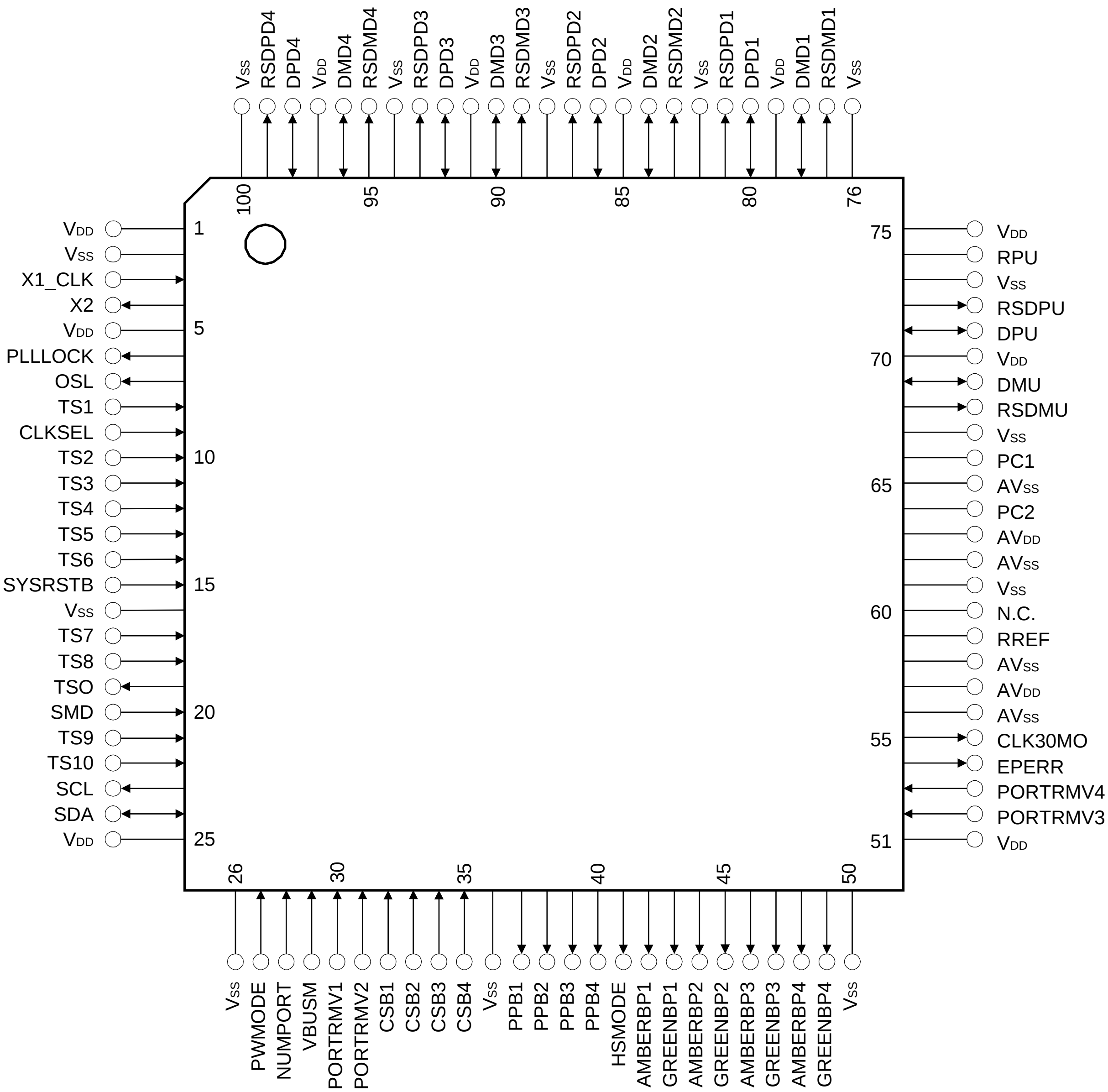


APLL	:	Generates all clocks of Hub.
ALL_TT	:	Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	:	Data & clock recovery circuit
DPC	:	Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	:	Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	:	Endpoint 0 controller
EP1	:	Endpoint 1 controller
F_TIM (Frame Timer)	:	Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	:	Full/low-speed repeater is enabled when the μPD720110A is worked at full-speed mode
OSB	:	Oscillator Block
ROM	:	Contains default Descriptors
ROM I/F	:	Interface block for external Serial ROM which contains user-defined Descriptors
SERDES	:	Serializer and Deserializer
SIE_2H	:	Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer
UP_PHY	:	Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	:	Upstream Port Controller handles Suspend and Resume

PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic LQFP (Fine pitch) (14 × 14)**

μPD720110AGC-8EA



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	26	V_{SS}	51	V_{DD}	76	V_{SS}
2	V_{SS}	27	PWMODE	52	PORTRMV3	77	RSDMD1
3	X1_CLK	28	NUMPORT	53	PORTRMV4	78	DMD1
4	X2	29	VBUSM	54	EPERR	79	V_{DD}
5	V_{DD}	30	PORTRMV1	55	CLK30MO	80	DPD1
6	PLLLOCK	31	PORTRMV2	56	AV_{SS}	81	RSDPD1
7	OSL	32	CSB1	57	AV_{DD}	82	V_{SS}
8	TS1	33	CSB2	58	AV_{SS}	83	RSDMD2
9	CLKSEL	34	CSB3	59	RREF	84	DMD2
10	TS2	35	CSB4	60	N.C.	85	V_{DD}
11	TS3	36	V_{SS}	61	V_{SS}	86	DPD2
12	TS4	37	PPB1	62	AV_{SS}	87	RSDPD2
13	TS5	38	PPB2	63	AV_{DD}	88	V_{SS}
14	TS6	39	PPB3	64	PC2	89	RSDMD3
15	SYSRSTB	40	PPB4	65	AV_{SS}	90	DMD3
16	V_{SS}	41	HSMODE	66	PC1	91	V_{DD}
17	TS7	42	AMBERBP1	67	V_{SS}	92	DPD3
18	TS8	43	GREENBP1	68	RSDMU	93	RSDPD3
19	TSO	44	AMBERBP2	69	DMU	94	V_{SS}
20	SMD	45	GREENBP2	70	V_{DD}	95	RSDMD4
21	TS9	46	AMBERBP3	71	DPU	96	DMD4
22	TS10	47	GREENBP3	72	RSDPU	97	V_{DD}
23	SCL	48	AMBERBP4	73	V_{SS}	98	DPD4
24	SDA	49	GREENBP4	74	RPU	99	RSDPD4
25	V_{DD}	50	V_{SS}	75	V_{DD}	100	V_{SS}

1. PIN INFORMATION

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Pin Name	I/O	Buffer Type	Active Level	Function
X1_CLK	I	Input		System clock input or oscillator in
X2	O	Output		Oscillator out
SYSRSTB	I	5 V tolerant Input	Low	Asynchronous chip reset
CLK30MO	O (I/O)	Output		30 MHz clock output
CLKSEL	I	Input		Clock select signal
RPU	A	Analog		External 1.5 kΩ pull-up resistor control
DPD(4:1)	B	USB high speed D+ I/O		Downstream high-speed data D+
DPU	B	USB high speed D+ I/O		Upstream high-speed data D+
DMD(4:1)	B	USB high speed D– I/O		Downstream high-speed data D–
DMU	B	USB high speed D– I/O		Upstream high-speed data D–
RSDPD(4:1)	O	USB full-speed D+ O		Downstream full-speed data D+ and R_S resistor terminal
RSDPU	O	USB full-speed D+ O		Upstream full-speed data D+ and R_S resistor terminal
RSDMD(4:1)	O	USB full-speed D– O		Downstream full-speed data D– and R_S resistor terminal
RSDMU	O	USB full-speed D– O		Upstream full-speed data D– and R_S resistor terminal
RREF	A	Analog		Reference resistor
PC1	A	Analog		Capacitor for PLL
PC2	A	Analog		Capacitor for PLL
CSB(4:1)	I (I/O)	5 V tolerant input	Low	Port’s overcurrent status input
PPB(4:1)	O	5 V tolerant N-ch open drain	Low	Port’s power supply control output
NUMPORT	I	Input		Number of available ports
PWMODE	I	Input		Power mode select
VBUSM	I	Input		VBus monitor
PORTRMV(2:1)	I	Input		Removable/Non-removable select
PORTRMV(4:3)	I (I/O)	Input		Removable/Non-removable select
OSL	O (I/O)	Output	High	Indication for suspend state
HSMODE	O	Output	Low	Indication for high-speed operation
AMBERBP(4:1)	O	Output	Low	Indication for downstream port status with amber colored LED
GREENBP(4:1)	O	Output	Low	Indication for downstream port status with green colored LED
SCL	O (I/O)	Output		Serial ROM clock out
SDA	I/O	I/O with 5 kΩ pull-up R		Serial ROM data
SMD	I	Input		Serial ROM input enable
EPERR	O (I/O)	Output		Indication for serial ROM error

(2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
PLLLOCK	O (I/O)	Output		Indication when PLL is locked
TS(1)	I	Input with 12 kΩ pull-down R		Test signal
TS(10:2)	I	Input		Test signal
TSO	I/O	I/O		Test signal
V_{DD}				V_{DD}
AV_{DD}				V_{DD} for analog circuit
V_{SS}				V_{SS}
AV_{SS}				V_{SS} for analog circuit
N.C.				Not connected

Remarks 1. “5 V tolerant“ means that the buffer is 3 V buffer with 5 V tolerant circuit.

2. The signal marked as “(I/O)” in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 5 V schmitt buffer
  SYSRSTB, CSB(4:1)
- 3.3 V oscillator block
  X1_CLK, X2
- 3.3 V input buffer
  CLKSEL, TS(10:1), SMD, PWMODE, NUMPORT, VBUSM, PORTRMV(4:1)
- 3.3 V I_{OL} = 6 mA output buffer
  PLLLOCK, OSL, TSO, SCL, CLK30MO
- 3.3 V I_{OL} = 12 mA output buffer
  EPERR
- 3.3 V I_{OL} = 6 mA schmitt I/O buffer with 5 kΩ pull-up resistor
  SDA
- 5 V I_{OL} = 12 mA output buffer
  HSMODE, AMBERBP(4:1), GREENBP(4:1)
- 5 V I_{OL} = 12 mA N-ch open drain buffer
  PPB(4:1)
- USB2.0 interface
  RPU, DPU, DMU, RSDPU, RSDMU, DPD(4:1), DMD(4:1), RSDPD(4:1), RSDMD(4:1), RREF, PC1, PC2

Above, “5 V” refers to a 3 V buffer that is 5 V tolerant (has 5 V maximum voltage). Therefore, it is possible to have a 5 V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD} voltage.

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when a current flow out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

2.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I			
3.3 V input voltage		$V_I < V_{DD} + 0.5$ V	–0.5 to +4.6	V
5 V input voltage		$V_I < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Output voltage	V_O			
3.3 V output voltage		$V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
5 V output voltage		$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Operating temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

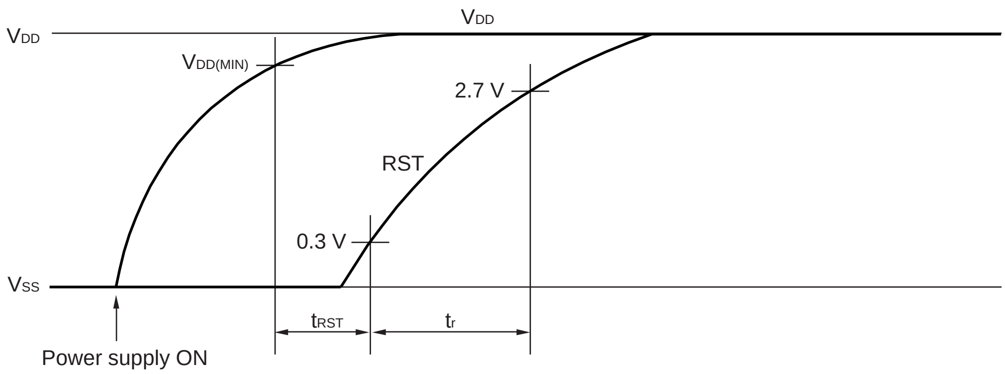
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	V_{DD}		3.14	3.30	3.46	V
High-level input voltage	V_{IH}					
3.3 V High-level input voltage			2.0		V_{DD}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V_H		0.3		1.5	V
Input rise time for SYSRSTB [Note]	t_r				10	ms
Reset time	t_{RST}		0.005		90	ms

Note Drive Low on SYSRSTB pin when only in Power On Reset timing.

Figure 2-1. Power On Reset Timing



DC Characteristics

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output leakage current	I_{OZ}	$V_O = V_{DD}$ or GND		±10	μA
Output short circuit current	I_{OS} Note			–250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current		V_{OL} = 0.4 V	6		mA
3.3 V low-level output current		V_{OL} = 0.4 V	12		mA
5.0 V low-level output current		V_{OL} = 0.4 V	12		mA
High-level output current	I_{OH}				
3.3 V high-level output current		V_{OH} = 2.4 V	–6		mA
3.3 V high-level output current		V_{OH} = 2.4 V	–12		mA
5.0 V high-level output current		V_{OH} = 2.4 V	–2		mA

Note The output short circuit time is one second or less and is only for one pin on the LSI.

USB Interface Block

Parameter	Symbol	Conditions	MIN	MAX	Unit
Serial Resistor between DPx (DMx) and RSDPx (RSDMx).	R_S		35.64	36.36	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}		1.425	1.575	kΩ
Bus pull-up resistor on downstream facing port	R_{PD}		14.25	15.75	kΩ
Termination voltage for upstream facing port pullup (full-speed)	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert (D+) - (D-) \rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See Figure 2-5.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10.0	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10.0	+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		–900	–500	mV

Figure 2-2. Differential Input Sensitivity Range for Low-/full-speed

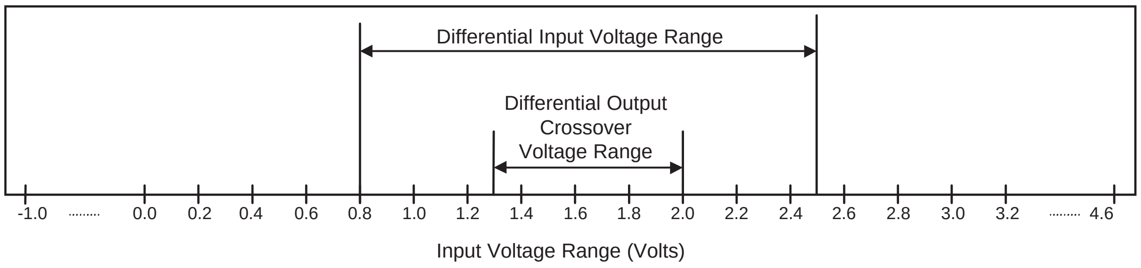


Figure 2-3. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

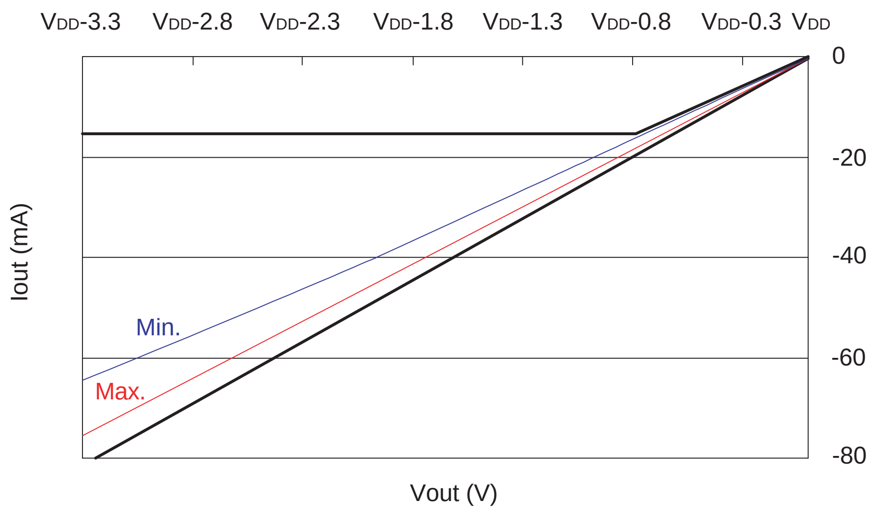


Figure 2-4. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

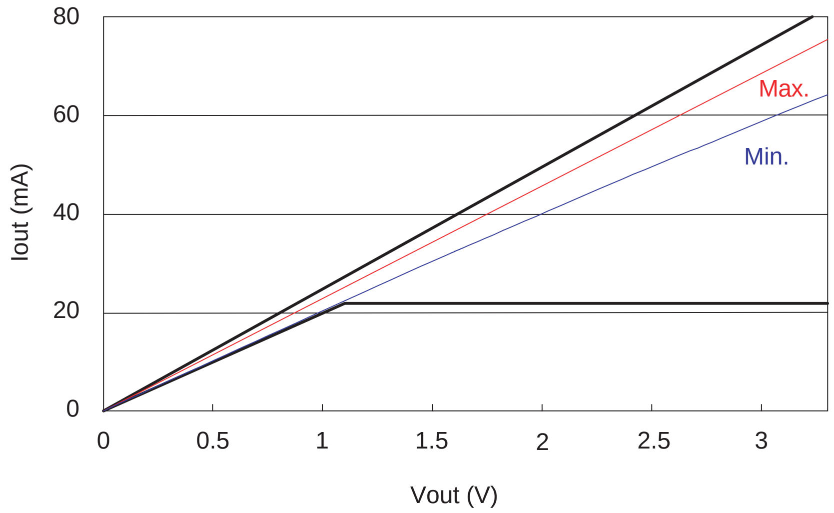


Figure 2-5. Receiver Sensitivity for Transceiver at DP/DM

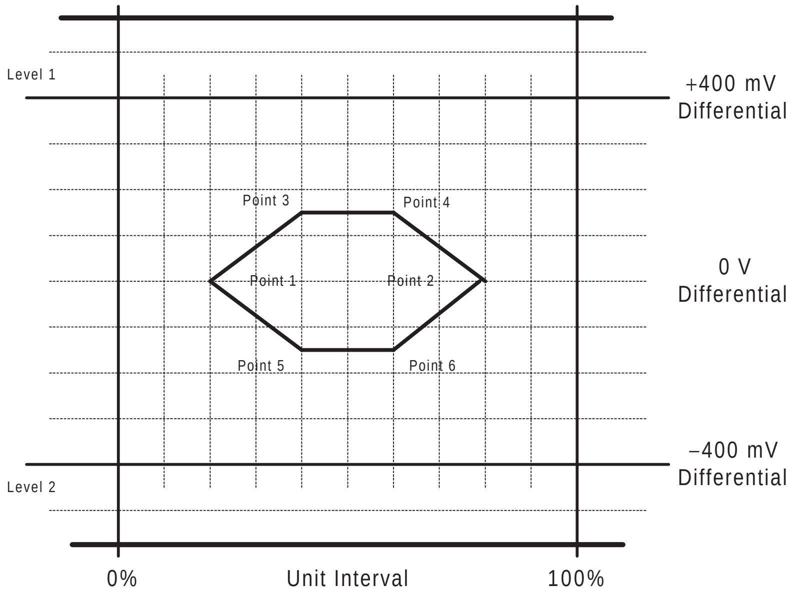
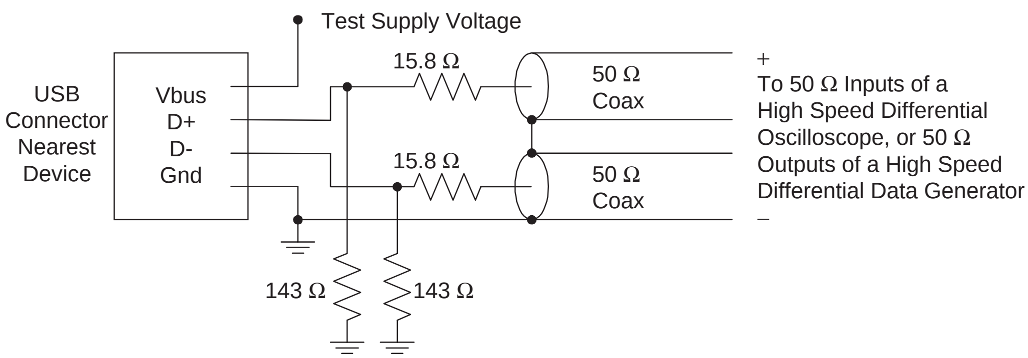


Figure 2-6. Receiver Measurement Fixtures



Power Consumption

Parameter	Symbol	Condition	TYP.	Unit
Power Consumption	P_{W-0}	The power consumption under the state without suspend. All the ports does not connect to any function. Note 1		
		Hub controller is operating at full-speed mode.	185	mA
		Hub controller is operating at high-speed mode.	270	mA
	P_{W-2}	The power consumption under the state without suspend. The number of active ports is 2. Note 2		
		Hub controller is operating at full-speed mode.	190	mA
		Hub controller is operating at high-speed mode.	400	mA
	P_{W-3}	The power consumption under the state without suspend. The number of active ports is 3. Note 2		
		Hub controller is operating at full-speed mode.	193	mA
		Hub controller is operating at high-speed mode.	460	mA
	P_{W-4}	The power consumption under the state without suspend. The number of active ports is 4. Note 2		
		Hub controller is operating at full-speed mode.	196	mA
		Hub controller is operating at high-speed mode.	525	mA
	P_{W_S}	The power consumption under suspend state. The internal clock is stopped.	1.3	mA

Notes **1.** When any device is not connected to all the ports of HC, the power consumption for HC does not depend on the number of active ports.

2. The number of active ports is set by the value of Port No field in PCI configuration space EXT register.

System Clock Ratings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}	X'tal	–500 ppm	30	+500 ppm	MHz
		Oscillator block	–500 ppm	48	+500 ppm	MHz
Clock Duty cycle	t_{DUTY}		40	50	60	%

Remarks **1.** Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

AC Characteristics (V_{DD} = 3.14 to 3.46 V, T_A = 0 to +70°C)

USB Interface Block

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	C_L = 50 pF to 150 pF, R_S = 36 Ω	75	300	ns
Fall time (90% to 10%)	t_{LF}	C_L = 50 pF to 150 pF, R_S = 36 Ω	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) Note	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Hub differential data delay (Figure 2-9)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (Figure 2-9):					
Downstream facing port					
To next transition	t_{LDHJ1}		–45	+45	ns
For paired transitions	t_{LDHJ2}		–45	+45	ns
Upstream facing port					
To next transition	t_{LUHJ1}		–45	+45	ns
For paired transitions	t_{LUHJ2}		–15	+15	ns
Data bit width distortion after SE0 (Figure 2-9)	t_{LSOP}		–60	+60	ns
Hub EOP delay relative to THDD (Figure 2-10)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (Figure 2-10)	t_{LHESK}		–300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% to 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (Figure 2-11):		**Note**			
To next transition	t_{DJ1}		–3.5	+3.5	ns
For paired transitions	t_{DJ2}		–4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (Figure 2-12)	t_{FDEOP}		–2	+5	ns

Note Excluding the first transition from the Idle state.

(2/4)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Full-speed Electrical Characteristics (Continued)					
Receiver jitter (Figure 2-13): To Next Transition For Paired Transitions	 t_{JR1} t_{JR2}		 –18.5 –9	 +18.5 +9	 ns ns
Source SE0 interval of EOP (Figure 2-12)	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (Figure 2-12)	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns
Hub differential data delay (with cable)	t_{HDD1}			70	ns
Hub differential data delay (without cable) (Figure 2-9)	t_{HDD2}			44	ns
Hub differential driver jitter (including cable) (Figure 2-9): To next transition For paired transitions	 t_{HDJ1} t_{HDJ2}		 –3 –1	 +3 +1	 ns ns
Data bit width distortion after SE0 Figure 2-9)	t_{FSOP}		–5	+5	ns
Hub EOP delay relative to THDD (Figure 2-10)	t_{FEOPD}		0	15	ns
Hub EOP output width skew (Figure 2-10)	t_{FHESK}		–15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{HSR}		500		ps
Fall time (90% to 10%)	t_{HSF}		500		ps
Driver waveform	See Figure 2-7.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 2-7.				
Receiver jitter tolerance	See Figure 2-5.				
Hub data delay (without cable)	t_{HSHDD}			36 high-speed+4 ns	Bit times
Hub data jitter	See Figure 2-5, Figure 2-7.				
Hub delay variation range	t_{HSHDV}			5 high-speed	Bit times
Hub Event Timings					
Time to detect a downstream facing port connect event (Figure 2-15): Awake hub Suspended hub	t_{DCNN}		 2.5 2.5	 2000 12000	 μs μs
Time to detect a disconnect event at a hub's downstream facing port (Figure 2-14)	t_{DDIS}		2.0	2.5	μs

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Hub Event Timings (Continued)					
Duration of driving resume to a downstream port (only from a controlling hub)	t_{DRSMDN}		20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Duration of driving reset to a downstream facing port (Figure 2-16)	t_{DRST}	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t_{URLK}		2.5	100	μs
Time to detect a long SE0 from upstream	t_{URLSE0}		2.5	10000	μs
Duration of repeating SE0 upstream (for low-/full-speed repeater)	t_{URPSE0}			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	$t_{HSRSPIPD1}$			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs
Time from internal power good to device pulling D+ beyond V_{IHZ} (Figure 2-16)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach (Figure 2-16)	t_{ATTDB}			100	ms
Maximum duration of suspend averaging interval	$t_{SUSAVGI}$			1	s
Period of idle bus before device can initiate resume	t_{WTRSM}		5		ms
Duration of driving resume upstream	t_{DRSMUP}		1	15	ms
Resume recovery time	t_{RSMRCY}	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t_{DETRST}		2.5	10000	μs
Reset recovery time (Figure 2-16)	t_{RSTRCY}			10	ms

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Hub Event Timings (Continued)					
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
SetAddress() completion time	$t_{DSETADDR}$			50	ms
Time to complete standard request with no data	$t_{DRQCMPLTND}$			50	ms
Time to deliver first and subsequent (except last) data for standard request	$t_{DRETDATA1}$			500	ms
Time to deliver last data for standard request	$t_{DRETDATAN}$			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	$t_{FILTSE0}$		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	$t_{WTRSTFS}$		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t_{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	$t_{WTRSTHS}$		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t_{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t_{UCHEND}			7.0	ms
Time between detection of downstream chip and entering high-speed state	t_{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t_{WTFS}		1.0	2.5	ms

Clock & Overcurrent Response Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK30MO cycle time	t_{C3C}			33.33		ns
CLK30MO high level width	t_{C3H}		15.9		17.5	ns
CLK30MO low level width	t_{C3L}		15.9		17.5	ns
Overcurrent response time from CSB low to PPB high (Figure 2-19)	t_{OC}		500		625	μs

Figure 2-7. Transmit Waveform for Transceiver at DP/DM

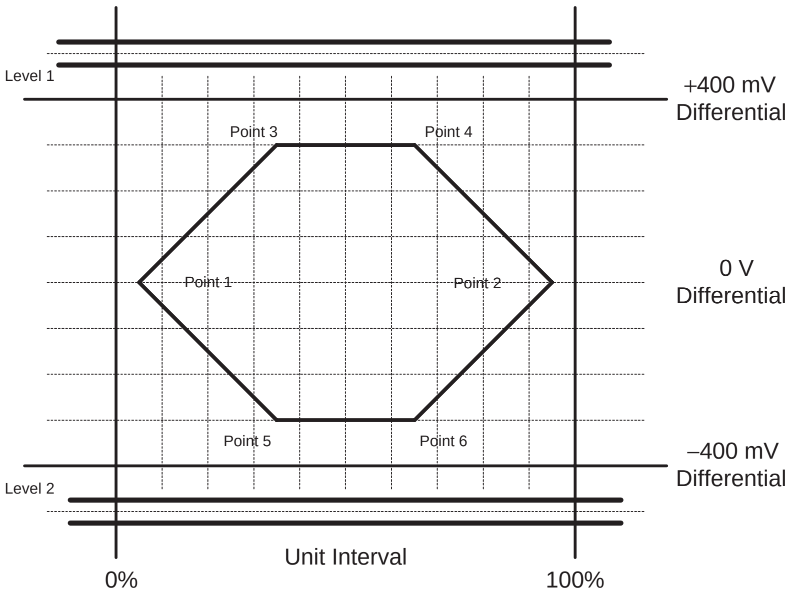
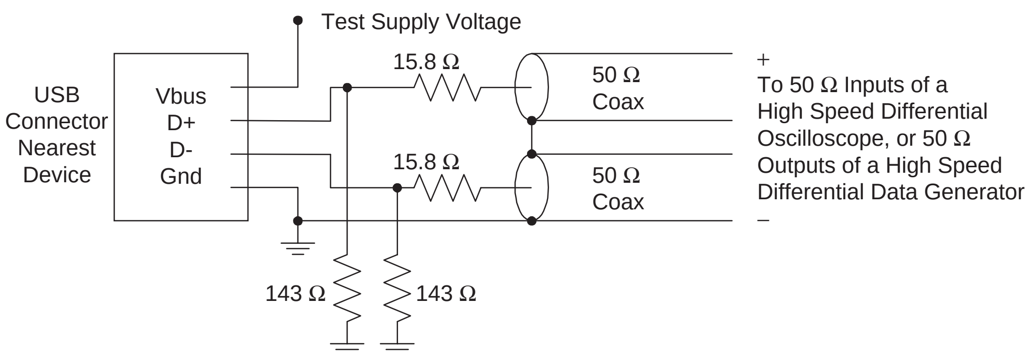
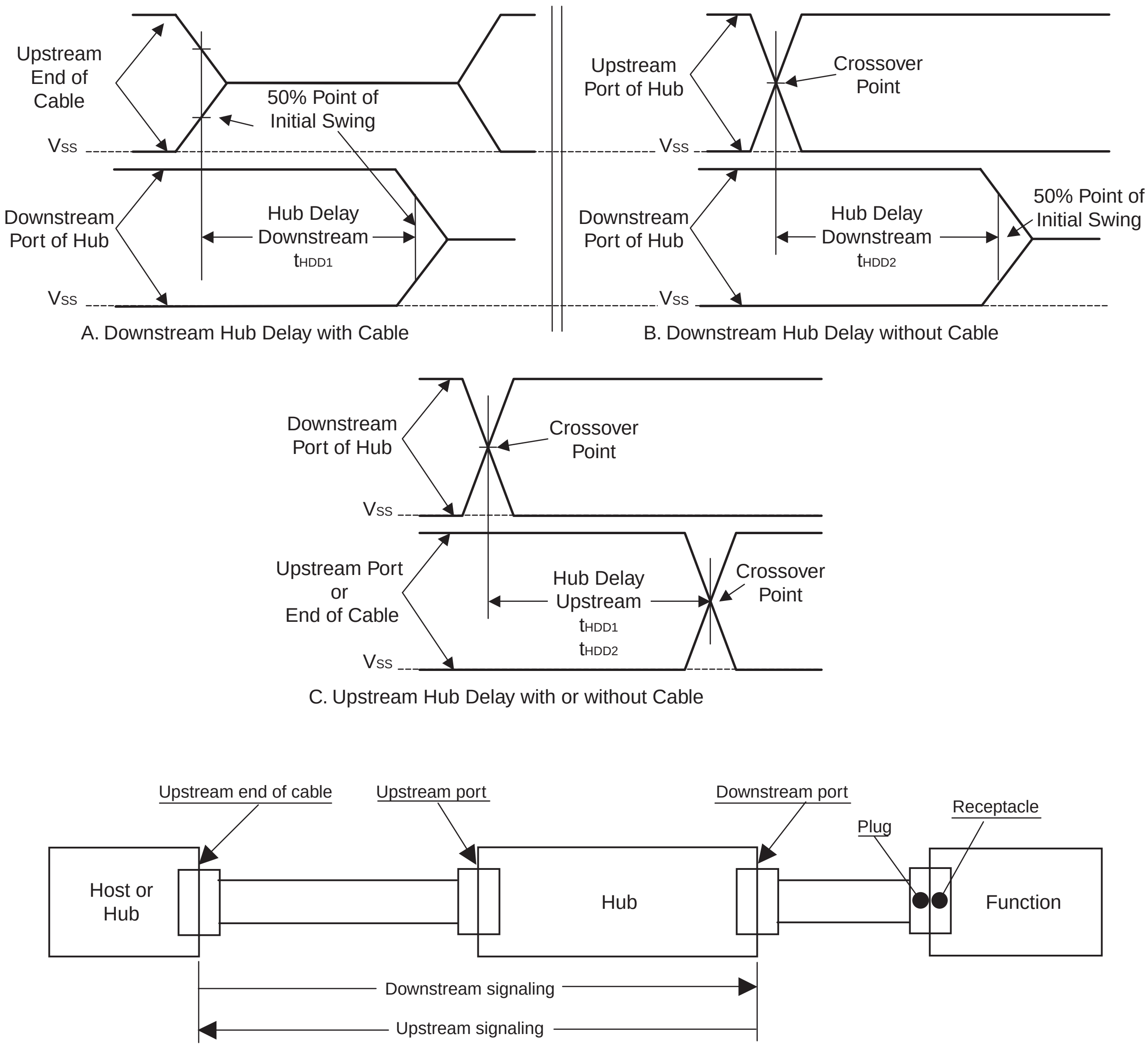


Figure 2-8. Transmitter Measurement Fixtures



Timing Diagram

Figure 2-9. Hub Differential Delay, Differential Jitter, and SOP Distortion



Hub Differential Jitter:

$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions

$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

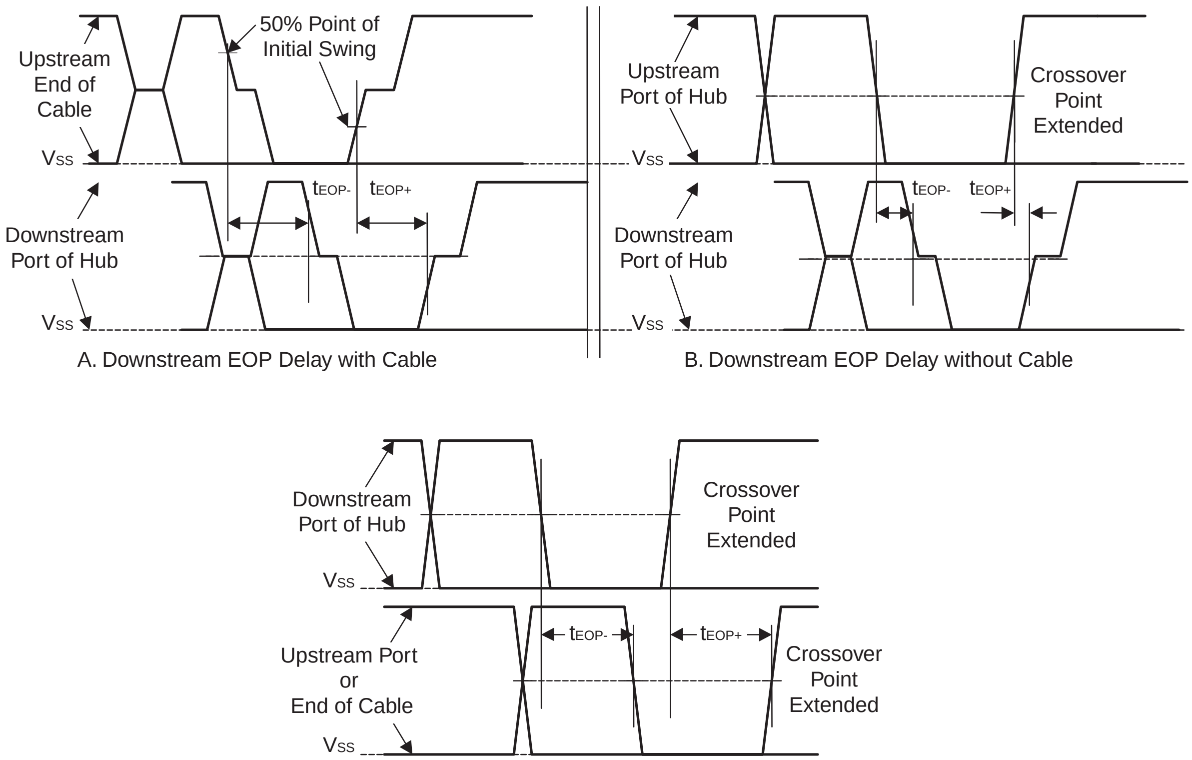
Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):

$t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$

Low-speed timings are determined in the same way for:

t_{LHDD}, t_{LDHJ1}, t_{LDJH2}, t_{LUHJ1}, t_{LUJH2}, and t_{LSOP}

Figure 2-10. Hub EOP Delay and EOP Skew



A. Downstream EOP Delay with Cable

B. Downstream EOP Delay without Cable

C. Upstream EOP Delay with or without Cable

EOP Delay:

$t_{FEOPD} = t_{EOPy} - t_{HDDx}$

(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:

$t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:

t_{LEOPD} and t_{LHESK}

Figure 2-11. USB Differential Data Jitter for Full-speed

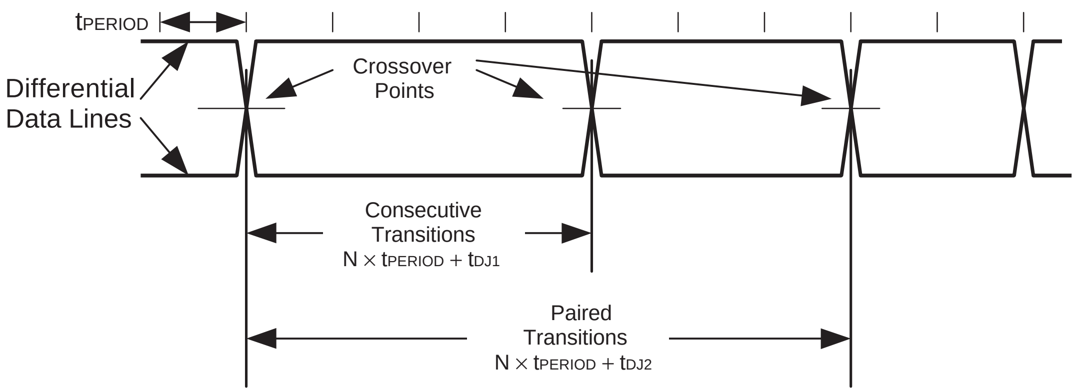


Figure 2-12. USB Differential-to-EOP Transition Skew and EOP Width for Full-speed

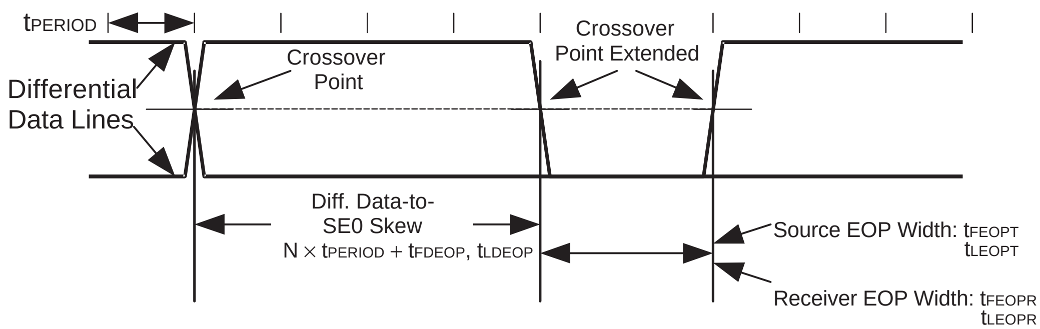


Figure 2-13. USB Receiver Jitter Tolerance for Full-speed

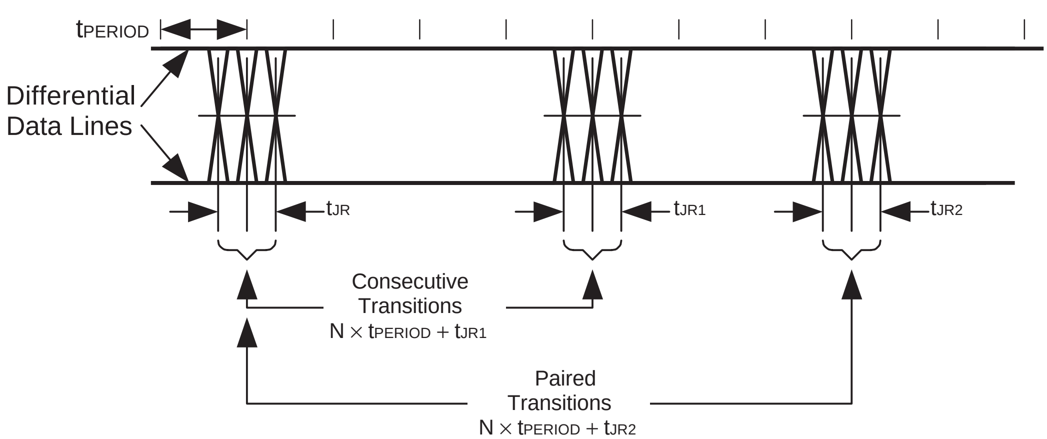


Figure 2-14. Low-/full-speed Disconnect Detection

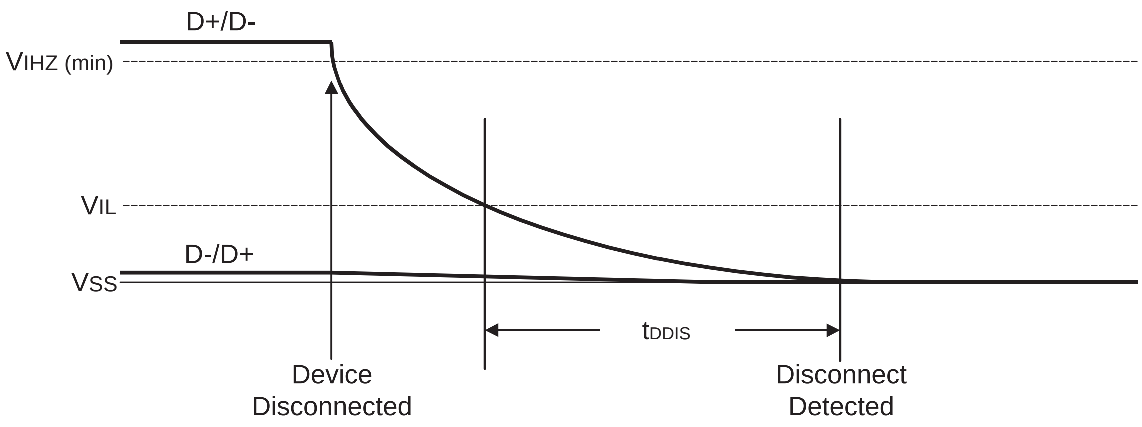


Figure 2-15. Full-/high-speed Device Connect Detection

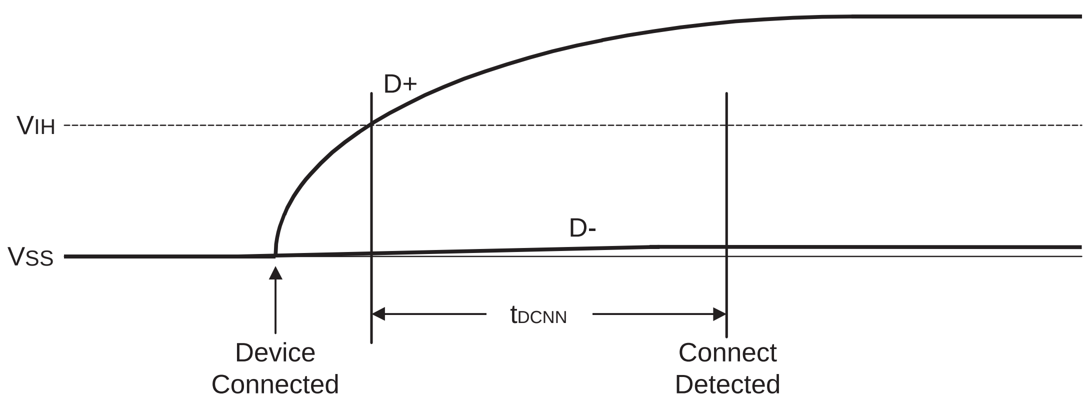


Figure 2-16. Power-on and Connection Events Timing

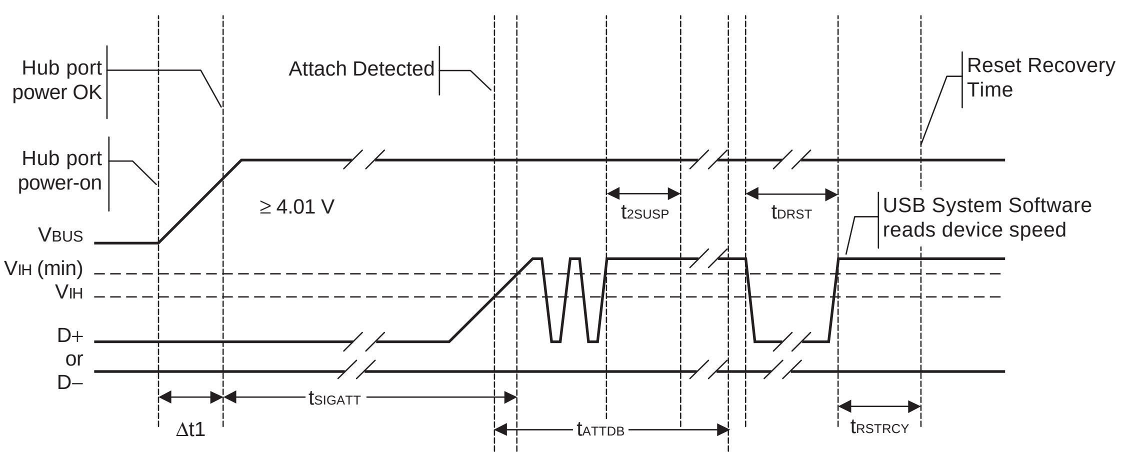


Figure 2-17. Clock Output

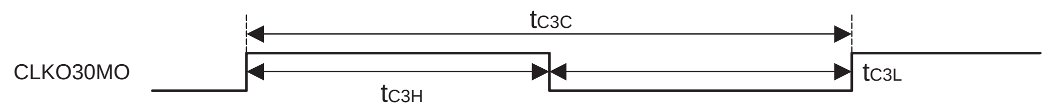
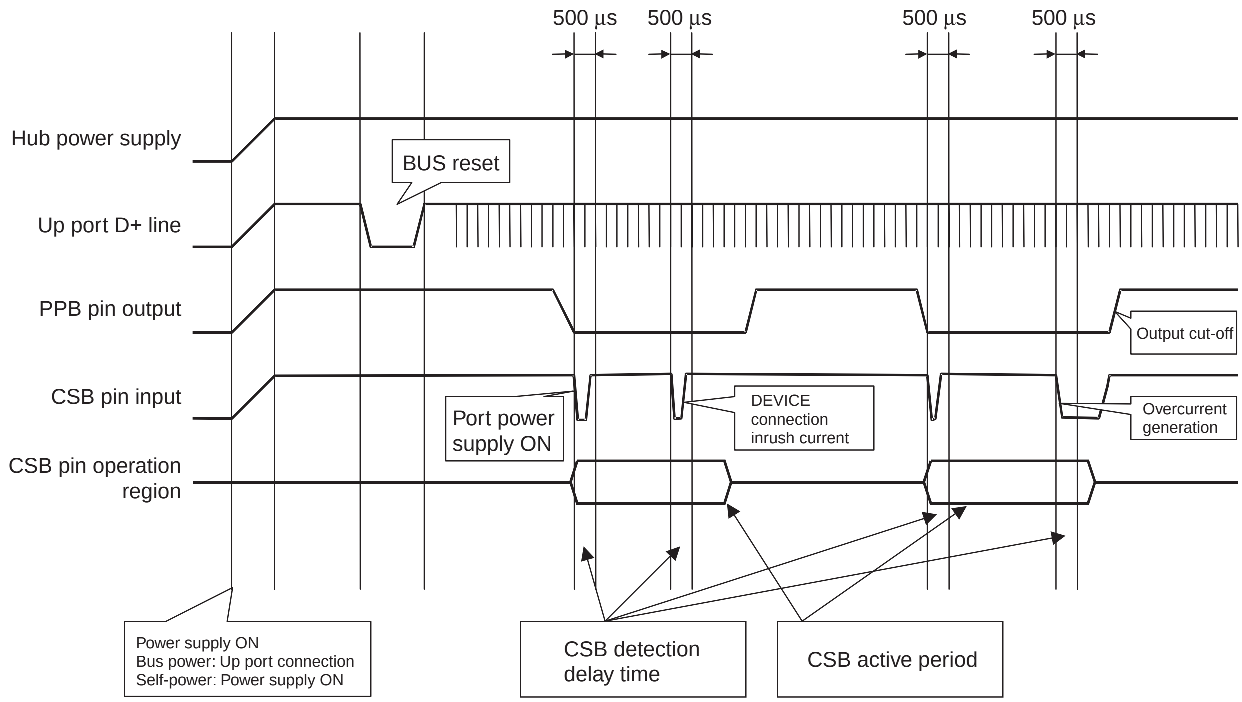
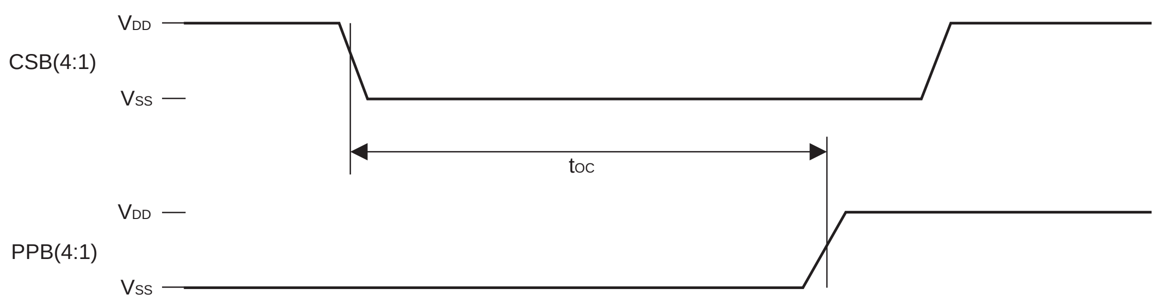


Figure 2-18. CSB/PPB Timing



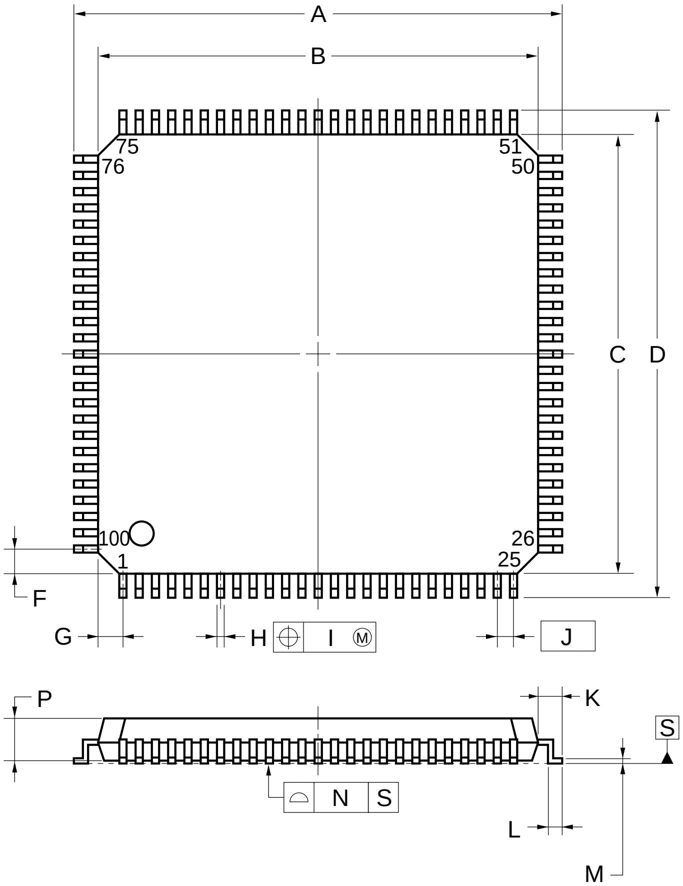
Note The active period of the CSB pin is in effect only when the PPB pin is ON.
There is a delay time of approximately 500 μs duration at the CSB pin.

Figure 2-19. Overcurrent Response Timing

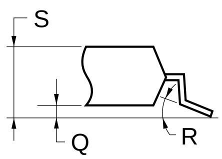


3. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3°^{+7°}_{-3°}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720110A should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact your NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD720100AGC-8EA: 100-pin plastic LQFP (Fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 2 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-102-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.