

MOS FIELD EFFECT TRANSISTOR μ PA1801

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA1801 is a switching device which can be driven directly by a 2.5-V power source.

The μ PA1801 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

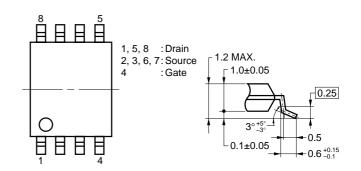
- Can be driven by a 2.5-V power source
- · Low on-state resistance

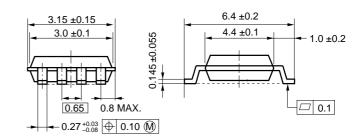
$$\begin{split} &\text{RdS(on)1} = 24~\text{m}\Omega~\text{MAX.}~\text{(VGS} = 4.5~\text{V, ID} = 3.0~\text{A)} \\ &\text{RdS(on)2} = 25~\text{m}\Omega~\text{MAX.}~\text{(VGS} = 4.0~\text{V, ID} = 3.0~\text{A)} \\ &\text{RdS(on)3} = 34~\text{m}\Omega~\text{MAX.}~\text{(VGS} = 2.5~\text{V, ID} = 3.0~\text{A)} \end{split}$$

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1801GR-9JG	Power TSSOP8

PACKAGE DRAWING (Unit:mm)

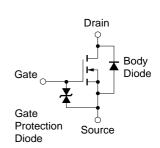




ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	Drain to Source Voltage	Voss	20	V
	Gate to Source Voltage	Vgss	±8.0	V
	Drain Current (DC)	ID(DC)	±6.0	Α
	Drain Current (pulse) Note1	D(pulse)	±24	Α
*	Total Power Dissipation Note2	PT	2.0	W
	Channel Temperature	Tch	150	°C
	Storage Temperature	T_{stg}	-55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on ceramic substrate of 5000 mm² x 1.1 mm

Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

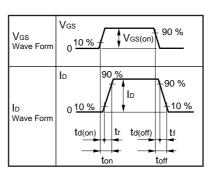


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

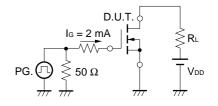
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vps = 20 V, Vgs = 0 V			10	μΑ
Gate Leakage Current	lgss	$V_{GS} = \pm 8.0 \text{V}, V_{DS} = 0 \text{V}$			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	0.5	0.7	1.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 3.0 A	1.0	13		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = 4.5 V, ID = 3.0 A		16	24	mΩ
	RDS(on)2	Vgs = 4.0 V, ID = 3.0 A		16.5	25	mΩ
	RDS(on)3	Vgs = 2.5 V, ID = 3.0 A		21	34	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		970		pF
Output Capacitance	Coss	V _G s = 0 V		700		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		320		pF
Turn-on Delay Time	td(on)	V _{DD} = 10 V		30		ns
Rise Time	tr	ID = 3.0 A		95		ns
Turn-off Delay Time	t d(off)	V _{GS(on)} = 4.0 V		90		ns
Fall Time	t _f	R _G = 10 Ω		100		ns
Total Gate Charge	Q _G	V _{DD} = 10 V		21		nC
Gate to Source Charge	Qgs	ID = 6.0 A		2		nC
Gate to Drain Charge	Q _{GD}	Vgs = 4.0 V		9		nC
Diode Forward Voltage	V _F (S-D)	IF = 6.0 A, VGS = 0 V		0.75		V
Reverse Recovery Time	trr	IF = 6.0 A, Vgs = 0 V		95		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μS		97		nC

TEST CIRCUIT 1 SWITCHING TIME

D.U.T. PG. RG VDD $\tau = 1 \mu s$ Duty Cycle $\leq 1 \%$



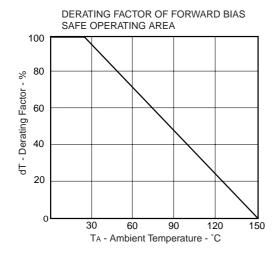
TEST CIRCUIT 2 GATE CHARGE

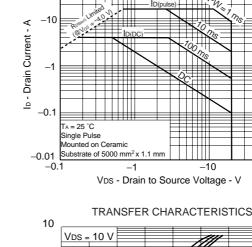


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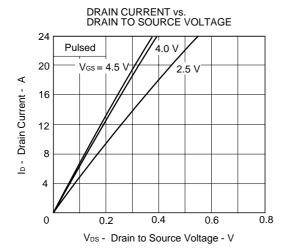
★ TYPICAL CHARACTERISTICS (TA = 25 °C)

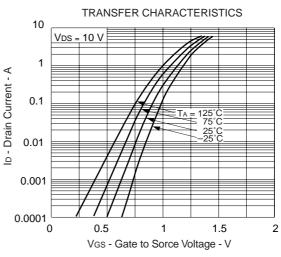


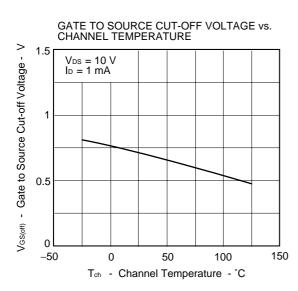


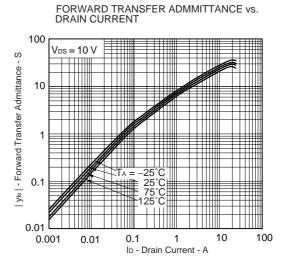
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FORWARD BIAS SAFE OPERATING AREA

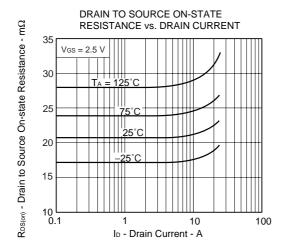


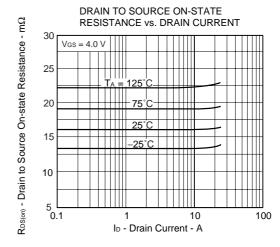


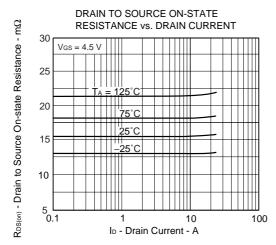


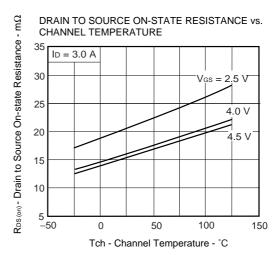


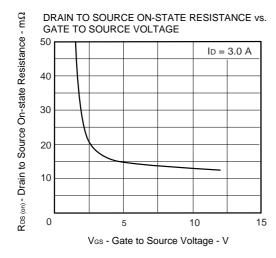
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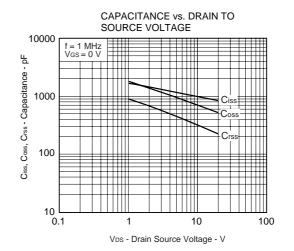




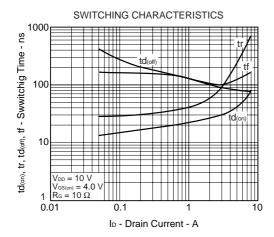


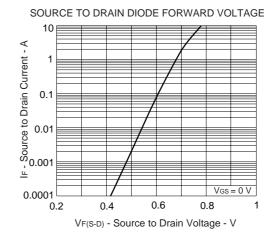


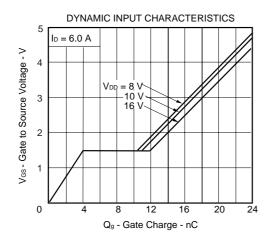




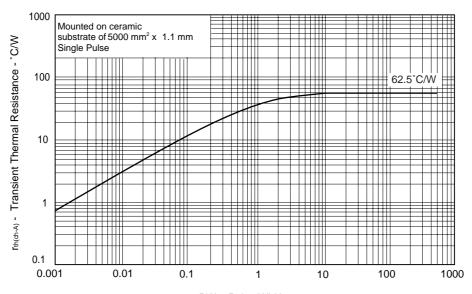








TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



PW - Pulse Width - s

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