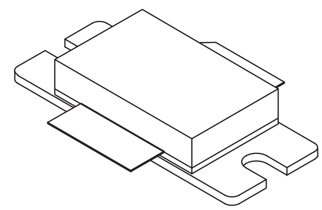
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19125
MRF19125S
MRF19125SR3

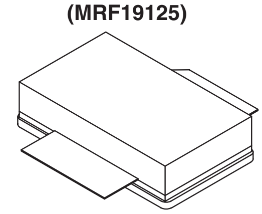
1990 MHz, 125 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical 2–Carrier N–CDMA Performance for V_{DD} = 26 Volts, I_{DQ} = 1300 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz
  IS–95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)
  1.2288 MHz Channel Bandwidth Carrier. Adjacent Channels Measured over a 30 kHz Bandwidth at f1 –885 kHz and f2 +885 kHz. Distortion Products Measured over 1.2288 MHz Bandwidth at f1 –2.5 MHz and f2 +2.5 MHz. Peak/Avg. = 9.8 dB @ 0.01% Probability on CCDF.
  Output Power — 24 Watts Avg.
  Power Gain — 13.6 dB
  Efficiency — 22%
  ACPR — –51 dB
  IM3 — –37.0 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1990 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465B–03, STYLE 1
(NI–880)
(MRF19125)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF19125S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	330 1.89	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

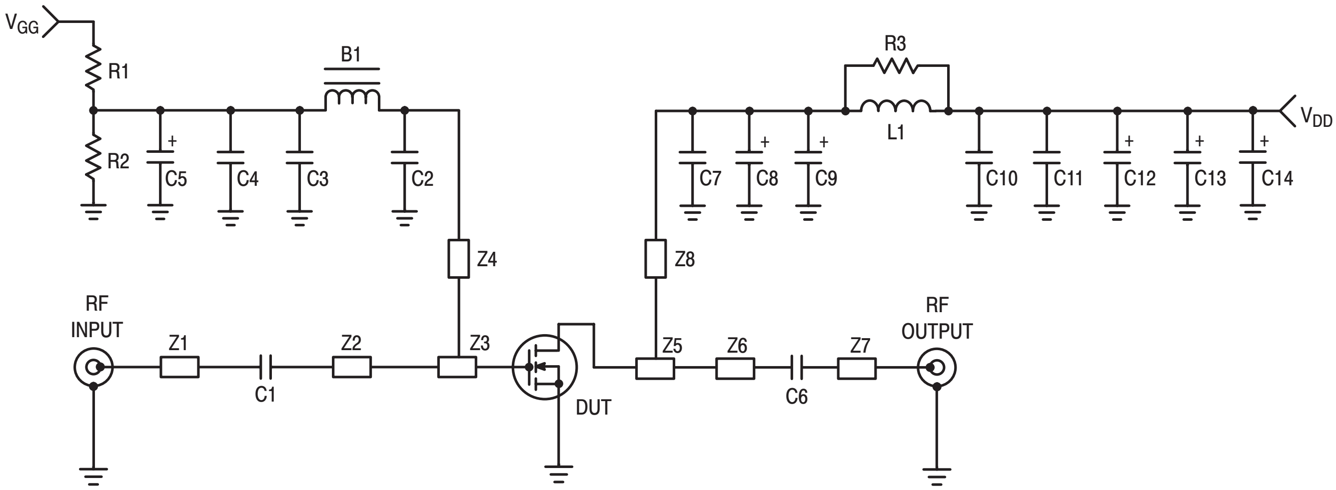
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	9	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 1300 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	0.185	0.21	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carriers. Peak/Avg = 9.8 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	G_{ps}	12	13.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	η	19	22	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; IM3 measured over 1.2288 MHz Bandwidth at f1 –2.5 MHz and f2 +2.5 MHz)	IMD	—	–37	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured over 30 kHz Bandwidth at f1 –885 MHz and f2 +885 MHz)	ACPR	—	–51	–47	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 125 W CW, I_{DQ} = 1300 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	—	13.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	η	—	35	—	%
Third Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–13	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 1300 mA, f = 1990 MHz)	P1dB	—	130	—	W



Z1, Z7	0.500″ x 0.084″ Microstrip	Board	0.030″ Glass Teflon®, Keene GX–0300–55–22, ε_r = 2.55
Z2	1.105″ x 0.084″ Microstrip	PCB	Etched Circuit Boards MRF19125 Rev. 5, CMR
Z3	0.360″ x 0.895″ Microstrip		
Z4	0.920″ x 0.048″ Microstrip		
Z5	0.605″ x 1.195″ Microstrip		
Z6	0.800″ x 0.084″ Microstrip		
Z8	0.660″ x 0.095″ Microstrip		

Figure 1. MRF19125 Test Circuit Schematic

Table 1. MRF19125 Test Circuit Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite #2743019447
C1	51 pF Chip Capacitor, ATC #100B510JCA500X
C2, C7	5.1 pF Chip Capacitors, ATC #100B5R1JCA500X
C3, C10	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C11	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	0.1 μF Tantalum Chip Capacitor, Kemet #T491C105M050
C6	10 pF Chip Capacitor, ATC #100B100JCA500X
C8	10 μF Tantalum Chip Capacitor, Kemet #T491X106K035AS4394
C9, C12, C13, C14	22 μF Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100″ ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052–1648–10
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	220 kΩ, 1/8 W Chip Resistor
R3	10 Ω, 1/8 W Chip Resistor

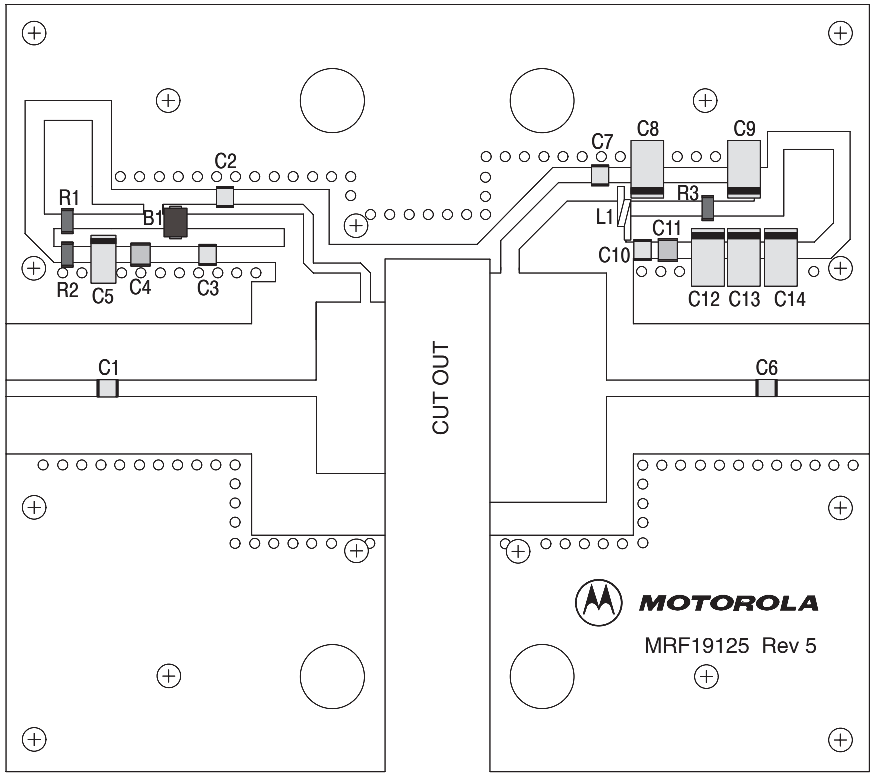


Figure 2. MRF19125 Test Circuit Component Layout

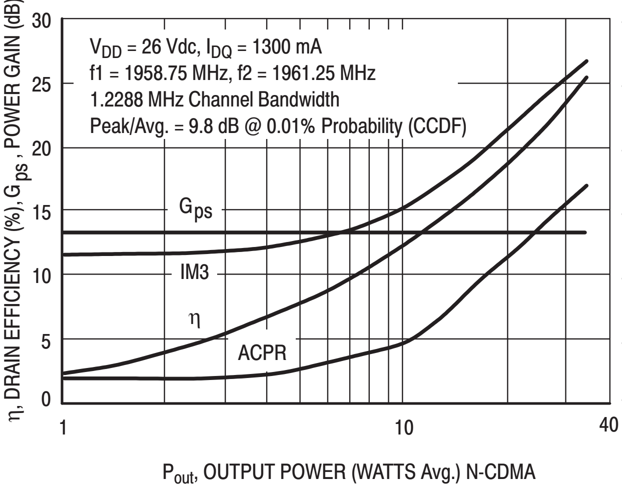


Figure 3. 2-Carrier CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

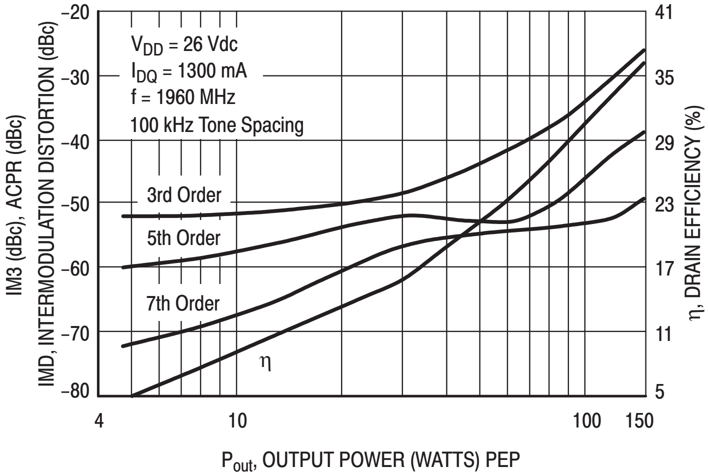


Figure 4. Intermodulation Distortion Products versus Output Power

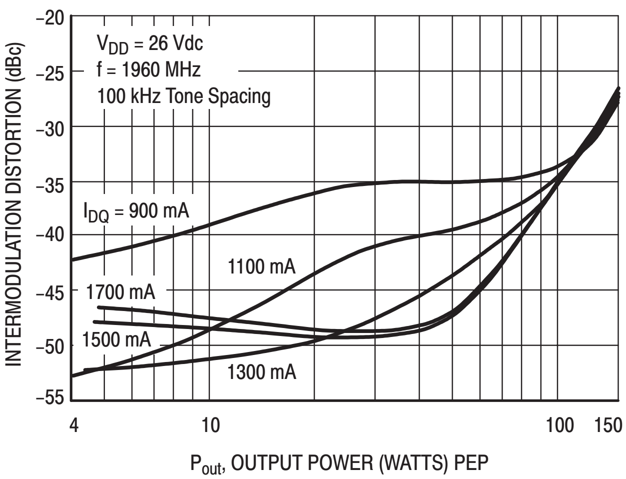


Figure 5. Third Order Intermodulation Distortion versus Output Power

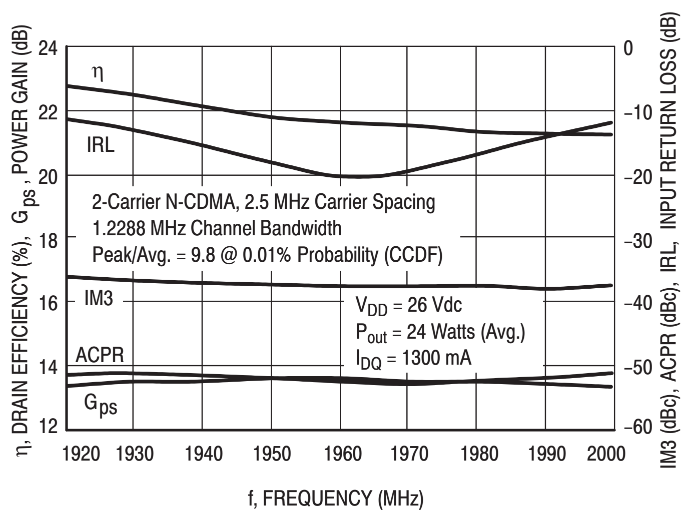


Figure 6. 2-Carrier N-CDMA Broadband Performance

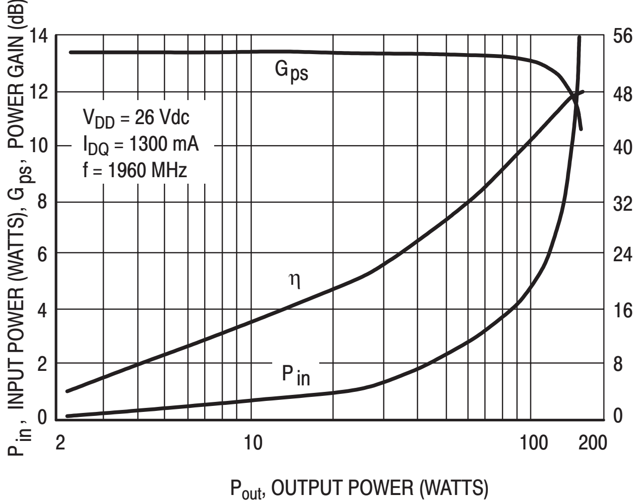


Figure 7. CW Performance

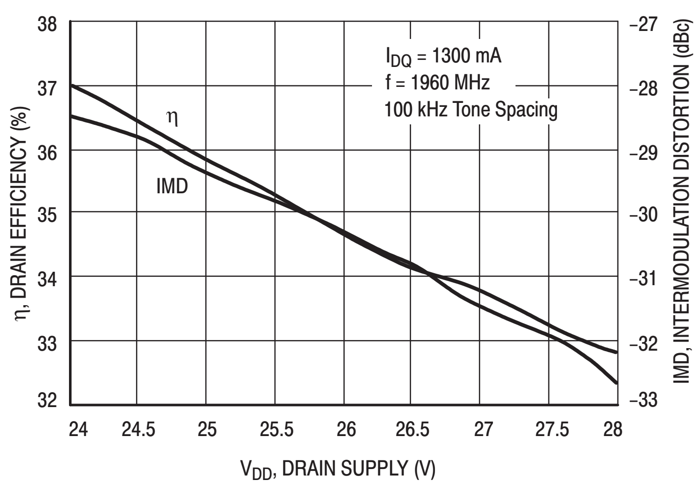


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

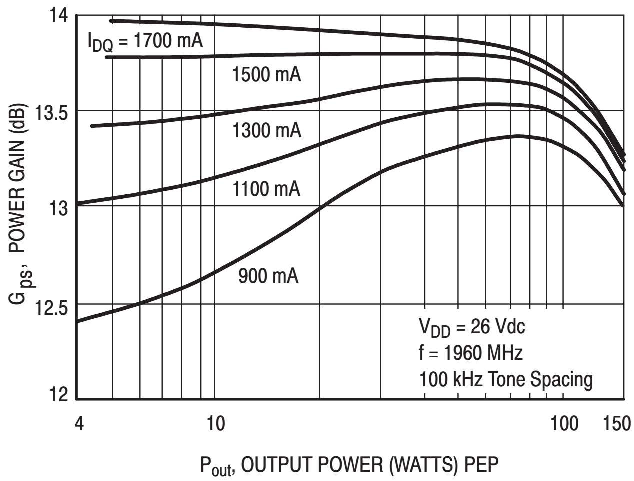


Figure 9. Two-Tone Power Gain versus Output Power

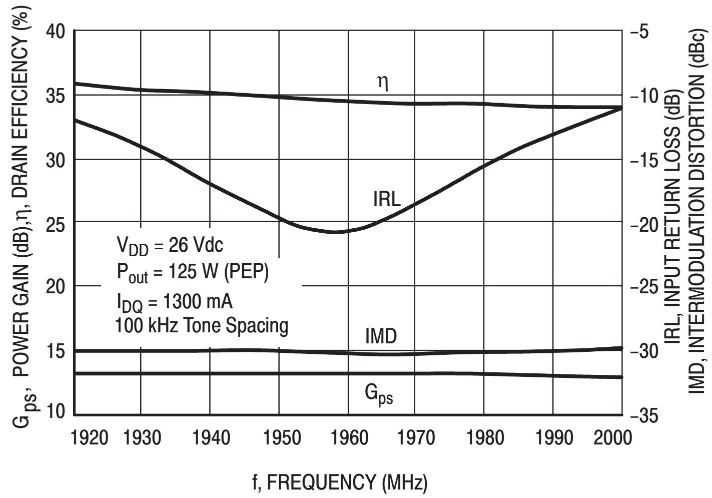


Figure 10. Two-Tone Broadband Performance

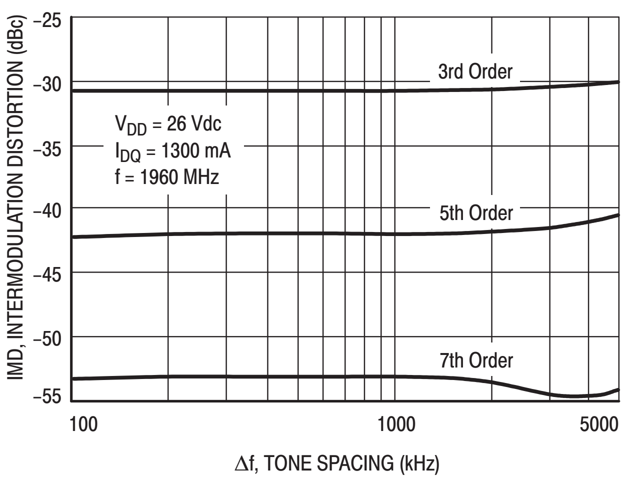


Figure 11. Intermodulation Distortion Products versus Two–Tone Tone Spacing

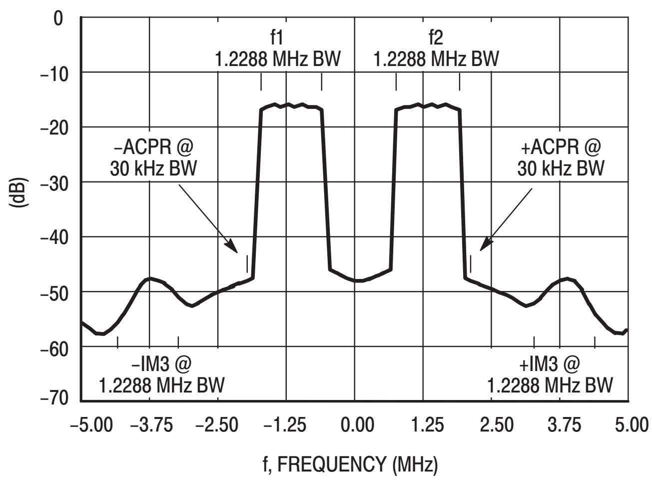
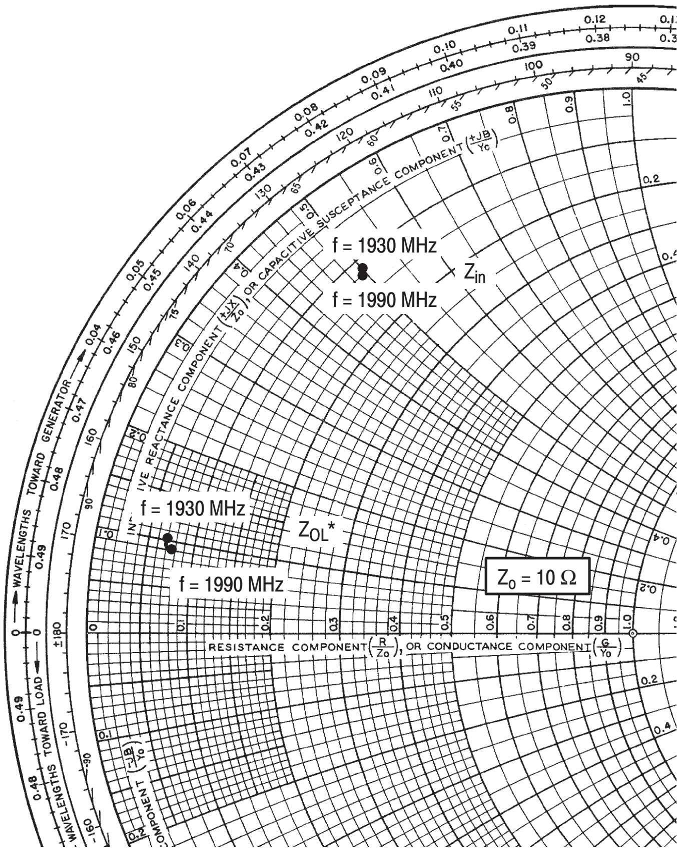


Figure 12. 2-Carrier N-CDMA Spectrum



V_{DD} = 26 V, I_{DQ} = 1300 mA, P_{out} = 24 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	1.43 + j5.01	0.75 + j0.93
1960	1.51 + j4.88	0.71 + j0.89
1990	1.56 + j4.93	0.68 + j1.02

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

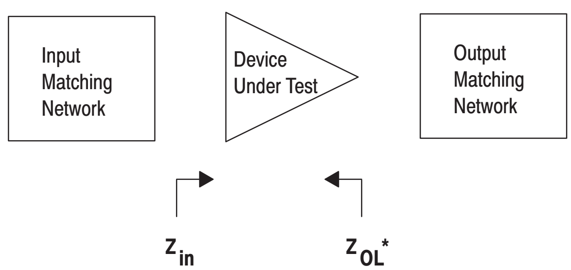
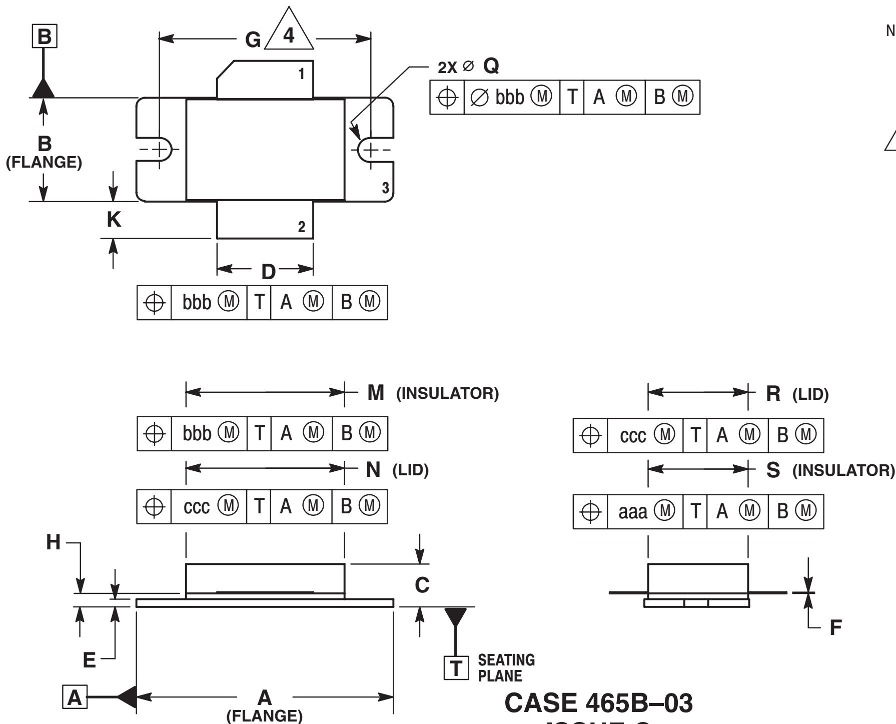


Figure 13. Series Equivalent Input and Output Impedance

NOTES

NOTES

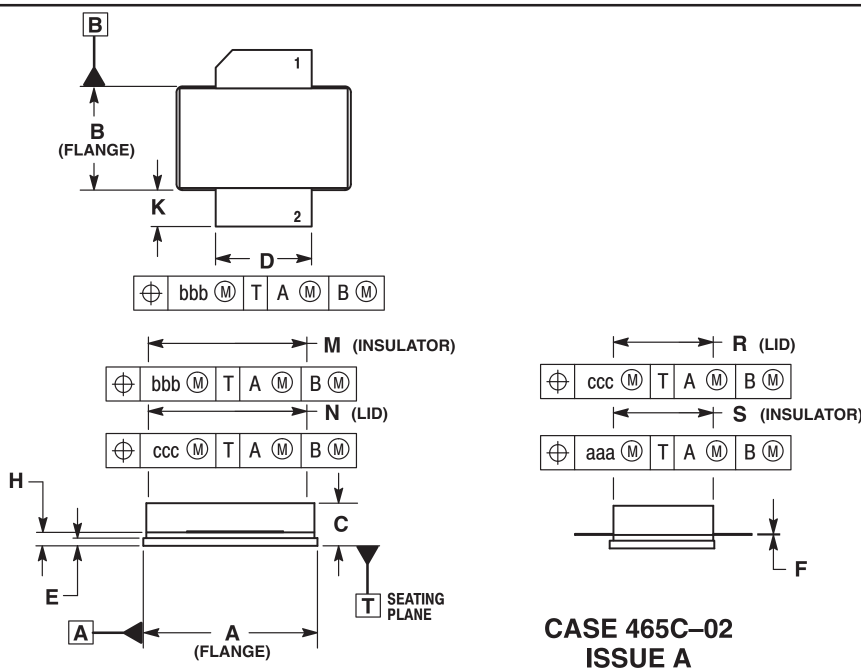


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–03
ISSUE C
(NI–880)
(MRF19125)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–02
ISSUE A
(NI–880S)
(MRF19125S)

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

HOME PAGE: http://www.motorola.com/semiconductors/

MOTOROLA