FLASH MEMORY

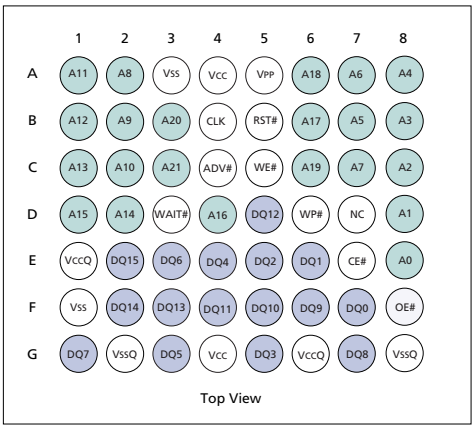
MT28F644W18
MT28F644W30

1.8V Low Voltage, Extended Temperature

Features

- Flexible 4Mb multipartition architecture
- Single word (16-bit) data bus
- Support for true concurrent operation with zero latency
- Basic configuration:
  135 individually programmable/erasable blocks
  16 Partitions (4Mb each for code and data storage)
- VCC, VCCQ, VPP voltages
  1.65V (MIN)–1.95V (MAX) VCC
  1.65V (MIN)–2.24V (MAX) VCCQ (W18)
  1.65V (MIN)–3.3V (MAX) VCCQ (W30)
  1.8V (TYP) VPP (in-system PROGRAM/ERASE)
  12V ±5% (HV) VPP tolerant (factory programming compatibility)
- Asynchronous Access Time
  Random access time: 60ns @ 1.65V VCC (W18)
  Random access time: 70ns @ 1.65V VCC (W30)
- Burst mode read access
  MAX clock rate: 66 MHz (^{t}CLK = 15ns) (W18)
  MAX clock rate: 54 MHz (^{t}CLK = 18.5ns) (W30)
  Burst latency 60ns @1.65V VCC and 66 MHz
  Burst latency 70ns @1.65V VCC and 54 MHz
  4 word, 8 word, and continuous burst modes
  ^{t}ACLK: 11ns @ 1.65V VCC and 66 MHz (W18)
  ^{t}ACLK: 14ns @ 1.65V VCC and 54 MHz (W30)
- Page mode read access
  Interpage read access: 60ns @ 1.65V VCC (W18)
  Intrapage read access: 15ns @ 1.65V VCC (W18)
  Interpage read access: 70ns @ 1.65V VCC (W30)
  Intrapage read access: 22ns @ 1.65V VCC (W30)
- Low power consumption (VCC = 1.95V)
  Burst read @ 66 MHz <8mA (TYP) (W18)
  Burst read @ 54 MHz <6mA (TYP) (W30)
  Standby <7µA (TYP)
  Automatic power save (APS)
- Enhanced write and erase suspend options
  ERASE-SUSPEND-to-READ within same partition
  PROGRAM-SUSPEND-to-READ within same partition
  ERASE-SUSPEND-to-PROGRAM within same partition
- Dual 64-bit chip protection registers for security purposes
- Cross-compatible command support
  Extended command set
  Common flash interface
- Programmable WAIT# configuration
- Clock suspend
- 100,000 ERASE cycles per block
- Fast programming algorithm (FPA)
- Manufacturer's ID (ManID)
  Micron® (0x2Ch)
  Intel® (0x89h)

Figure 1: 56-Ball VFBGA



NOTE:
1. See Table 3 for ball descriptions.
2. See Figure 35 for mechanical drawing.

Options / Marking

• Timing	
60ns access	-60
70ns access	-70
80ns access	-80
• Burst Frequency	
66 MHz[1]	6
54 MHz	5
40 MHz	4
• Boot Block Configuration	
Top	T
Bottom	B
• I/O Voltage Range	
VccQ 1.70V–1.95V	18
VccQ 1.70V–3.3V	30
• Manufacturer's ID (ManID)	
Micron (0x2Ch)	None
Intel (0x89h)	K
• Package	
56-ball VFBGA (7 x 8 ball grid)	FE
• Operating Temperature Range	
Extended (-40ºC to +85ºC)	ET

NOTE:
1. Contact factory for availability.

Part Number Example:
MT28F644W30FE-705 TET

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General Description

The MT28F644W18/W30 is a high-performance, high-density, nonvolatile memory solution that can significantly improve system performance. This new architecture features a multipartition configuration that supports READ-while-PROGRAM/ERASE operations with no latency. A 4Mb partition size enables optimal design flexibility.

A high-performance bus interface enables a fast burst mode READ operation; a conventional asynchronous/page bus interface is provided as well. The burst interface increases the data throughput, minimizing the impact of the first data latency.

The MT28F644W18/W30 enables soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, two 64-bit chip protection registers are provided.

The embedded WORD PROGRAM and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip device status register can be used to monitor the WSM status and determine the progress of the PROGRAM/ERASE tasks.

The MT28F644W18/W30 is offered with two manufacturing identifiers (ManID), Micron (0x2Ch) and Intel (0x89h). this option provides flexibility for the customer's design.

Please refer to Micron's Web site at www.micron.com/flash for the latest data sheet.

Architecture and Memory Organization

The MT28F644W18/W30 Flash device contains sixteen separate partitions of memory for simultaneous READ and PROGRAM/ERASE operations. Burst READs can cross partition boundaries, but the user must ensure that the burst does not extend into a partition that is actively programming or erasing. During a PROGRAM/ERASE operation, any of the fifteen other partitions may be read. Note that only two partitions can operate simultaneously. Partitions are configured as follows:

- Partition 0 (bottom boot) or partition 15 (top boot) contains eight 4K-word parameter blocks and seven 32K-word main blocks.
- The other 15 partitions contain eight 32K-word main blocks and comprise one-sixteenth of the total memory.

Figure 3 depicts the memory organization.

Figure 2: Functional Block Diagram

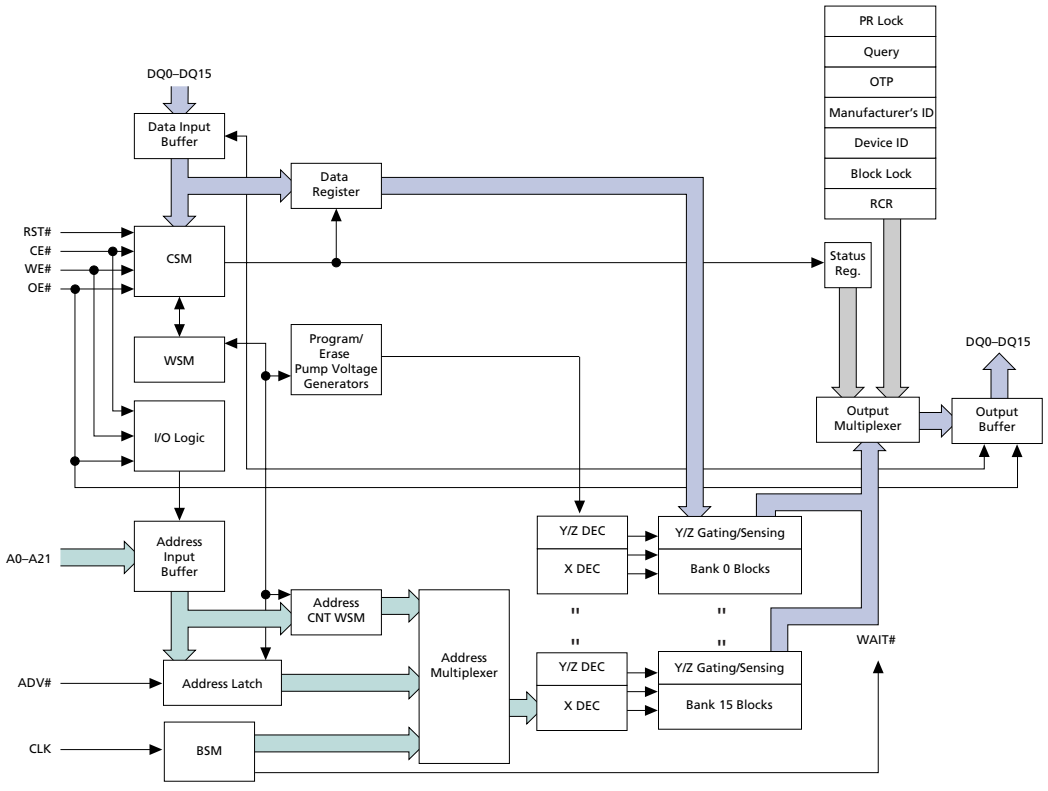


Figure 3: Memory Organization

Bottom Boot Block Device

		SIZE (K-words)	BLOCK #	64Mb
Partition 15		32	134	3F8000h–3FFFFFh
		. . .	. . .	. . .
		32	127	3C0000h–3C7FFFh
Partition 14		32	126	3B8000–3BFFFFh
		. . .	. . .	. . .
		32	119	380000h–387FFFh
. . .		32	. . .	
		. . .	. . .	. . .
		32		
Partition 3		32	38	0F8000h–0FFFFFh
		. . .	. . .	. . .
		32	31	0C0000h–0C7FFFh
Partition 2		32	30	0B8000h–0BFFFFh
		. . .	. . .	. . .
		32	23	080000h–087FFFh
Partition 1		32	22	078000h–07FFFFh
		. . .	. . .	. . .
		32	15	040000h–047FFFh
Partition 0		32	14	038000h–03FFFFh
		. . .	. . .	. . .
		32	8	008000h–00FFFFh
	Parameter	4	7	007000h–007FFFh
		. . .	. . .	. . .
		4	0	000000h–000FFFh

Top Boot Block Device

		SIZE (K-words)	BLOCK #	64Mb
Partition 15	Parameter	4	134	3FF000h–3FFFFFh
		. . .	. . .	. . .
		4	127	3F8000h–3F8FFFh
		32	126	3F0000–3F7FFFh
		. . .	. . .	. . .
		32	120	3C0000h–3C7FFFh
Partition 14		32	119	3B8000h–3BFFFFh
		. . .	. . .	. . .
		32	112	380000h–387FFFh
Partition 13		32	111	378000h–37FFFFh
		. . .	. . .	. . .
		32	104	340000h–347FFFh
Partition 12		32	103	338000h–33FFFFh
		. . .	. .	. .
		32	96	300000h–307FFFh
		32	. . .	. . .
		. .	. .	. .
		32	. . .	. . .
Partition 1		32	15	078000h–07FFFFh
		. .	. .	. .
		32	8	040000h–047FFFh
Partition 0		32	7	038000h–03FFFFh
		. . .	. . .	. . .
		32	0	000000h–007FFFh

NOTE:

Total number of blocks: 8 parameter + 127 main = 135.

Device Marking

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross referenced to the Micron part numbers in Table 1.

Table 1: Cross Reference for Abbreviated Device Marks

PRODUCT PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL MARKING
MT28F644W18FE-606 BET	FW100	FX100	FY100
MT28F644W18FE-606 TET	FW112	FX112	FY112
MT28F644W18FE-606 KBET	FW115	FX115	FY115
MT28F644W18FE-606 KTET	FW116	FX116	FY116
MT28F644W18FE-70 TET	FW101	FX101	FY101
MT28F644W18FE-70 BET	FW102	FX102	FY102
MT28F644W18FE-705 BET	FW113	FX113	FY113
MT28F644W18FE-705 TET	FW114	FX114	FY114
MT28F644W18FE-705 KTET	FW117	FX117	FY117
MT28F644W18FE-705 KBET	FW118	FX118	FY118
MT28F644W30FE-70 BET	FW121	FX121	FY121
MT28F644W30FE-70 TET	FW103	FX103	FY103
MT28F644W30FE-705 TET	FW104	FX104	FY104
MT28F644W30FE-705 BET	FW108	FX108	FY108
MT28F644W30FE-705 KTET	FW119	FX119	FY119
MT28F644W30FE-705 KBET	FW120	FX120	FY120
MT28F644W30FE-804 TET	FW110	FX110	FY110
MT28F644W30FE-804 BET	FW109	FX109	FY109

Part Numbering Information

Micron's low-power devices are available with several different combinations of features (see Figure 4). Valid combinations of features and their corresponding part numbers are listed in Table 2.

Figure 4: Part Number Chart

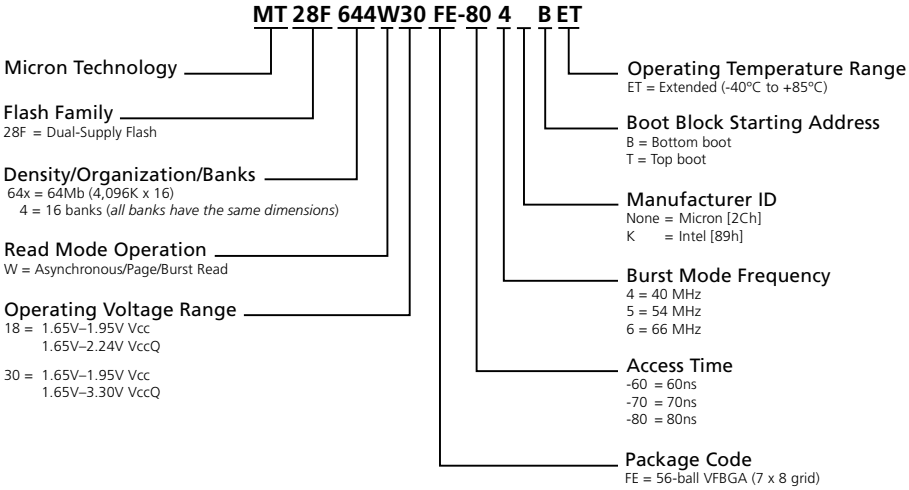


Table 2: Valid Part Number Combinations

PART NUMBER	ManID	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	BURST FREQUENCY (MHz)	OPERATING TEMPERATURE RANGE
MT28F644W18FE-606 BET	Micron	60	Bottom	66	-40°C to +85°C
MT28F644W18FE-606 TET	Micron	60	Top	66	-40°C to +85°C
MT28F644W18FE-606 KBET	Intel	60	Bottom	66	-40°C to +85°C
MT28F644W18FE-606 KTET	Intel	60	Top	66	-40°C to +85°C
MT28F644W18FE-70 TET	Micron	70	Top	NA	-40°C to +85°C
MT28F644W18FE-70 BET	Micron	70	Bottom	NA	-40°C to +85°C
MT28F644W18FE-705 BET	Micron	70	Bottom	54	-40°C to +85°C
MT28F644W18FE-705 TET	Micron	70	Top	54	-40°C to +85°C
MT28F644W18FE-705 KTET	Intel	70	Top	54	-40°C to +85°C
MT28F644W18FE-705 KBET	Intel	70	Bottom	54	-40°C to +85°C
MT28F644W30FE-70 BET	Micron	70	Bottom	NA	-40°C to +85°C
MT28F644W30FE-70 TET	Micron	70	Top	NA	-40°C to +85°C
MT28F644W30FE-705 TET	Micron	70	Top	54	-40°C to +85°C
MT28F644W30FE-705 BET	Micron	70	Bottom	54	-40°C to +85°C
MT28F644W30FE-705 KTET	Intel	70	Top	54	-40°C to +85°C
MT28F644W30FE-705 KBET	Intel	70	Bottom	54	-40°C to +85°C
MT28F644W30FE-804 TET	Micron	80	Top	40	-40°C to +85°C
MT28F644W30FE-804 BET	Micron	80	Bottom	40	-40°C to +85°C

Table 3: Ball Descriptions

58-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
E8, D8, C8, B8, A8, B7, A7, C7, A2, B2, C2, A1, B1, C1, D2, D1, D4, B6, A6, C6, B3, C3	A0–A21	Input	Address inputs: Inputs for the addresses during READ and WRITE operations. All addresses are internally latched during WRITE cycles and synchronous READ cycles. During asynchronous READ cycles, A0–A2 are not internally latched.
B4	CLK	Input	Clock: Synchronizes the Flash device to the system operating frequency during burst mode READ operations. When configured for burst mode READs, address is latched on the first rising (or falling, depending upon the read configuration register setting) CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. CLK is ignored during asynchronous page access READ and WRITE operations.[1]
C4	ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses are latched on the rising edge of ADV# during READ operations.[1]
E7	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device goes into standby power mode if neither PROGRAM nor ERASE operations are pending.
F8	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
C5	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command state machine (CSM) or to the memory array.
B5	RST#	Input	Reset: When RST# is a logic LOW, the device is in reset mode, which drives the outputs to High-Z and resets the write state machine. When RST# is at logic HIGH, the device is in standard operation. When RST# transitions from logic LOW to logic HIGH, the device resets all blocks to locked and defaults to the read array mode.
D6	WP#	Input	Write Protect: Controls the lock down function of the flexible locking feature.
F7, E6, E5, G5, E4, G3, E3, G1, G7, F6, F5, F4, D5, F3, F2, E2	DQ0–DQ15	Input/ Output	Data Inputs/Outputs: Inputs array data on the second CE# and WE# cycle during PROGRAM operation. Inputs commands to the command user interface when CE# and WE# are active. DQ0–DQ15 output data when CE# and OE# are active.
D3	WAIT#	Output	Wait: Provides data valid feedback during continuous burst read access. The signal is gated by CE#. The WAIT# signal polarity is set by RCR10 in the RCR.
A4, G4	V_{CC}	Supply	Device Power Supply: [1.65V–1.95V] Supplies power for device operation.
E1, G6	V_{CCQ}	Supply	I/O Power Supply: [1.65V–3.3V for W30] Supplies power for input/output buffers. I/O Power Supply: [1.65V–2.24V for W18] Supplies power for input/output buffers.
G2, G8	V_{SSQ}	Supply	I/O Ground: Do not float any ground ball.
A3, F1	V_{SS}	Supply	Supply Ground: Do not float any ground ball.
D7	NC	–	Internally not connected.
A5	V_{PP}	Supply/ Input	Program/Erase Enable: [0.9V–1.95V or 11.4V–12.6V] Operates as input at logic levels to control complete device protection. Provides factory programming compatibility, and acts as a current source, when driven to 11.4V–12.6V.

NOTE:
1. The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous/page mode.

Command State Machine (CSM)

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between external microprocessors and the internal write state machine (WSM). Table 5 defines the available commands and provides data for each of the bus cycles, and Table 6 provides the command descriptions. Program and erase algorithms are automated by an on-chip WSM. During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested. Table 27 on page 64 shows the CSM transition states.

Once a valid PROGRAM/ERASE command is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally to accomplish the requested operation. A command is valid only if the exact sequence is completed. After the WSM completes its task, the WSM status bit (SR7) (see Table 7) is set to a logic HIGH level (VIH), allowing the CSM to respond to the full command set again.

Command State Machine Activation

Device operations are selected by entering an 8-bit command code with conventional microprocessor timings into an on-chip CSM through I/Os DQ0–DQ7. The number of bus cycles required to activate a command is typically one or two. The first operation is always a WRITE. Control signals CE# and WE# must be at a logic LOW level (VIL), and OE# and RST# must be at logic HIGH (VIH). The second operation, when needed, can be a WRITE or a READ, depending upon the command. During a READ operation, control signals CE#, ADV#, and OE# must be at a logic LOW level (VIL), and WE# and RST# must be at logic HIGH (VIH). Table 4 illustrates the bus operations for all the modes: write, read, reset, standby, and output disable.

When the device is reset, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. Users can verify the status of the operations initiated by the CSM by reading the status register. This single status register permits monitoring of the progress of the various operations that can take place on a memory partition. Status register bits SR0–SR7 correspond to DQ0–DQ7 (see Table 7).

Table 4: Bus Operations

MODE	RST#	CE#	ADV#	OE#	WE#	WAIT#	DQ0–DQ15
Read (array, status registers, device identifier, or query)	VIH	VIL	VIL	VIL	VIH	Active[1]	DOUT
Standby	VIH	VIH	X	X	X	High-Z	High-Z
Output disable	VIH	VIL	X	VIH	VIH	Active[1]	High-Z
Reset	VIL	X	X	X	X	High-Z	High-Z
Write	VIH	VIL	X	VIH	VIL	High-Z	DIN

NOTE:

1. The WAIT# signal is driven by CE#; polarity depends on RCR10. Valid only in synchronous mode only.

Table 5: Command Sequencing

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE		
	OPERATION	ADDRESS[1]	DATA	OPERATION	ADDRESS[1]	DATA[1]
READ ARRAY	WRITE	PnA	FFh			
READ DEVICE IDENTIFIER	WRITE	PnA	90h	READ	BBA + IA	IC
READ QUERY	WRITE	PnA	98h	READ	PBA + QA	QD
READ STATUS REGISTER	WRITE	PnA	70h	READ	BA	SRD
CLEAR STATUS REGISTER	WRITE	XX	50h			
BLOCK ERASE SETUP	WRITE	BA	20h	WRITE	BA	D0h
PROGRAM SETUP	WRITE	WA	40h/10h	WRITE	WA	WD
FAST PROGRAMMING ALGORITHM	WRITE	WA	30h	WRITE	WA	D0h
PROGRAM/ERASE SUSPEND	WRITE	XX	B0h			
PROGRAM/ERASE RESUME	WRITE	XX	D0h			
LOCK BLOCK	WRITE	BA	60h	WRITE	BA	01h
UNLOCK BLOCK	WRITE	BA	60h	WRITE	BA	D0h
LOCK-DOWN BLOCK	WRITE	BA	60h	WRITE	BA	2Fh
PROTECTION PROGRAM	WRITE	PA	C0h	WRITE	PA	PD
LOCK PROTECTION PROGRAM	WRITE	LPA	C0h	WRITE	LPA	FFFDh
SET READ CONFIGURATION REGISTER	WRITE	RCRV	60h	WRITE	RCRV	03h

NOTE: 1. BA:Address within the block.
IA: Identification code address.
IC:Identifier code data.
ID: Identification code data.
BBA: Block base address. The first address of a particular block.
LPA: Lock protection register address (BBA + 80h).
PA: Protection register address.
PBA:Partition base address. The very first address of a particular partition.
PD: Data to be written at location PA.
PnA:Any address within a specific partition.
QA: Query code address.
QD: Query code data DQ[7:0].
RCRV: Data to be written into the read configuration register presented on A15–A0.
SRD: Data read from the status register.
WA: Word address of memory location to be written.
WD: Data to be written at the location WA.
XX: Any valid address within the device.

Table 6: Command Codes and Descriptions

OPERATION	CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
READ	FFh	Read Array	First	Places the addressed partition in read array mode.
	70h	Read Status Register	First	This command places the addressed partition into read status register mode. Reading the partition will output the contents of the status register for the addressed partition. The device will automatically enter this mode for the addressed partition after a PROGRAM or ERASE operation has been initiated.
	90h	Read Device Identifier	First	Puts the addressed partition into the read device identifier mode so that reading the device will output the manufacturer's/ device codes, configuration register data, block lock status, or protection register data on DQ0–DQ15.
	98h	Read Query	First	Puts the addressed partition into the read query mode so that reading the partition will output common flash interface information.
	50h	Clear Status Register	First	The WSM can set the block lock status (SR1), V_{PP} status (SR3), program status (SR4), and erase status (SR5) bits in the status register to "1," but it cannot clear them to "0." SR1, SR3, SR4, and SR5 can only be cleared by a device reset or by using the CLEAR STATUS REGISTER command.
PROGRAM	40h	Program Setup	First	A two-cycle command: The first cycle prepares for a PROGRAM operation, and the second cycle latches addresses and data and initiates the WSM to execute the program algorithm. After the second cycle, the device outputs status register data on the falling edge of OE# or CE#, whichever occurs last.
	10h	Program Setup	First	Equivalent to Program Setup (40h).
	30h	FPA Setup	First	This program command activates FPA mode. The first write cycle sets up the command. If the second cycle is an FPA CONFIRM COMMAND (D0h), subsequent WRITEs provide program data. All other commands are ignored once FPA mode begins.
	D0h	FPA Confirm	Second	If the previous command was FPA SETUP (30h), the CSM latches the address and data and prepares the device for FPA mode.
ERASE	20h	Erase Setup	First	Prepares the CSM for the ERASE CONFIRM command. If the next command is not ERASE CONFIRM, the CSM will set both SR4 and SR5 of the status register to a "1," place the partition into read status register mode, and wait for another command.
	D0h	Erase Confirm	Second	If the previous command was an ERASE SETUP command, then the CSM will close the address and data latches, and it will begin erasing the block indicated on the address pins. The device will then output status register data on the falling edge of OE# or CE#, whichever occurs last.
SUSPEND	B0h	Program/Erase Suspend	First	Issuing this command will suspend the currently executing PROGRAM/ERASE operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR2) or erase suspend (SR6), and the WSM status bit (SR7) to a "1" (ready). The WSM will continue to idle in the suspend state, regardless of the state of all input control signals except RST#, which will reset the WSM and the remainder of the chip if RST# is driven to V_{IL}.
	D0h	Program/Erase Resume	First	If a PROGRAM or ERASE operation is suspended (as indicated by SR2 or SR6), this command will resume the operation.

Table 6: Command Codes and Descriptions (continued)

OPERATION	CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
BLOCK LOCKING	60h	Block Lock Setup	First	Prepares the CSM for changes to the block locking status. See note 1.
	01h	Lock Block	Second	If the previous command was BLOCK LOCK SETUP, the CSM will latch the address and lock the block indicated on the address bus.
	D0h	Unlock Block	Second	If the previous command was BLOCK LOCK SETUP, the CSM will latch the address and unlock the block indicated on the address bus. If the block had been previously set to lock down, this operation will have no effect unless WP# is driven to V_{IH}.
	2Fh	Lock Down Block	Second	If the previous command was BLOCK LOCK SETUP, the CSM will latch the address and lock down the block indicated on the address bus.
PROTECTION PROGRAM	C0h	Protection Register Program Setup	First	Prepares the CSM for a PROTECTION REGISTER PROGRAM operation. The second cycle latches address and data, and starts the WSM's protection register program or lock algorithm. After the second cycle, the device outputs status register data on the falling edge of OE# or CE#, whichever occurs last. To read array data after programming, issue a READ ARRAY command.
SET READ CONFIGURATION REGISTER	60h	Set Read Configuration Register Setup	First	Prepares the RCR to be modified. See note 1.
	03h	Set Read Configuration Register Data	Second	If the previous command was SET READ CONFIGURATION REGISTER SETUP, the configuration bits presented on the address bus will be stored into the Read Configuration Register.

NOTE:
1. If the 60h command is not followed by D0h, 01h, 2Fh, or 03h, the CSM sets SR4 and SR5 to indicate a command sequence error.

Status Register

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete.

During periods when the WSM is active in a partition, that partition will default to the read status register mode and can be polled to determine the WSM status.

After monitoring the status register during a PROGRAM/ERASE operation in a partition, that partition will remain in read status mode until a new command is issued to the CSM. Table 7 defines the status register bits.

Clear Status Register

The internal circuitry can set, but not clear, the block lock status bit (SR1), the VPP status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to the internal operations. When the status bits are cleared, the state of the device does not change.

Table 7 Status Register Bit Definitions

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	SR7 indicates ERASE or PROGRAM completion in the device. SR6–SR1 are invalid while SR7 = 0. See Table 8 for valid SR7 and SR0 combinations.
SR6	ERASE SUSPEND STATUS 1 = BLOCK ERASE Suspended 0 = BLOCK ERASE in Progress/ Completed	When ERASE SUSPEND is issued, WSM halts execution and sets both SR7 and SR6 bits to "1." SR6 bit remains set to "1" until an ERASE RESUME command is issued.
SR5	ERASE STATUS 1 = Error in Block Erasure 0 = Successful BLOCK ERASE	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
SR4	PROGRAM STATUS 1 = Error in PROGRAM 0 = Successful PROGRAM	When this bit is set to "1," WSM has attempted but failed to program a word.
SR3	VPP STATUS 1 = VPP Low Detect, Operation Abort 0 = VPP = OK	The VPP status bit does not provide continuous indication of the VPP level. The WSM interrogates the VPP level only after the PROGRAM or ERASE command sequences have been entered and informs the system if VPP is LOW. The VPP level is also checked before the PROGRAM/ERASE is verified by the WSM.
SR2	PROGRAM SUSPEND STATUS 1 = PROGRAM Suspended 0 = PROGRAM in Progress/Completed	When PROGRAM SUSPEND is issued, WSM halts execution and sets both SR7 and SR2 bits to "1." SR2 bit remains set to "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS 1 = PROGRAM/ERASE Attempted on a Locked Block; Operation Aborted 0 = No Operation to Locked Blocks	If a PROGRAM or ERASE operation is attempted to a locked block, SR1 is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR0	FAST PROGRAMMING ALGORITHM STATUS 0 = Partition is busy, but only if SR7 = 0 1 = Another partition is busy, but only if SR7 = 0	Addressed partition is erasing or programming. In FPA mode, SR0 indicates a data stream word has finished programming or verifying, depending on the FPA phase. Refer to Table 8 for valid SR7 and SR0 combinations.

Table 8: Status Register SR7 and SR0 Description

SR7	SR0	DESCRIPTION
0	0	The addressed partition is performing a PROGRAM/ERASE operation. FPA: Device is finished programming or verifying data or is ready for data.
0	1	A partition other than the one currently addressed is performing a PROGRAM/ERASE operation. FPA: the device is either programming or verifying data.
1	0	No PROGRAM/ERASE operation is in progress in any partition. Erase and program suspend bits (SR6 and SR2) indicate whether other partitions are suspended.
1	1	Will not occur in standard PROGRAM/ERASE operations. FPA: This combination will not occur.

READ Operations

The following READ operations are available: READ ARRAY, READ DEVICE IDENTIFIER, READ QUERY, and READ STATUS REGISTER.

Note that READ DEVICE IDENTIFIER, READ QUERY, and READ STATUS REGISTER will read in either asynchronous or single burst mode.

Read Array

The array is read by entering the command code FFh on DQ0–DQ7 to each partition to be read. Control signals CE#, ADV#, and OE# must be at a logic LOW level (V_{IL}) and WE# and RST# must be at a logic HIGH level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15. Upon device reset, all partitions default to the read array mode. To return the addressed partition to read array mode, write the read array command code (FFh) on DQ0–DQ7.

Read Device Identifier

The read device identifier mode outputs five types of information: the manufacturer and device identifier, the block locking status, the read configuration register, and the protection register data. Two bus cycles are required for this operation: device identifier data is read by entering the command code 90h on DQ0–DQ7 and the identification code address on the address lines. Control signals CE#, ADV#, and OE# must be at a logic LOW level (V_{IL}), and WE# and RST# must be at a logic HIGH level (V_{IH}) to read device identifier data. Data is available on DQ0–DQ15. To return the addressed partition to read array mode, write the read array command code (FFh) on DQ0–DQ7. See Table 15 on page 37 for more details.

Read Query

The read query mode outputs common flash interface (CFI) data when the device is read. (See Table 26 on page 60 for more information.) Two bus cycles are required for this operation. It is possible to access the query by writing the read query command code 98h on DQ0–DQ7. Control signals CE#, ADV#, and OE# must be at a logic LOW level (V_{IL}) and WE# and RST# must be at a logic HIGH level (V_{IH}) to read data from the query. The CFI data structure contains information such as block size, density, command set, and electrical specifications. To return the addressed partition to read array mode, write the read array command code (FFh) on DQ0–DQ7.

Read Status Register

The status register provides the status of the device to the external microprocessor. The status register is read by entering the command code 70h on DQ0–DQ7. The address for both cycles must be in the same partition. Status register data is updated and latched on the falling edge of OE#, on the falling edge of CE#, or on the clock edge which starts a burst (whichever occurs last). See “Burst Read Mode” on page 17 for burst operation. Latching the data prevents errors from occurring if the register input changes while monitoring the status register.

The status register outputs the data on DQ0–DQ7. Table 7 contains the status register definitions.

To return the addressed partition to read array mode, write the read array command code (FFh) on DQ0–DQ7.

Read Modes

The MT28F644W18/W30 supports two read configurations: asynchronous/page mode and burst mode. The RCR15 bit (see Table 9) in the read configuration register sets the read configuration. At reset, asynchronous/page mode is the default configuration for all READ operations.

Asynchronous/Page Read Mode

Asynchronous/page read mode is the default read configuration state. To use the device in an asynchronous-only application, ADV# and CLK may be tied to VSS, and WAIT# should be floated. Note that ADV# may also be used in asynchronous mode to latch addresses (latched asynchronous read mode).

A random access is initiated either on the falling edge of CE#, on the falling edge of ADV#, or on a transition of the address lines (A0–A21), whichever occurs last. Access times are given by ^{t}ACE, ^{t}AADV, and ^{t}AA, respectively.

A latched asynchronous read mode is also available in which all address lines except A0–A2 are latched. In this mode, the rising edge of ADV# will latch the addresses. After the addresses are latched, this mode becomes identical to the normal mode. The latched mode is useful when noise is present on the address lines, which might cause a READ operation from unwanted locations.

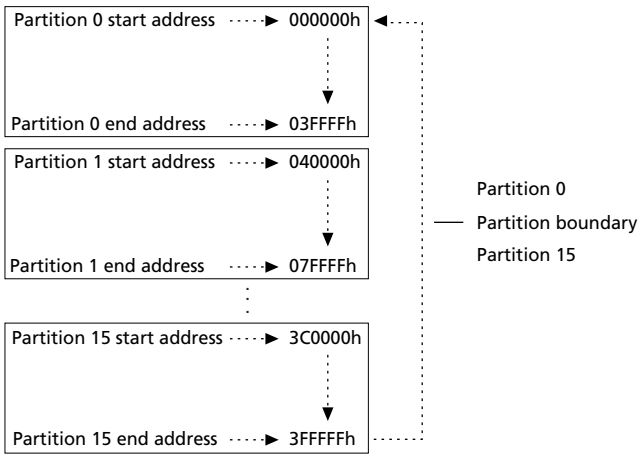
Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. The initial portion of the page mode cycle is the same as the asynchronous access cycle. Subsequent READs are performed by holding CE# LOW and toggling A0–A2, allowing random access of other words in the page. These subsequent READs are done at the faster page access time, ^{t}APA.

Burst Read Mode

The burst read mode is used to achieve a faster data rate than is possible with asynchronous read mode. A burst access is started when an active clock edge (defined by RCR6; refer to Table 9 for more information) occurs after ADV# goes LOW. The address is latched when ADV# goes HIGH or on the active clock edge, whichever occurs first. The burst read configuration is set in the read configuration register.

Burst READ operations can traverse partition boundaries, but application code is responsible for ensuring that the operations do not extend into partitions that are programming or erasing. All blocks in all partitions are burstable. For example, if a burst starts in partition 0, the application can keep clocking until the partition boundary is reached, and then read from partition 1. If the application keeps clocking beyond partition 15 last location, then the internal counter restarts from partition 0 first address (see Figure 5).

Figure 5: Partition Boundary Wrapping (Bottom Boot Example)



Clock Suspend

The clock suspend feature enables the device to suspend a burst sequence, to allow data to be retrieved from another device sharing the same bus. The system processor can resume the burst sequence where it left off at a later time, with zero initial access latency penalty. Clock suspend is most beneficial in non-cached systems.

Clock suspend can occur at any stage of a burst, during initial access latency, or when outputting data. When a burst access is suspended, internal array sensing continues, and any previously latched internal data is retained. As long as the device operation conditions are met, a burst sequence can be suspended and resumed without any limit.

Clock suspend is executed when CE# is asserted, the current address has been latched (either ADV# rising edge or CLK edge), CLK is halted, and OE# is de-asserted. CLK can be halted when it is at VIH or VIL. To resume, OE# is re-asserted and CLK is restarted. Subsequent CLK edges resume the burst sequence where it left off.

Note that when using the clock suspend feature, the device's WAIT# signal remains active. Multiple devices should not share the systems's READY signal when using the clock suspend feature. Refer to the WAIT# signal configuration on RCR8.

Read Configuration Register (RCR)

The SET READ CONFIGURATION REGISTER command is a sequence used to load the read configuration register (RCR). It is a two-cycle command sequence. Read configuration setup (60h) is written, followed by a second WRITE (03h) that specifies the value to be written to the read configuration register. The new RCR settings are placed on the address bus (A0–A15), and are latched on the rising edge of CE# or WE#, whichever occurs first. Refer to Table 9 for the RCR bit settings. After setting the RCR, the device automatically returns to read array mode. Upon reset, the RCR is set to FFCFh.

Table 9: Read Configuration Register

BIT #	DESCRIPTION	FUNCTION
15	Read Mode	0 = Synchronous Burst Access Mode 1 = Asynchronous/Page Access Mode (default)
14	Reserved	Default = 1
13–11	Latency Code	Sets the number of clock cycles before valid data out (see Figure 6): 000 = Code 0 - reserved 001 = Code 1 - reserved 010 = Code 2 011 = Code 3 100 = Code 4 101 = Code 5 110 = Code 6 - reserved 111 = Code 7 - reserved (default)
10	Wait Signal Polarity	0 = WAIT# signal is active LOW 1 = WAIT# signal is active HIGH (default)
9	Hold Data Out	Sets the data output configuration: 0 = Hold data for one clock 1 = Hold data for two clocks (default)
8	Wait Configuration	Controls the behavior of the WAIT# output signal: 0 = WAIT# asserted during delay 1 = WAIT# asserted one data cycle before delay (default)
7	Burst Sequence	Specifies the order in which data is addressed in synchronous burst mode: 0 = Reserved 1 = Linear (default)
6	Clock Configuration	Defines the clock edge on which the burst operation starts and data is referenced: 0 = Falling edge 1 = Rising edge (default)
5–4	Reserved	Default = 0
3	Burst Wrap	0 = Burst wraps within the burst length 1 = Burst no wrap (default)
2–0	Burst Length	Sets the number of words the device will output in burst mode: 001 = 4 words 010 = 8 words 011 = reserved 111 = Continuous burst (default)

WAIT# Signal Function

When performing a continuous burst, or when performing a four- or eight-word burst with no wrap selected (RCR3 = 1), the device may have an output delay when the burst sequence crosses the first eight-word boundary. The delay will occur only once during any burst access. The starting address dictates the amount of delay. If the starting address is at the end of an eight-word boundary, the output delay will be the maximum delay. If the starting address is aligned with an eight-word boundary, a delay will not be seen. Likewise, if a burst never crosses an eight-word boundary, no delay will be seen. For example, in a four-word burst, no-wrap mode, possible linear burst sequences that do not cause delays are:

0-1-2-3
1-2-3-4
2-3-4-5
3-4-5-6
4-5-6-7

The WAIT# signal informs the system if an output delay occurs. When the WAIT# signal is asserted, it indicates invalid data. When the WAIT# signal is deasserted, it indicates valid data. See Figure 26 for more details.

The WAIT# output is high impedance until the device is active (CE# = V_{IL}). In asynchronous/page mode, WAIT# is set to an asserted state (as defined by RCR10). WAIT# is also set to an asserted state during non-read-array burst operations such as burst read of status register, query, or device identifier.

During clock suspend, WAIT# remains active because CE# gates the WAIT# signal. The WAIT# signal does not revert to a high-impedance state when OE# is de-asserted and therefore can cause contention with another device attempting to control the system's ready signal during a clock suspend. Multiple devices should not be connected directly to the sysem's READY ready signal if the clock suspend feature is used.

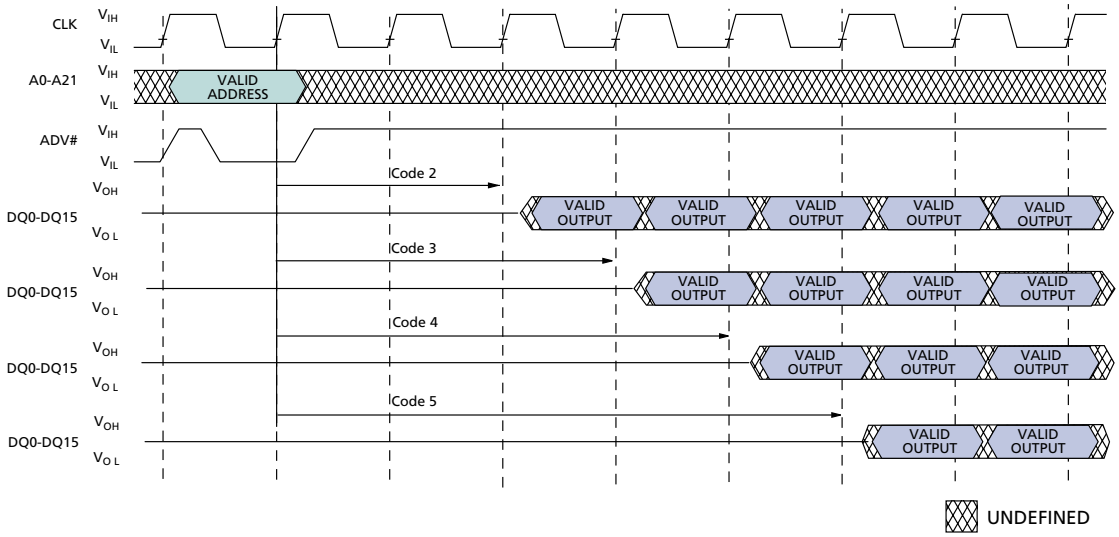
Read Mode

The device supports two read configurations: burst mode, and asynchronous/page mode. The RCR15 bit (refer to Table 9) in the read configuration register sets the read mode. Asynchronous/page mode is the default read mode.

Latency Counter

The latency counter (RCR13–RCR11) provides the number of clocks that must elapse after the clock edge that starts the burst before data is valid, as shown in Figure 6. This value depends on the input clock frequency. See Table 10 for the clock frequency vs. first access latency information.

Figure 6: Latency Counter[1]



NOTE:
1. CLK shown as rising edge configuration (RCR6 = 1).

Table 10: Clock Frequency vs. First Access Latency

LATENCY COUNTER CODE	2	3	4/5
Frequency (MHz)	≤40	≤54	≤66

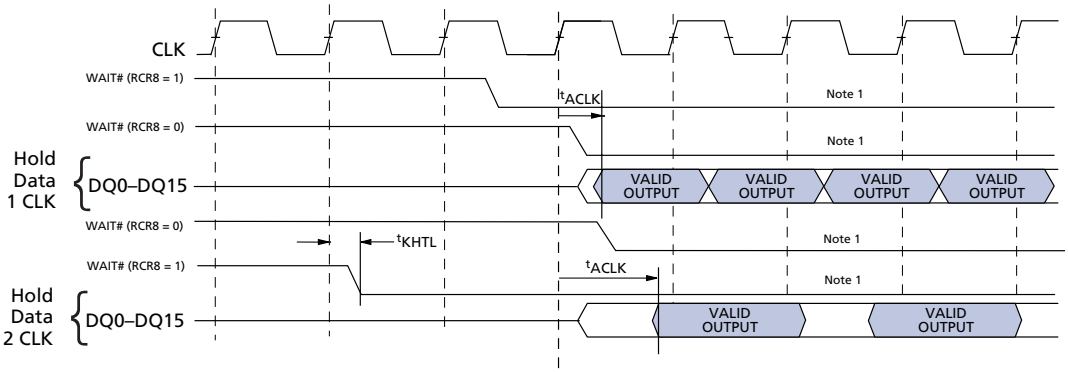
WAIT# Signal Polarity

RCR10 sets the WAIT# signal polarity. When RCR10 = 0, WAIT# is active LOW. When RCR10 = 1, the WAIT# signal is active HIGH. See "WAIT# Signal Function" on page 19 for more information.

Hold Data Out

The hold data out (RCR9) specifies for how many clocks data will be held valid. (See Figure 7.)

Figure 7: Hold Data Output Configuration



NOTE:

WAIT# shown active HIGH (RCR10 = 1).

WAIT# Configuration

The wait configuration bit (RCR8) controls the WAIT# signal behavior for all burst read modes. It should be set according to the system and CPU characteristics. The WAIT# signal can be configured to assert either during valid data, or one data cycle before data becomes valid (see Figure 6). See "WAIT# Signal Function" on page 19 for more information.

Burst Sequence

The burst sequence (RCR7) specifies the ordering of data in burst mode. Linear burst order (RCR7 = 1) is the only burst sequence supported by the device. See Table 11 for more details.

Clock Configuration

The clock configuration (RCR6) defines the clock edge on which the burst operation starts and data is defined.

Burst Wrap

The burst wrap option (RCR3) determines whether the burst access wraps within the burst length or crosses the burst length boundary. In wrap mode (RCR3 = 0) the four- or eight-word access will wrap within the four or eight words, respectively. In no-wrap mode (RCR3 = 1), the device operates similarly to a continuous burst. See Table 11 for more details.

Burst Length

The burst length (RCR2–RCR0) defines the number of words the device outputs. The device supports burst lengths of four words, eight words, or continuous burst. When the continuous burst option is selected, the internal address wraps to 000000h after reaching the maximum address.

Table 11: Sequence and Burst Length

STARTING ADDRESS (DEC)	WRAP	NO WRAP	4-WORD BURST LENGTH	8-WORD BURST LENGTH	CONTINUOUS BURST
	RCR3	RCR3	LINEAR	LINEAR	LINEAR
0	0		0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-…
1	0		1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-…
2	0		2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-…
3	0		3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-…
4	0			4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-…
5	0			5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-…
6	0			6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-…
7	0			7-0-1-2-3-4-5-6	6-7-8-9-10-11-12-13-…
…	…	…	…	…	…
14	0				14-15-16-17-18-19-20-..
15	0				15-16-17-18-19-20-21-..
…	…	…	…	…	…
0		1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-…
1		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-…
2		1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-…
3		1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-…
4		1		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-…
5		1		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11…
6		1		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12…
7		1	…	7-8-9-10-11-12-13-14	7-8-9-10-11-12-13…
…	…	…	…	…	…
14		1	…		14-15-16-17-18-19-20-…
15		1			15-16-17-18-19-20-21-…

Programming Operations

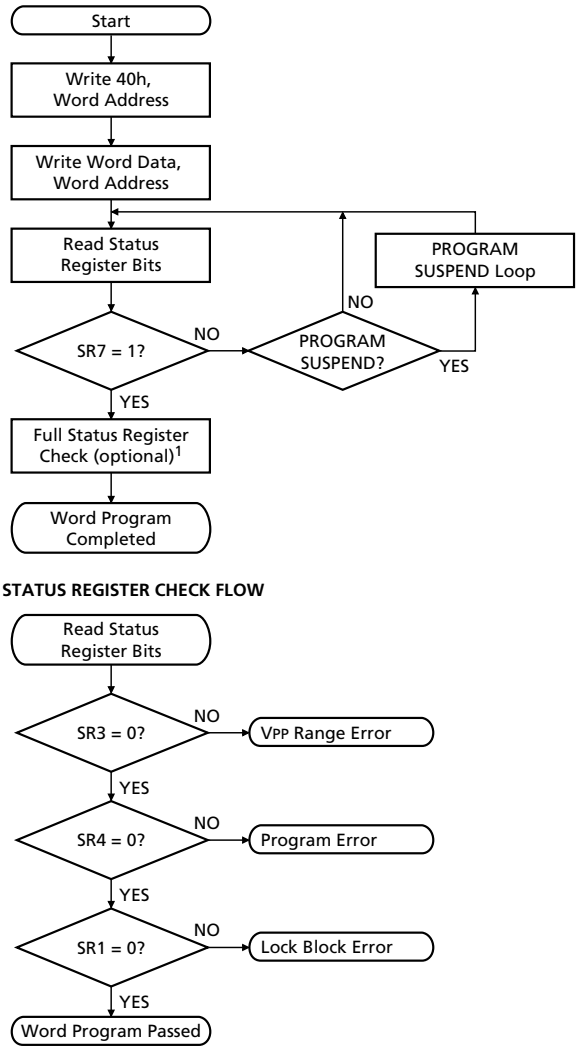
In addition to the traditional single word programming commands (10h and 40h), another sequence is offered to speed up the in-factory programming operations (30h). The in-factory programming operation is compatible with the use of an external power supply connected to the VPP ball. For in-system operations, the VPP ball can be connected either to a general purpose I/O ball of the host system, or the VCC ball.

Conventional Word Programming

After the setup command code is entered (10h/40h) on DQ0–DQ7, followed by the data to be programmed, the WSM takes over and correctly sequences the device to complete the PROGRAM operation. The PROGRAM operation may be monitored through the status register. During this time, the CSM will only respond to a PROGRAM SUSPEND, READ ARRAY, READ DEVICE IDENTIFIER, READ QUERY, and READ STATUS REGISTER command until the PROGRAM operation has been completed, after which time, all commands to the CSM become valid again.

Taking RST# to VIL during programming aborts the PROGRAM operation, leaving undetermined data in the location being programmed. When programming is aborted, a delay time of ^{t}PRD must elapse after RST# goes LOW before the internal RESET operation is complete. An additional delay of ^{t}RWH must elapse after RESET is complete (or after RST# goes HIGH, whichever occurs last) before data can be read from the device. Refer to Figure 18 and Table 17 for more information. During programming, VPP must remain above VPPLK, and VCC must remain in the voltage range provided in the recommended operating conditions.

Figure 8: Conventional WordProgramming Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE PROGRAM SETUP	Data = 40h Addr = Address of word to be programmed
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data Toggle OE# or CE# to update status register.
		Check SR7 1 = Ready, 0 = Busy

BUS OPERATION	COMMAND	COMMENTS
READ		Check SR3[2] 1 = VPP range error
		Check SR4[2] 1 = Data program error
		Check SR1 1 = Attempted PROGRAM to locked block. PROGRAM aborted.

NOTE:
1. Full status register check can be done after each word or after a sequence of words.
2. SR1, SR3, and SR4 are cleared only by the CLEAR STATUS REGISTER command, but do not prevent additional PROGRAM operation attempts.

Fast Programming Algorithm (FPA) Mode

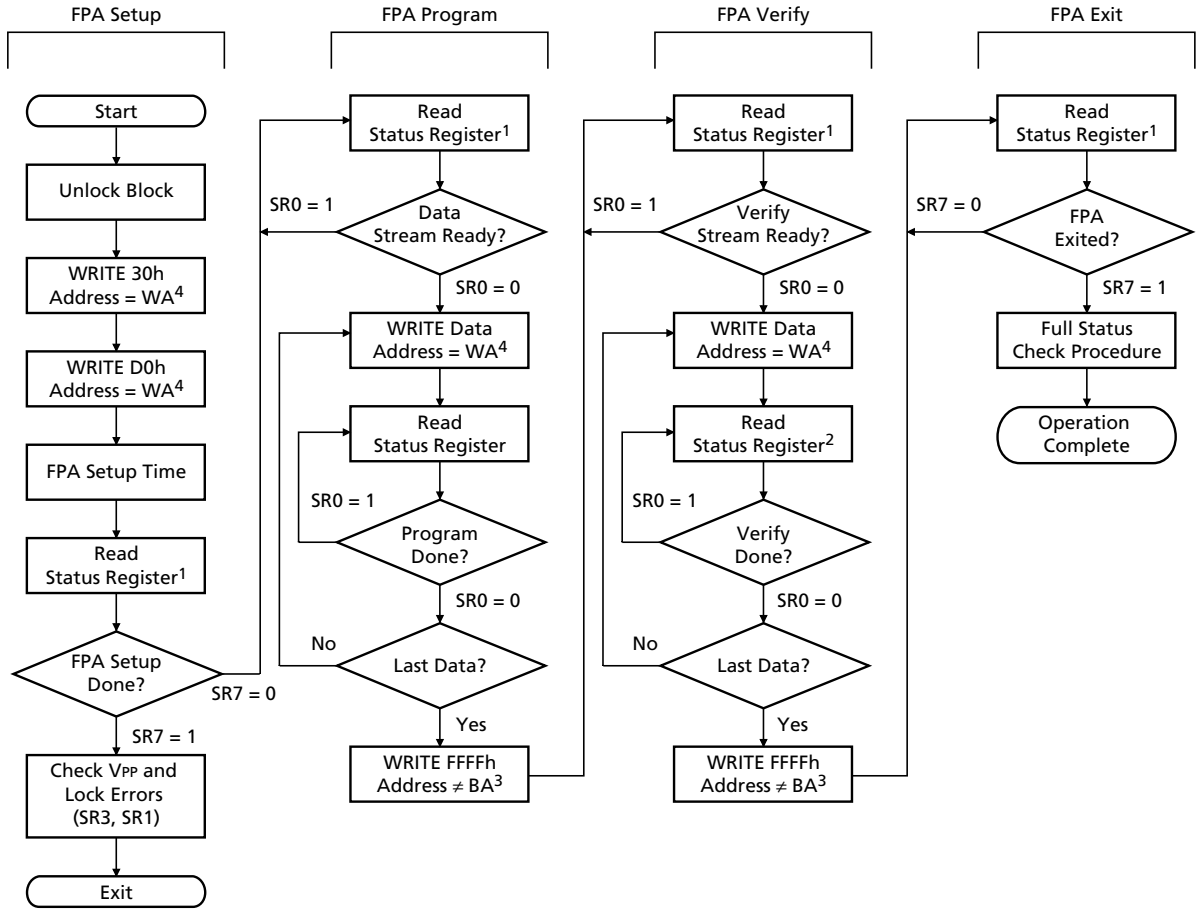
The fast programming algorithm (FPA) is intended for in-factory use. It enables fast data stream programming. For in-factory programming, FPA minimizes chip programming time when 11.4V < VPP < 12.6V. FPA algorithm can also provide accelerated program with VPP = 1.8V. Executing the FPA command (30h) followed by FPA CONFIRM (D0h), enables an entire block to be programmed. This eliminates the need to continuously update the address to be programmed.

An initial delay is required after issuing the FPA command. (See Table 25.) If the block is locked, the status register returns an error. When the FPA command is executed successfully, a data stream can be programmed beginning at the first address. The address can be held constant, or it can be incremented within the address range. The program cycle ends when the programmer writes FFFFh outside the address range of the current block.

When the FPA is activated, the data must be provided in sequential order to the WSM. Immediately after programming, verification is executed. The data sequence and starting address are provided to the WSM, which automatically performs a data verification. The result is stored in the status register. Writing FFFFh outside the memory block boundary exits the verification cycle. Figure 9 shows the FPA flowchart.

Note that issuing a 70h command to the device after FPA setup will be interpreted as data and will be written to the device.

Figure 9: Fast Programming Algorithm (FPA) Flowchart (in-factory only)



NOTE:
1. When reading the status register, the address must be within the block being programmed.
2. During FPA verify, if a word fails to verify, status changes to 90h.
3. BA = Address within block.
4. WA = First word Address to be written in the block.

ERASE Operations

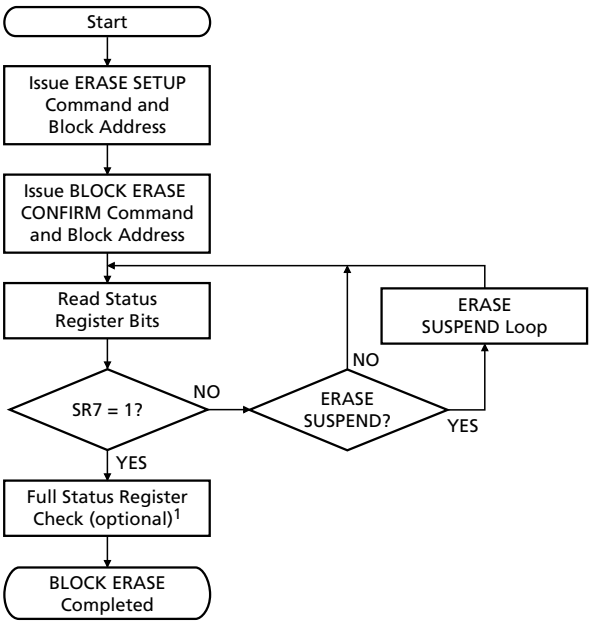
An ERASE operation must be used to initialize bits in an array block to "1s." The commands to initiate BLOCK ERASE are as follows: BLOCK ERASE SETUP (20h) followed by BLOCK ERASE CONFIRM (D0h) (see Figure 10).

A two-command erase sequence protects against accidental erasure of memory contents.

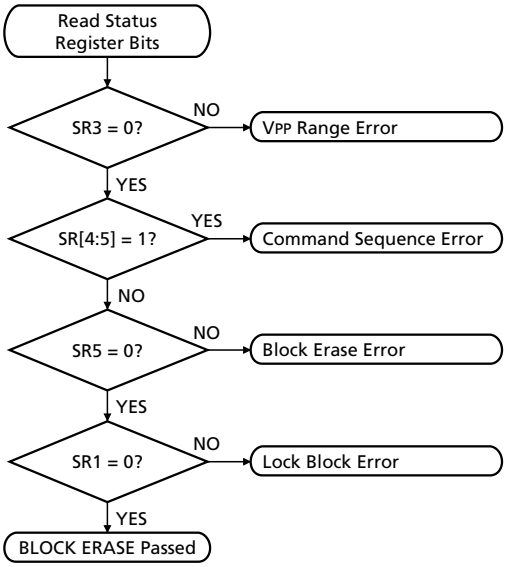
When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the BLOCK ERASE. During this sequence, the block is programmed with logic 0s, the 0s are then verified, all bits in the block are erased to logic 1 state, and finally verification is performed to ensure that all bits are correctly erased. During an ERASE, V_{PP} must remain above V_{PPLK}, and V_{CC} must remain in the voltage range provided in the recommended operating conditions. Monitoring of the ERASE operation is possible through the status register. SR7 = 1 indicates the ERASE operation is complete. SR5 = 1 indicates an ERASE failure; SR3 = 1 indicates an invalid V_{PP} supply voltage; and SR1 = 1 indicates an ERASE operation was attempted on a locked block.

Taking RST# to V_{IL} during an ERASE aborts the ERASE operation leaving undetermined data in the block being erased. When an ERASE is aborted, a delay time of ^{t}ERD must elapse after RST# goes LOW, before the internal RESET operation is complete. An additional delay of ^{t}RWH must elapse after the RESET is complete (or after RST# goes HIGH, whichever occurs last) before data can be read from the device. Refer to Figure 18 and Table 17 for more information.

Figure 10: Block Erase Flowchart



FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Block Addr = Address within block to be erased
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data Toggle OE# or CE# to update status register
		Check SR7 1 = Ready, 0 = Busy

BUS OPERATION	COMMAND	COMMENTS
READ		Check SR3[2] 1 = VPP error
		Check SR4 and SR5[2] Both = 1 = Command sequence error
		Check SR5[2] 1 = BLOCK ERASE error
		Check SR1[2] 1 = Attempted ERASE of locked block. ERASE aborted.

NOTE:
1. Full status register check can be done after each block or after a sequence of blocks.
2. SR1, SR3, SR4, and SR5 are cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked. (These bits do not prevent additional ERASE operation attempts.)

PROGRAM SUSPEND, PROGRAM RESUME, ERASE SUSPEND, ERASE RESUME Commands

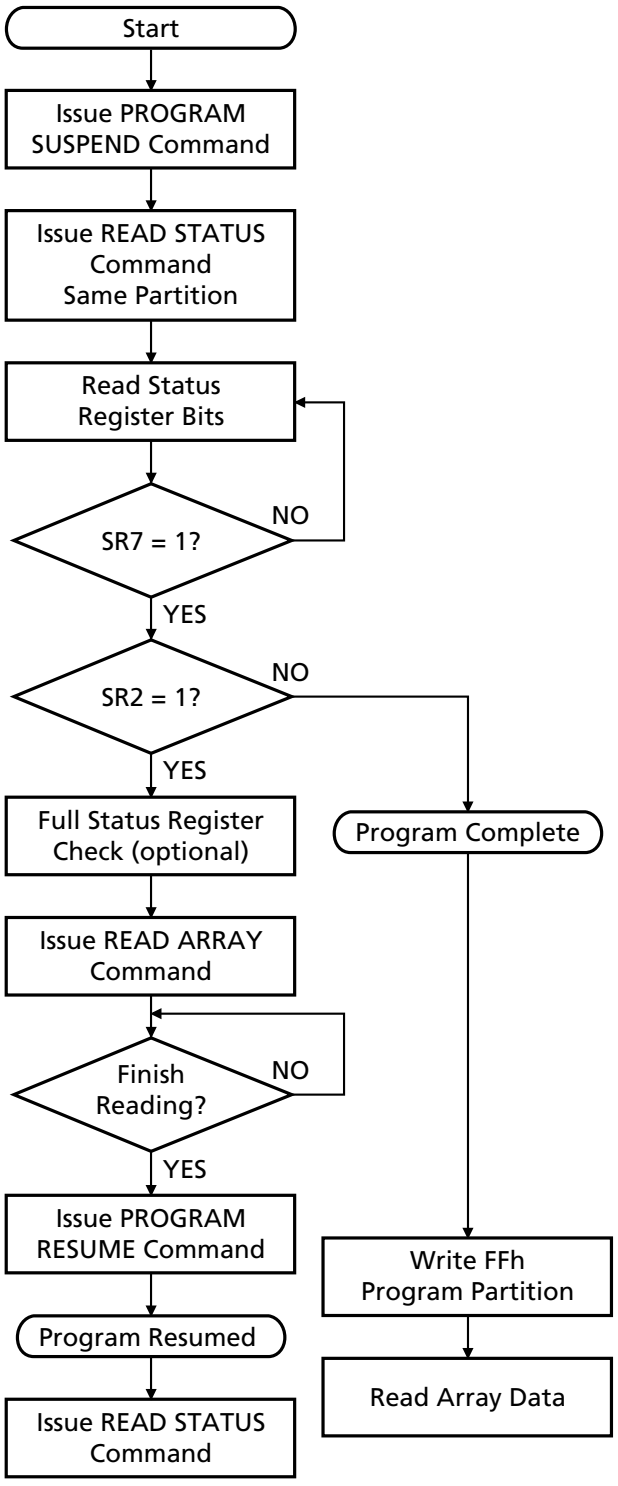
During the execution of an ERASE/PROGRAM operation, the SUSPEND command (B0h) can be issued to direct the WSM to suspend the ERASE/PROGRAM operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, READ QUERY, READ DEVICE IDENTIFIER, and PROGRAM RESUME. Additionally, PROGRAM, PROGRAM SUSPEND, ERASE RESUME, LOCK BLOCK, UNLOCK BLOCK, and LOCK DOWN BLOCK are valid commands during an ERASE SUSPEND. (See Block Locking section).

Once in erase suspend mode, array data must be read/programmed into a block other than the one being erased. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the ERASE/PROGRAM operation, a RESUME command (D0h) needs to be issued to cause the CSM to clear the suspend state previously set (see Figure 12). The RESUME command (D0h) needs to be issued when the device is in the ready state, SR7 = 1. If the RESUME command is issued when the device is busy, SR7 = 0, the WSM will ignore the RESUME command.

It is also possible that an ERASE in any block can be suspended and a PROGRAM to another block within any partition can be initiated. At this point, a PROGRAM SUSPEND may be issued to allow a READ of yet another location. After the completion of a READ operation, PROGRAM can be resumed by issuing a PROGRAM RESUME command. Finally, after the device has reached the ready state, SR7 = 1, an ERASE RESUME will allow the WSM to finish the original ERASE operation.

A minimum time should elapse between an ERASE RESUME command and a subsequent ERASE SUSPEND command to ensure that the device achieves sufficient cumulative erase time.

Figure 11: Program Suspend/Program Resume Flowchart



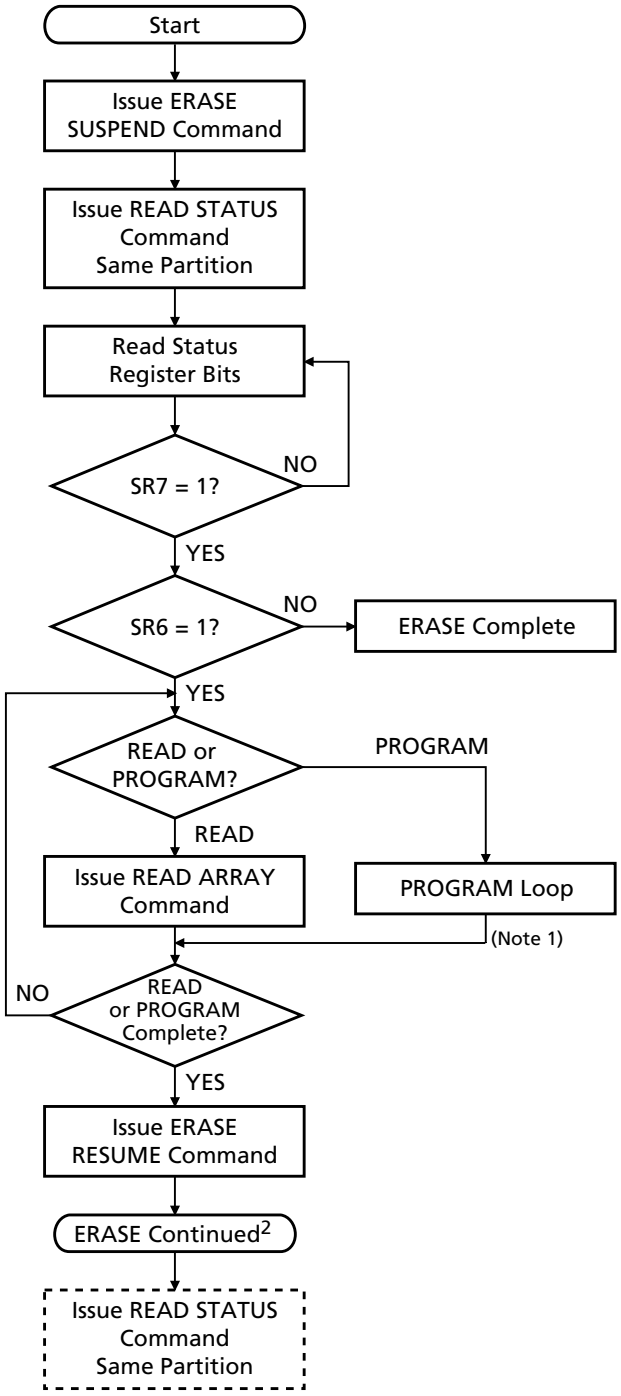
BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
WRITE	READ STATUS	Data = 70h
READ		Status register data Toggle OE# or CE# to update status register
		Check SR7 1 = Ready
		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed
WRITE	PROGRAM/ RESUME	Data = D0h

NOTE:

If the suspended partition was placed in read array mode, then the following condition applies:

BUS OPERATION	COMMAND	COMMENTS
WRITE	READ STATUS	Return partition to status mode: Data = 70h Addr = address within same partition

Figure 12: Erase Suspend/Erase Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h
WRITE	READ STATUS	Data = 70h Addr = Any address in same partition
		Check SR7 1 = Ready, 0 = Busy
		Check SR6 1 = Suspended 0 = Completed
WRITE	READ ARRAY	Data = FFh Addr = Any device address (except block being erased)
READ or WRITE		Read data from, or write data to, a block other than that being erased
WRITE	ERASE RESUME	Data = D0h Addr = Any address

NOTE:

If the suspended partition was placed in read array mode or a program loop, then the following condition applies:

BUS OPERATION	COMMAND	COMMENTS
WRITE	READ STATUS	Return partition to status mode Data = 70h Addr = Address within same partition

NOTE:

1. See Word Programming flowchart for complete programming procedure.
2. See BLOCK ERASE flowchart for complete erase procedure.

READ-While-PROGRAM/ERASE Concurrency

It is possible for the device to read from one partition while erasing/programming to another partition. For example, during a READ CONCURRENCY operation, if a PROGRAM or ERASE operation is being performed in partition *x*, then partition *x* changes to the read status mode and an array READ operation can be performed on any other partition. Partition *x* will remain in read status mode.

The CFI and the device identifier areas are considered an additional partition separate from the array partitions and support concurrent operations. (See Table 12 for simultaneous operations allowed between the protection register and the main partitions.)

Table 12: Simultaneous Operations Allowed in the Protection Register

PROTECTION REGISTER	MAIN PARTITION	DESCRIPTION
READ	PROGRAM/ERASE	During the programming or erasing of a main partition, the protection register may be read from any other partition.
PROGRAM	READ	During the programming of the protection register, READs are only allowed in the main partitions. A delay of 200ns must be inserted after issuing the PROTECTION PROGRAM command (C0h) before performing concurrent read of the main partitions.

Block Locking

The Flash device provides a flexible locking scheme that allows each block to be individually locked or unlocked with no latency.

The device offers two-level protection for the blocks. The first level allows software-only control of block locking (for data that needs to be changed frequently), while the second level requires hardware interaction before locking can be changed (code that does not require frequent updates).

Control signals WP#, DQ1, and DQ0 define the state of a block; for example, state [001] means WP# = 0, DQ1 = 0, and DQ0 = 1. See "Reading a Block's Lock Status" on page 34.

Table 13 defines all of the possible locking states, Figure 13 shows the block locking state diagram, and Figure 14 describes the locking operations.

Table 13: Block Locking State Transition

WP#	DQ1	DQ0	NAME	ERASE/PROG ALLOWED	LOCK	UNLOCK	LOCK DOWN
0	0	0	Unlocked	Yes	To [001]	No Change	To [011]
0	0	1	Locked (Default)	No	No Change	To [000]	To [011]
0	1	1	Lock Down	No	No Change	No Change	No Change
1	0	0	Unlocked	Yes	To [101]	No Change	To [111]
1	0	1	Locked	No	No Change	To [100]	To [111]
1	1	0	Lock Down Disabled	Yes	To [111]	No Change	To [111]
1	1	1	Lock Down Disabled	No	No Change	To [110]	No Change

Figure 13: Block Locking State Diagram

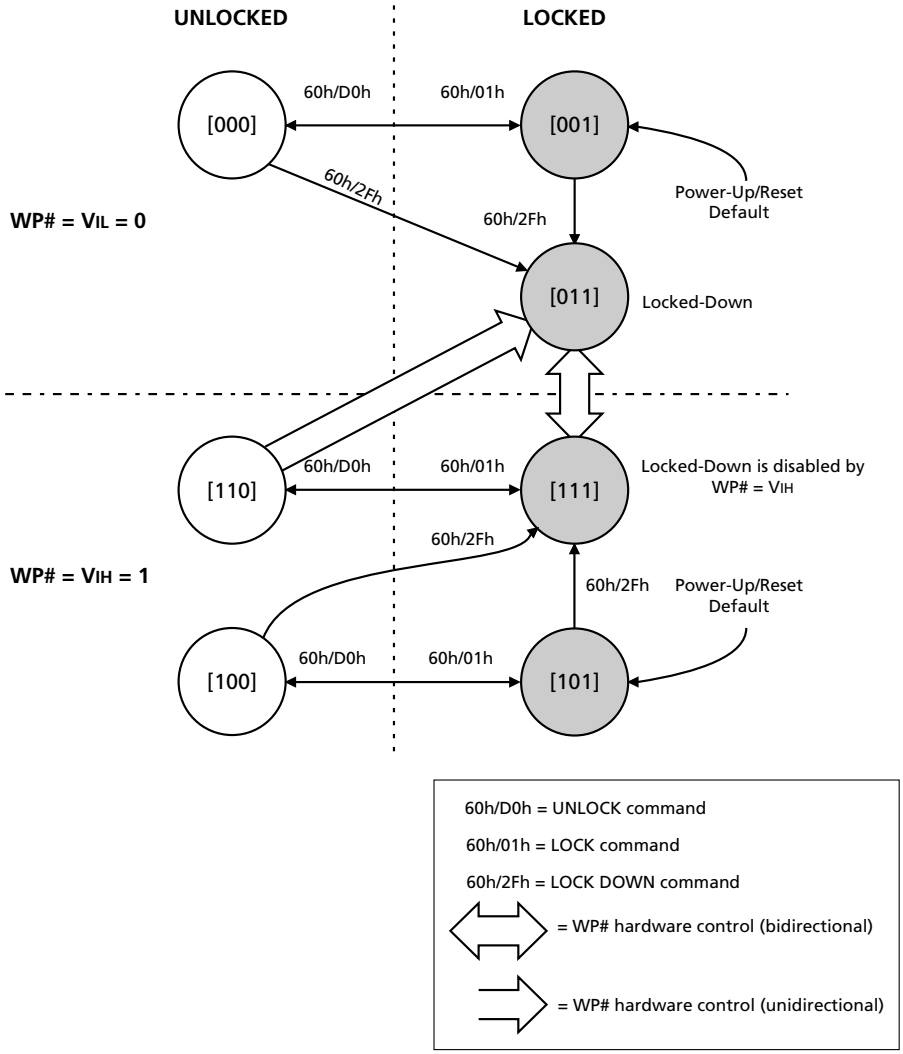
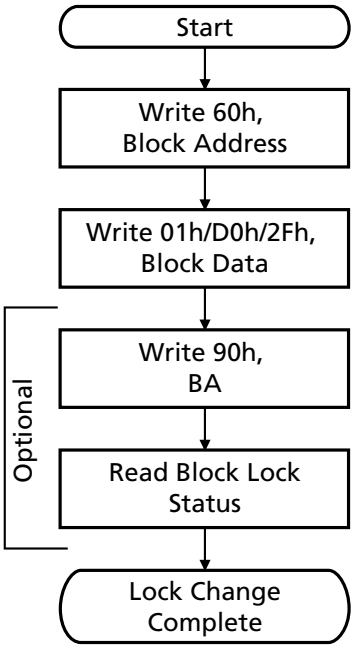


Figure 14: Locking Operations Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	LOCK SETUP	Data = 60h Addr = BLOCK to LOCK/UNLOCK/ LOCK DOWN (BA)
WRITE	LOCK, UNLOCK, or LOCK DOWN CONFIRM	Data = 01h (LOCK BLOCK) D0h (UNLOCK BLOCK) 2Fh (LOCK DOWN BLOCK) Addr = BLOCK to LOCK/UNLOCK/ LOCK DOWN (BA)
WRITE (Optional)	READ ID	Data = 90h Addr = BA
READ (Optional)	BLOCK LOCK STATUS	Data = Block Lock Status Data Addr = BBA + 02h
		Confirm locking change on DQ[1:0]. See Table 13 for valid combinations.

Locked State

After a reset sequence, all blocks are locked (states [001] or [101]). This means full protection from alteration. Any PROGRAM or ERASE operations attempted on a locked block will return an error on bit SR1 of the status register. The status of a locked block can be changed to unlocked or lock down using the appropriate software commands. Writing the LOCK SETUP command sequence (60h) followed by UNLOCK BLOCK (D0h) can unlock a locked block.

Unlocked State

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered down. An unlocked block can be locked or locked down by writing the LOCK SETUP command (60h) followed by LOCK BLOCK (01h), or LOCK DOWN BLOCK (2Fh).

Locked Down State

The lock down function is dependent on the WP# input. When WP# = 0, blocks in lock down [011] are protected from PROGRAM, ERASE, and lock status changes. When WP# reverts to WP# = 1, the lock down function is disabled [111], and locked down blocks can be individually unlocked by a software command to the [110] state, where they can be erased and programmed. These blocks can then be relocked [111] and unlocked [110] as desired while WP# remains HIGH. When WP# goes LOW, blocks that were previously locked down return to the locked down state [011] regardless of any changes made while WP# was HIGH. A locked or unlocked block can be locked down by writing the LOCK SETUP command (60h) followed by LOCK DOWN (2Fh). Resetting the device resets all blocks, including those in lock down, to the locked state (see Table 13).

Reading a Block's Lock Status

The lock status of every block can be read in the read device identifier mode. To enter this mode, write 90h to the device. Subsequent READs at the base block address +00002 will output the lock status of that block. The lowest two outputs, DQ0 and DQ1, represent the lock status. DQ0 indicates the block lock/unlock status and is set by the LOCK command and cleared by the UNLOCK command. It is also automatically set when entering lock down. DQ1 indicates lock down status and is set by the LOCK DOWN command. It can only be cleared by reset or power-down, not by software. Table 13 on page 31 shows the locking state transition scheme and Table 14 shows the write protection truth table.

Table 14: Write Protection Truth Table

VPP	WP#	RST#	WRITE PROTECTION
X	X	VIL	Device inaccessible
VIL	X	VIH	Word program and block erase prohibited
X	VIL	VIH	All lock down blocks locked
X	VIH	VIH	All lock down blocks can be unlocked

Locking Operations During Erase Suspend

Changes to a block's lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock, or lock down. This is useful in the case when another block needs to be updated while an ERASE operation is in progress.

To change a block's lock status during an ERASE operation, first write the ERASE SUSPEND command (B0h), then check the status register until it indicates that the ERASE operation has been suspended. Next, write the desired LOCKING command sequence to the desired block, and the block's lock status will be changed. After completing any desired LOCK, READ, or PROGRAM operations, resume the ERASE operation with the ERASE RESUME command (D0h).

If an erase suspended block has its lock status changed, the lock status bits will change immediately. When the ERASE is resumed, the ERASE operation will complete. A LOCKING operation cannot be performed during a PROGRAM SUSPEND.

Using nested locking or program command sequences during erase suspend can introduce ambiguity into status register results. Following protection configuration setup (60h), an invalid command will produce a command sequence error (SR4 and SR5 will be set to "1") in the status register. If a command sequence error occurs during an erase suspend, SR4 and SR5 will be set to "1" and will remain at "1" after the erase suspend is resumed. When the ERASE is complete, any possible error during the ERASE cannot be detected via the status register because of the previous command sequence error. This is also true if an error occurs during a PROGRAM operation error nested within an erase suspend.

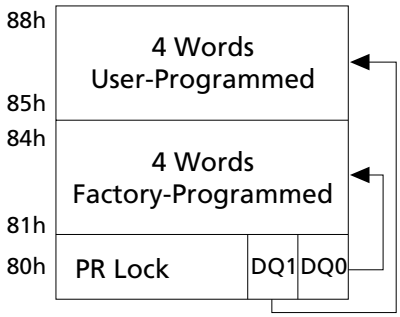
Protection Register

The 128-bit security area is divided into two 64-bit segments. The first 64 bits of the protection register (addresses 81h–84h) are programmed at the factory with a unique 64-bit unchangeable number. DQ0 of the PR lock register (address 80h) is programmed to a "0" state, locking the first 64 bits and preventing any further programming.

The second 64 bits (addresses 85h–88h) are left erased for the user to program as desired (see Figure 15). The user can program any information into this area as long as DQ1 of the PR lock register (address 80h) remains unprogrammed. After DQ1 of the PR lock register is programmed, no further programming is allowed in the user area. ERASE operations are not allowed on the protection register.

READ-While-WRITE operation is only allowed between the chip protection register and main partitions. Table 12 describes the simultaneous operations allowed in the chip protection register.

Figure 15: Protection Register Memory Map



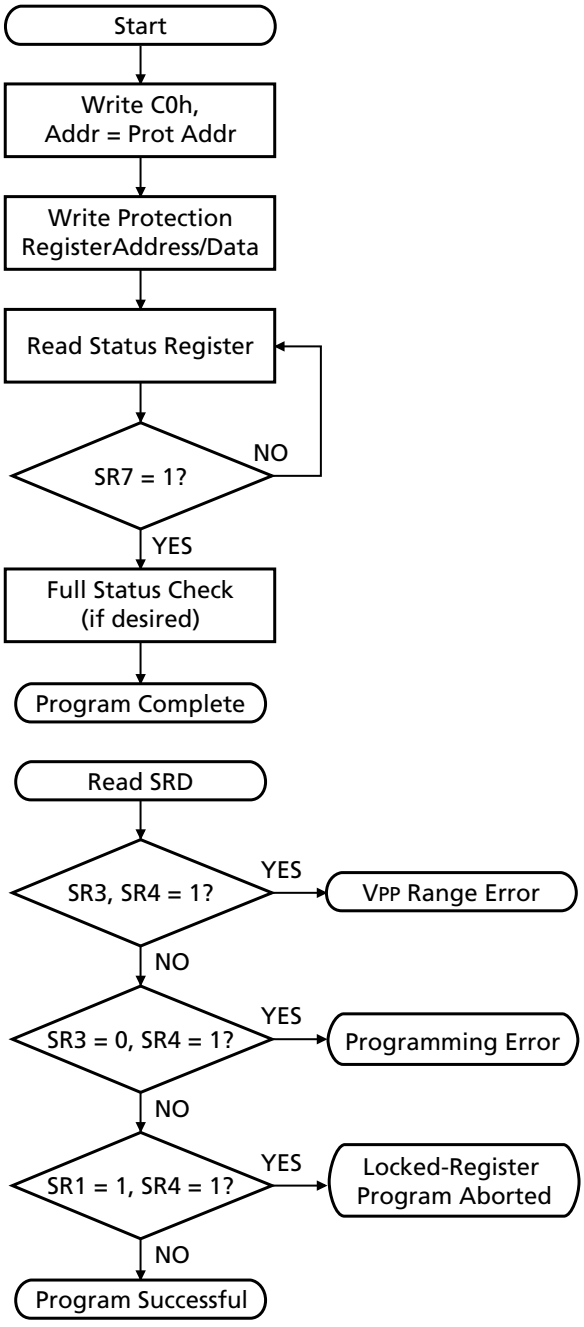
Reading the Protection Register

The protection register is read in the device identifier mode. To enter this mode, load the 90h command. Once in this mode, READ cycles from addresses shown in Table 15 on page 37 retrieve the specified information. To return to the read array mode, write the READ ARRAY command (FFh).

Programming the Protection Register

The user area of the protection register (addresses 85h–88h) may be programmed by writing the PROTECTION PROGRAM command (C0h), followed by the data to be programmed at one of the addresses within the user area. This procedure may be repeated for each of the addresses in the user area, as long as DQ1 of the PR lock register remains unprogrammed. Issuing a PROTECTION PROGRAM command outside the register's address space results in a status register error (SR4 = 1). See Figure 16 on page 36 for more information.

Figure 16: Protection Register Programming Procedure



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROTECTION PROGRAM SETUP	Data = C0h Addr = Protection address
WRITE		Data = Data to program Addr = Protection address
READ		Read SRD Toggle CE# or OE# to update SRD
		Check SR7 1 = WSM Ready 0 = WSM Busy
Protection program operations addresses must be within the protection register address space. Addresses outside this space will return an error. Repeat for subsequent programming operations. Full status register check can be done after each PROGRAM or after a sequence of PROGRAM operations.		

BUS OPERATION	COMMENTS			
READ	SR1	SR3	SR4	
	0	1	1	VPP error
	0	0	1	Protection register program error
	1	0	1	Register locked; operation aborted
Only the CLEAR STATUS REGISTER command clears SR1, SR3, and SR4. If an error is detected, clear the status register before attempting a program retry or other error recovery.				

Locking the Protection Register

DQ0 of the PR lock register is programmed to "0" by the factory to protect the unique device number. DQ1 of the PR lock register can be programmed by the user to lock the user portion (upper 64 bits) of the chip protection register (refer to Figure 15). This bit is set using the PROTECTION PROGRAM command, C0h, to program FFFDh into the PR lock register (address 80h).

After DQ1 of the PR lock register is programmed, the user's protection register cannot be changed. The PR lock register will read FFFCh. PROTECTION PROGRAM commands written to a locked section result in a status register error (SR1 = 1, SR4 = 1).

Table 15: Device Identifier Codes

ITEM	ADDRESS[1]		DATA	DESCRIPTION
	BASE	OFFSET		
Manufacturer's ID (ManID)[2]	Block	00h	002Ch 0089h	Micron ManID Intel ManID
Device ID Code (DevID)[3]	Block	01h	44C6h 44C7h	64Mb top boot device (Micron) 64Mb bottom boot device (Micron)
			8864h 8865h	64Mb top boot device (Intel) 64Mb bottom boot device (Intel)
Block lock status	Block	02h	DQ0 = 0	Block is unlocked
			DQ0 = 1	Block is locked
Block lock down status	Block	02h	DQ1 = 0	Block is not locked down
			DQ1 = 1	Block is locked down
Read configuration register	Block	05h	Register data	
Protection register lock status	Block	80h	Lock data	
Protection register	Block	81h–84h	Factory data	
		85h–88h	User data	

NOTE:
1. Address = base + offset.
2. Different ManID devices are ordered via separate part numbers. See Figure 4 on page 9 for details.
3. Different Device ID codes are dependent on the Manufacturer's ID ordered. See Figure 4 on page 9 for details.

VPP/VCC Program and Erase Voltages

The Flash device provides in-system programming and erase with VPP in the 0.9V–1.95V range (VPP). The 12V VPP mode programming is offered for compatibility with existing programming equipment.

The device can withstand 100,000 PROGRAM/ERASE operations with VPP = VPP1, or 1,000 PROGRAM/ERASE operations with VPP = VPP2.

In addition to the flexible block locking, the VPP programming voltage can be held LOW for absolute hardware write protection of all blocks in the Flash device. When VPP is below VPPLK, any PROGRAM or ERASE operation will result in an error, prompting the corresponding status register bit (SR3) to be set.

During PROGRAM and ERASE operations, the WSM monitors the VPP voltage level. PROGRAM/ERASE operations are allowed only when VPP is within the ranges specified in Table 16.

When VCC is below VLKO, any PROGRAM/ERASE operation will be disabled.

Table 16: VPP Range (V)

SYMBOL	MIN	MAX
VPP1	0.9	1.95
VPP2	11.4	12.6

Device Reset

To reset the device, the RST# signal must be asserted (RST# = VIL) for a minimum of tRP. After reset, the device defaults to read array mode, the status register is set to 80h, and the read configuration register defaults to asynchronous/page read mode. A delayed access time of tRWH from the rising edge of RST# must elapse before data can be read from the device. The circuitry used to generate the RST# signal needs to be common with the system reset. Refer to the timing diagram for further details.

If RST# is asserted during a PROGRAM or ERASE operation, the operation will be aborted and the memory contents at the aborted block or address are invalid.

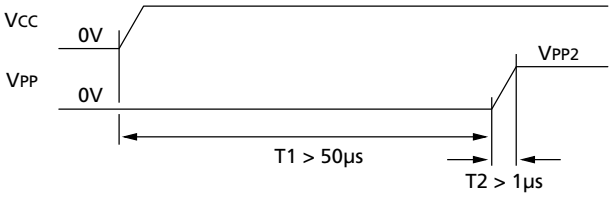
Power-Up Sequence

The device is protected against accidental block erasure or programming during power transitions. If VCC, VCCQ, and VPP are connected together, it does not matter whether VPP or VCC powers up first.

If VCCQ and/or VPP are not connected to the system supply, then VCC should attain VCC (MIN) before applying VCCQ and VPP. Device inputs should not be driven before supply voltage = VCC (MIN). Power supply transitions should only occur when RST# is LOW.

When VPP is applied within the in-factory programming range (VPP2), the sequence shown in Figure 17 must be followed. Applying VPP within the in-system programming range (VPP1) does not require this sequence.

Figure 17: VCC and VPP at Power Up



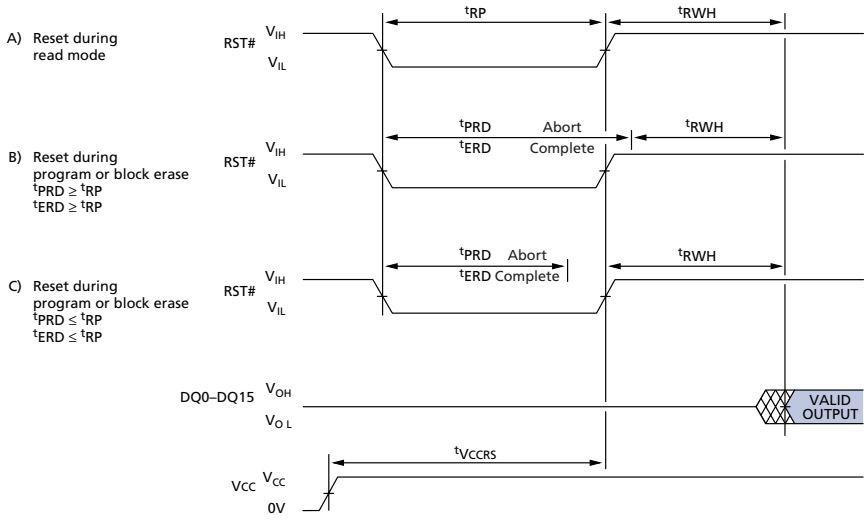
Standby Mode

ICC supply current is reduced by applying a logic HIGH level on CE# to enter the standby mode. In the standby mode, the outputs are at a high impedance state independent of OE#. Applying a logic HIGH level on CE# reduces the current to ICCS. If the device is deselected during an ERASE operation or during programming, the device continues to draw current until the operation is complete.

Automatic Power Save (APS) Mode

Substantial power savings are realized during periods when the array is not being read and the device is in active mode. During this time, the device switches to the automatic power save (APS) mode. When the device switches to APS mode, ICC is reduced to a level comparable to ICCS. Further power savings can be realized by applying a logic HIGH level on CE# to place the device in standby mode. The low level of power is maintained until another operation is initiated. In this mode, the I/Os retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control signals toggle.

Figure 18: Reset Operations



NOTE:

Address signals and control signals CE#, ADV#, WE#, and OE# not shown. Refer to the appropriate READ timing diagrams for correct operation of these signals.

Table 17: Reset Parameter Definitions

PARAMETER	SYMBOL	MIN	MAX	UNIT
RST# pulse width	^{t}RP	100		ns
RST# HIGH to output delay	^{t}RWH		150	ns
RST# LOW during PROGRAM to RESET operation complete	^{t}PRD		10	µs
RST# LOW during BLOCK ERASE to RESET operation complete	^{t}ERD		20	µs
VCC setup to RST# going HIGH	$^{t}VCCRS$	60		µs

Electrical Specifications

Table 18: Absolute Maximum Ratings[1]

PARAMETERS/CONDITIONS	MIN		MAX	UNITS	NOTES
Voltage to any ball except VCC, VCCQ, and VPP	(W18)	-0.5	+2.45	V	
	(W30)	-0.5	+3.45	V	
VPP Voltage		-0.2	+14	V	2
VCC Supply Voltage	(W18)	-0.2	+2.45	V	
	(W30)	-0.2	+2.45		
VCCQ Supply Voltage	(W18)	-0.2	+2.45	V	
	(W30)	-0.2	+3.465		
Output Short Circuit Current			100	mA	
Operating Temperature Range		-40	+85	°C	
Storage Temperature Range		-65	+125	°C	
Soldering Cycle			260°C for 10s		

NOTE:

1. Stresses greater than those listed in Table 18 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum DC voltage on VPP may overshoot to +14V for periods < 20ns.

Table 19: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Temperature	T_A	-40	–	+85	°C
VCC Supply Voltage	VCC	1.65	–	1.95	V
I/o Supply Voltage	VCCQ (W18)	1.65	–	2.24V	V
	VCCQ (W30)			3.3V	
Input/output Capacitance: DQs	CIO	–	4.0	6.5	pF
VPP Voltage	VPP1	0.9	–	1.95	V
VPP In-factory Programming Voltage	VPP2	11.4	–	12.6	V
Block Erase Cycling (VPP = VPP1)		–	–	100,000	Cycles
Block Erase Cycling (VPP = VPP2)		–	–	1,000	Cycles
Time For VPP at VPP2	t_{PPH}			100	Hours

Table 20: Capacitance

T_A = +25°C; f = 1 MHz

PARAMETER/CONDITION	SYMBOL	W18		W30		UNITS
		TYP	MAX	TYP	MAX	
Input Capacitance	CIN	5	8	5	8	pF
Output Capacitance	COUT	8	10	6	9	pF
Clock Capactitance	CCLK	10	12	10	12	pF

Table 21: DC Characteristics

All currents are in RMS unless otherwise noted

PARAMETER	SYM	MIN	W18		W30		UNITS	NOTES
			TYP	MAX	TYP	MAX		
Input Low Voltage	V_{IL}	0		0.4		0.4	V	1
Input High Voltage	V_{IH}	V_{CCQ} – 0.4		V_{CCQ}		V_{CCQ}	V	1
Output Low Voltage I_{OL} = 100µA	V_{OL}			0.1		0.1	V	
Output High Voltage I_{OH} = -100µA	V_{OH}	V_{CCQ} – 0.1					V	
V_{PP} Lockout Voltage	V_{PPLK}	0.4					V	
V_{CC} Lock	V_{LKO}	1.0					V	
V_{CCQ} Lock	V_{ILKOQ}	0.9					V	
Input Load Current	I_{LI}			±1		±1	µA	
Output Leakage Current	I_{LO}			±1		±1	µA	
V_{CC} Standby Current	I_{CCS}		7	25	7	25	µA	
Asynchronous Read Current	I_{CCR}		2	4	2	4	mA	2, 3
Page Read Current	I_{CCR}		3	6	3	6		
V_{CC} Burst Read Current 4-word Burst Read Current @ 40 MHz 4-word Burst Read Current @ 54 MHz 4-word Burst Read Current @ 66 MHz	I_{CCR}		 2 3 3	 4 5 5	 2 3 3	 4 5 5	mA	2, 3
V_{CC} Burst Read Current 8-word Burst Read Current @ 40 MHz 8-word Burst Read Current @ 54 MHz 8-word Burst Read Current @ 66 MHz	I_{CCR}		 2 3 3	 4 5 5	 2 3 3	 4 5 5	mA	2, 3
V_{CC} Continuous Burst Read Current Continous Burst Read Current @ 40 MHz Continous Burst Read Current @ 54 MHz Continous Burst Read Current @ 66 MHz	I_{CCR}		 5 7 8	 8 10 12	 5 7 8	 8 10 12	mA	2, 3
V_{CC} Program Current V_{PP} = V_{PP}1, Program in Progress V_{PP} = V_{PP}2, Program in Progress	I_{CCW}		 18 8	 25 15	 18 8	 25 15	mA	
V_{CC} Block Erase Current V_{PP} = V_{PP}1, Block Erase in Progress V_{PP} = V_{PP}2, Block Erase in Progress	I_{CCE}		 18 8	 30 15	 18 8	 30 15	mA	
V_{CC} Program Suspend Current	I_{CCWS}		7	25	7	25	µA	4
V_{CC} Erase Suspend Current	I_{CCES}		7	25	7	25	µA	4
V_{CC} Automatic Power Save Current	I_{CCAPS}		7	25	7	25	µA	
V_{PP} Standby Current V_{PP} Program Suspend Current	I_{PPS} I_{PPWS}		0.2 0.2	5 5	0.2 0.2	5 5	µA	

Table 21: DC Characteristics

All currents are in RMS unless otherwise noted

PARAMETER	SYM	MIN	W18		W30		UNITS	NOTES
			TYP	MAX	TYP	MAX		
V_{PP} Erase Suspend Current V_{PP} Read Current	I_{PPES} I_{PPR}		0.2 2	5 15	0.2 2	5 15	µA	
V_{PP} Program Current V_{PP} = V_{PP}1, Program in Progress V_{PP} = V_{PP}2, Program in Progress	I_{PPW}		 0.05 8	 0.10 22	 0.05 8	 0.10 22	mA	
V_{PP} Erase Current V_{PP} = V_{PP}1, Erase in Progress V_{PP} Erase Current V_{PP} = V_{PP}2, Erase in Progress	I_{PPE}		0.05 8	0.10 22	0.05 8	0.10 22	mA	

NOTE:

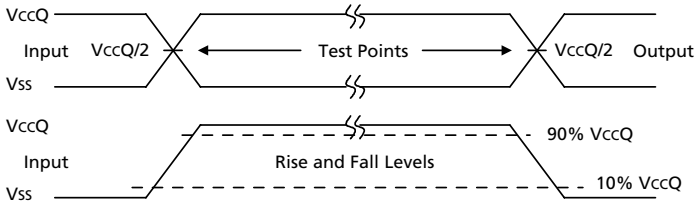
1. V_{IL} may decrease to -0.4V and V_{IH} may increase to $V_{CC}Q$ + 0.3V for durations not to exceed 20ns.
2. APS mode reduces I_{CC} to approximately I_{CCS} levels.
3. Test conditions: V_{CC} = V_{CC} (MAX), CE# = V_{IL}, OE# = V_{IH}. All other inputs = V_{IH} or V_{IL}.
4. I_{CCES} and I_{CCWS} values are valid when the device is deselected. Any READ operation performed while in suspend mode will have an additional current draw of suspend current (I_{CCES} or I_{CCWS}).

Table 22: Asynchronous READ Cycle Timing Requirements

See Figure 19 and Figure 20 for timing requirements and load configuration.

PARAMETER	SYM	-60		-70		-80		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ cycle time	^{t}RC	60		70		80		ns
Address to output delay	^{t}AA		60		70		80	ns
CE# LOW to output delay	^{t}ACE		60		70		80	ns
OE# LOW to output delay	^{t}AOE		20		30		30	ns
RST# HIGH to output delay	^{t}RWH		150		150		150	ns
CE# LOW to output in Low-Z	^{t}CEZ	0		0		0		ns
OE# LOW to output in Low-Z	^{t}OEZ	0		0		0		ns
CE# or OE# HIGH to output High-Z	^{t}OD		5		20		20	ns
Output hold from address, CE# or OE# transition	^{t}OH	0		0		0		ns
Address setup to ADV# HIGH	^{t}AVS	7		7		10		ns
CE# LOW to ADV# HIGH	^{t}CVS	7		7		10		ns
ADV# LOW to output delay	$^{t}AADV$		60		70		80	ns
ADV# pulse width LOW	^{t}VP	7		7		10		ns
ADV# pulse width HIGH	^{t}VPH	7		7		10		ns
Address hold from ADV# HIGH	^{t}AVH	7		7		9		ns
Page address access	^{t}APA		17		22		22	ns

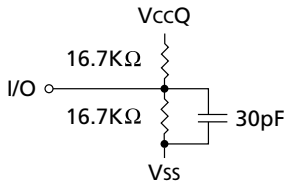
Figure 19: AC Input/Output Reference Waveforms



NOTE:

AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input timing begins at VccQ/2, and output timing ends at VccQ/2. Input rise and fall times (10% to 90%) < 5ns.

Figure 20: Output Load Circuit[1]



NOTE:

1. Minimum recommended capacitive loading is 5pF.

Table 23: Burst READ Cycle Timing Requirements

PARAMETER	SYM	-606		-705		-804		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
CLK period	^{t}CLK	15		18.5		25		ns
CLK frequency	^{f}CLK		66		54		40	MHz
CLK HIGH (LOW) time	^{t}KP	3		6		9.5		ns
CLK fall (rise) time	$^{t}KHKL$		2		3		3	ns
Address valid setup to CLK	^{t}AKS	7		7		9		ns
ADV# LOW setup to CLK	^{t}VKS	7		7		10		ns
CE# LOW setup to CLK	^{t}CKS	7		7		9		ns
CLK to output valid (latency codes 3, 4, and 5)	$^{t}ACLK$		11		14		20	ns
CLK to output valid (latency code 2)	$^{t}ACLK$		20		20		20	ns
Output hold from CLK	^{t}KOH	3		3		3		ns
Address hold from CLK	^{t}AKH	7		7		10		ns
CLK to WAIT# valid	$^{t}KHTL$		11		14		20	ns
CE# LOW to WAIT# valid	$^{t}CEWV$		11		14		20	ns
CE# HIGH to WAIT# High-Z	$^{t}CEWZ$		11		14		20	ns
CE# HIGH between subsequent burst READs	$^{t}CBPH$	14		18		18		ns

Table 24: WRITE Cycle Timing Requirements

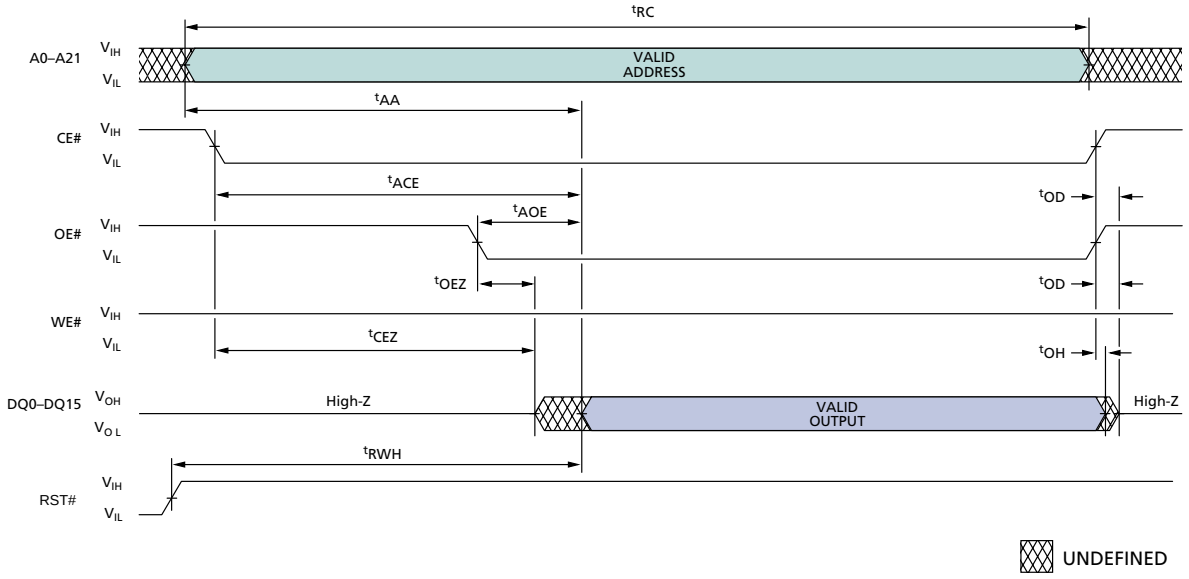
PARAMETER	SYMBOL	-60/-70/-80		UNITS
		MIN	MAX	
RST# HIGH recovery to WE# (CE#) going LOW	^{t}RS	150		ns
CE# (WE#) setup to WE# (CE#) going LOW	^{t}CS	0		ns
Write pulse width	^{t}WP	40		ns
Data setup to WE# (CE#) going HIGH	^{t}DS	40		ns
Address setup to WE# (CE#) going HIGH	^{t}AS	40		ns
CE# (WE#) hold from WE# (CE#) HIGH	^{t}CH	0		ns
Data hold from WE# (CE#) HIGH	^{t}DH	0		ns
Address hold from WE# (CE#) HIGH	^{t}AH	0		ns
Write pulse width HIGH	^{t}WPH	20		ns
V_{PP} setup to WE# (CE#) going HIGH	^{t}VPS	200		ns
V_{PP} hold from valid SRD	$^{t}VPPH$	0		ns
WP# hold from valid SRD	^{t}RHH	0		ns
WP# setup to WE# (CE#) going HIGH	^{t}RHS	200		ns
WE# HIGH to OE# LOW	^{t}WOA	0		ns
Write recovery before READ	^{t}WOS	50		ns
WE# HIGH to output valid	^{t}WB	$^{t}AA+20$		ns
WE# HIGH to address valid	^{t}WAV	0		ns
WE# HIGH to CLK valid	^{t}WCV	12		ns
WE# HIGH to ADV# HIGH	^{t}WAH	12		ns

Table 25: ERASE and PROGRAM Timing Requirements

OPERATION	PARAMETER	DESCRIPTION	V_{PP1}		V_{PP2}		UNIT	NOTES
			TYP	MAX	TYP	MAX		
Erasing and Suspending								
Erase Time	$^{t}ERS/PB$	4 KW parameter block	0.3	2.5	0.25	2.5	s	1, 2
	$^{t}ERS/MB$	32 KW main block	0.7	4	0.4	4	s	1, 2
Suspend Latency	$^{t}SUSP/P$	PROGRAM SUSPEND	5	10	5	10	µs	1
	$^{t}SUSP/E$	ERASE SUSPEND	5	20	5	20	µs	1
Conventional Word Programming								
Program Time	$^{t}PROG/W$	Single word	8	150	8	130	µs	1, 3
	$^{t}PROG/PB$	4 KW parameter block	0.03	0.07	0.03	0.07	s	1, 2
	$^{t}PROG/MB$	32 KW main block	0.24	0.6	0.24	0.6	s	1, 2
Fast Programming Algorithm								
Program	$^{t}FPA/W$	Single word	3.5	16	3.5	16	µs	
	$^{t}FPA/PB$	4KW parameter block	15		15		ms	1, 2
	$^{t}FPA/MB$	32KW main block	120		120		ms	1, 2
Operation Latency	$^{t}FPA/SETUP$	FPA Setup		5		5	µs	
	$^{t}FPA/TRAN$	Program-to-verify transition	2.7	5.6	2.7	5.6	µs	
	$^{t}FPA/VERIFY$	Verify	1.7	150	1.7	130	µs	

NOTE:
1. Excludes external system-level overhead.
2. Exact results may vary based on system overhead.
3. Measurements are based on T = 25°C and nominal voltage conditions unless otherwise specified.

Figure 21: Single Asynchronous READ Operation (Nonlatched Mode)

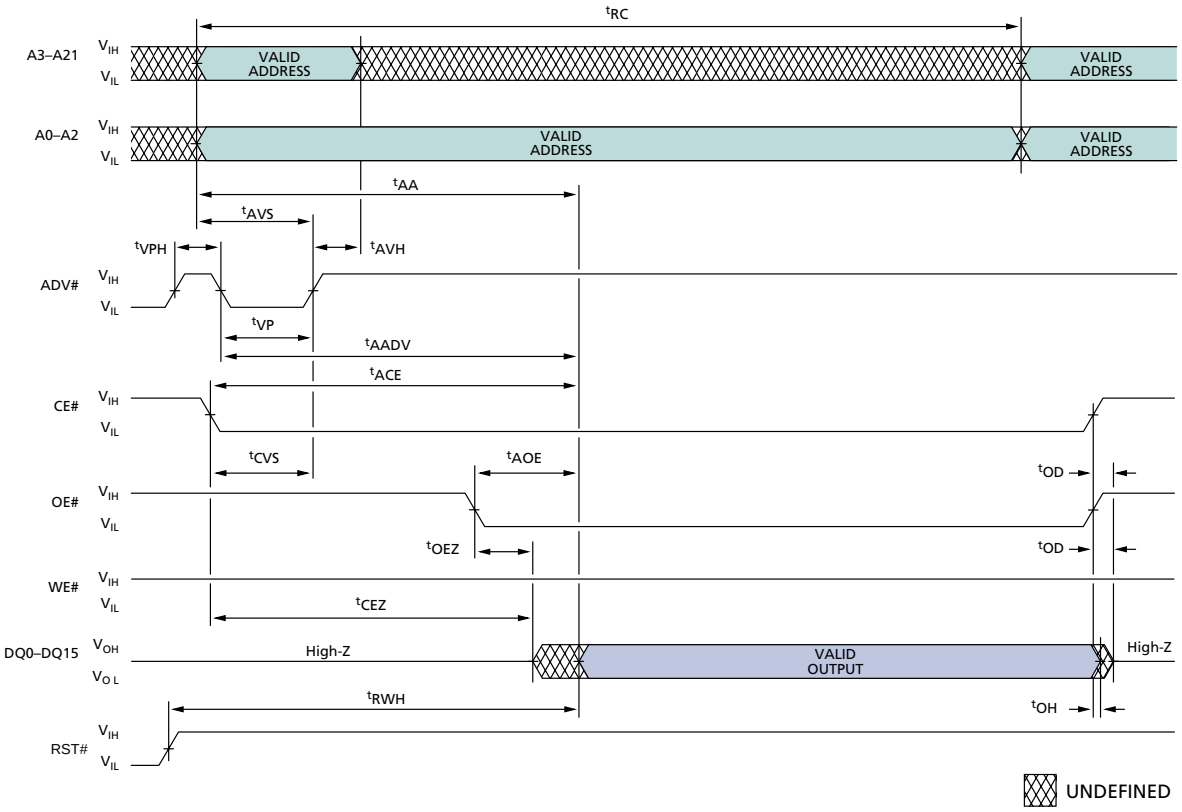


READ Timing Parameters

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tRC	60		70		80		ns
^tAA		60		70		80	ns
^tACE		60		70		80	ns
^tAOE		20		30		30	ns
^tRWH		150		150		150	ns

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tCEZ	0		0		0		ns
^tOEZ	0		0		0		ns
^tOD		5		20		20	ns
^tOH	0		0		0		ns

Figure 22: Latched Asynchronous READ Operation

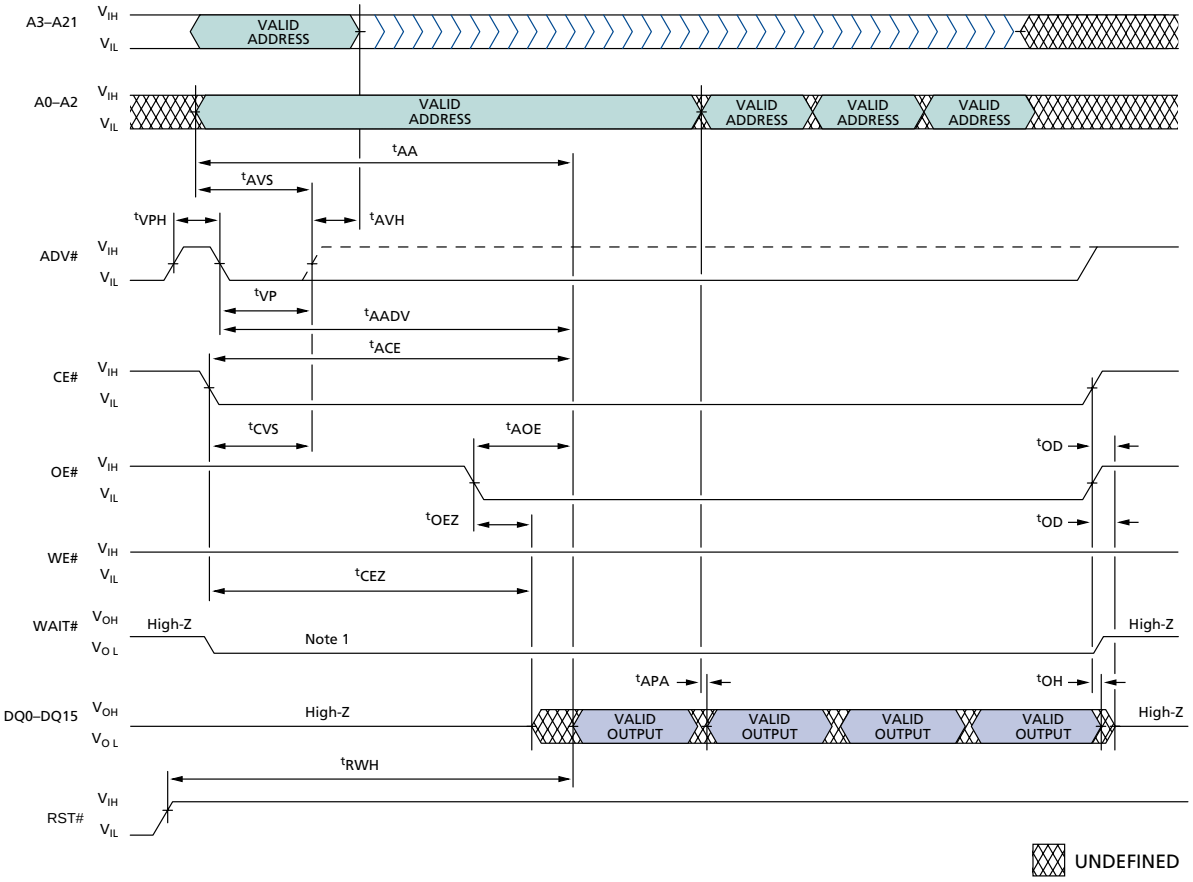


READ Timing Parameters

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}		60		70		80	ns
t_{ACE}		60		70		80	ns
t_{AOE}		20		30		30	ns
t_{RWH}		150		150		150	ns
t_{CEZ}	0		0		0		ns
t_{OEZ}	0		0		0		ns
t_{OD}		5		20		20	ns
t_{AVS}	7		7		10		ns

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{OH}	0		0		0		ns
t_{CVS}	7		7		10		ns
t_{AADV}		60		70		80	ns
t_{VP}	7		7		10		ns
t_{VPH}	7		7		10		ns
t_{AVH}	7		7		9		ns
t_{RC}		60	70		80		ns

Figure 23: Page Mode READ Operation



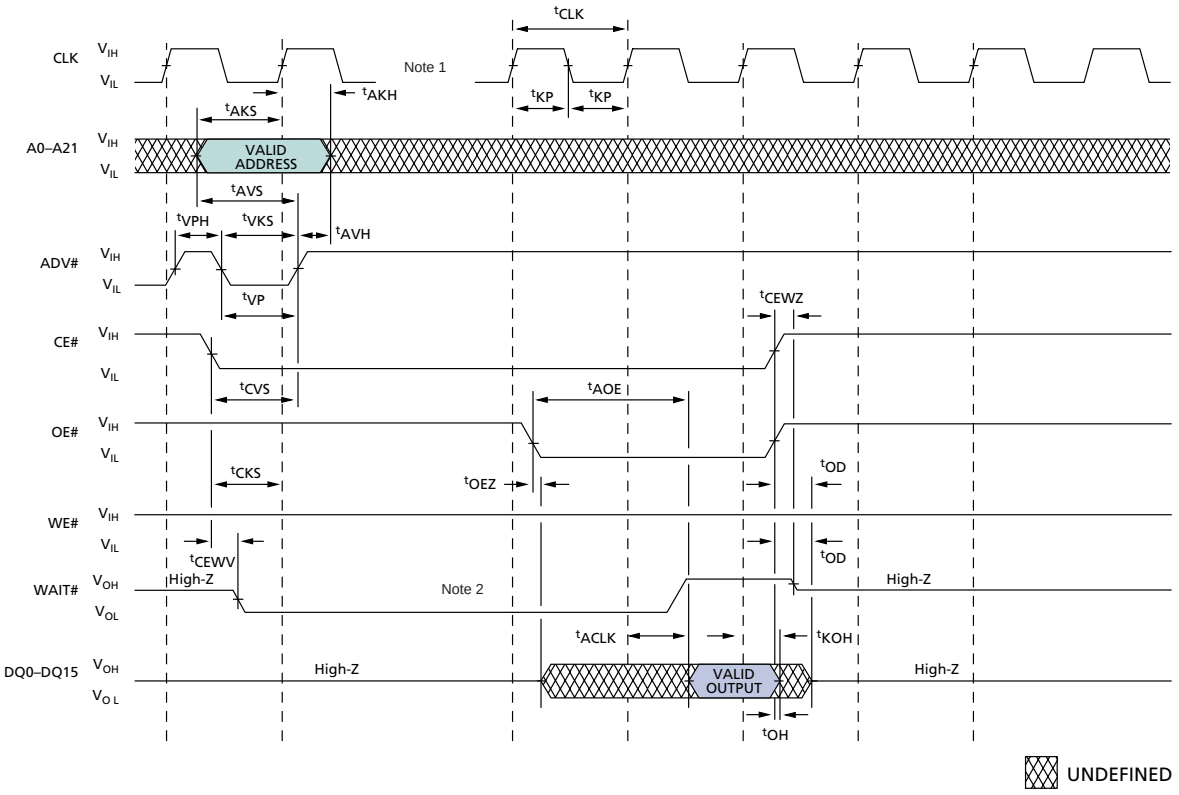
NOTE:
1. WAIT# is shown active LOW.

READ Timing Parameters

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}		60		70		80	ns
t_{ACE}		60		70		80	ns
t_{AOE}		20		30		30	ns
t_{RWH}		150		150		150	ns
t_{CEZ}	0		0		0		ns
t_{OEZ}	0		0		0		ns
t_{OD}		5		20		20	ns
t_{OH}	0		0		0		ns

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVS}	7		7		10		ns
t_{CVS}	7		7		10		ns
t_{AADV}		60		70		80	ns
t_{VP}	7		7		10		ns
t_{VPH}	7		7		10		ns
t_{AVH}	7		7		9		ns
t_{APA}		17		22		22	ns

Figure 24: Single Burst READ Operation



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.
2. WAIT# is shown active LOW, and WAIT# configured during delay (RCR8 = 0, RCR10 = 0).

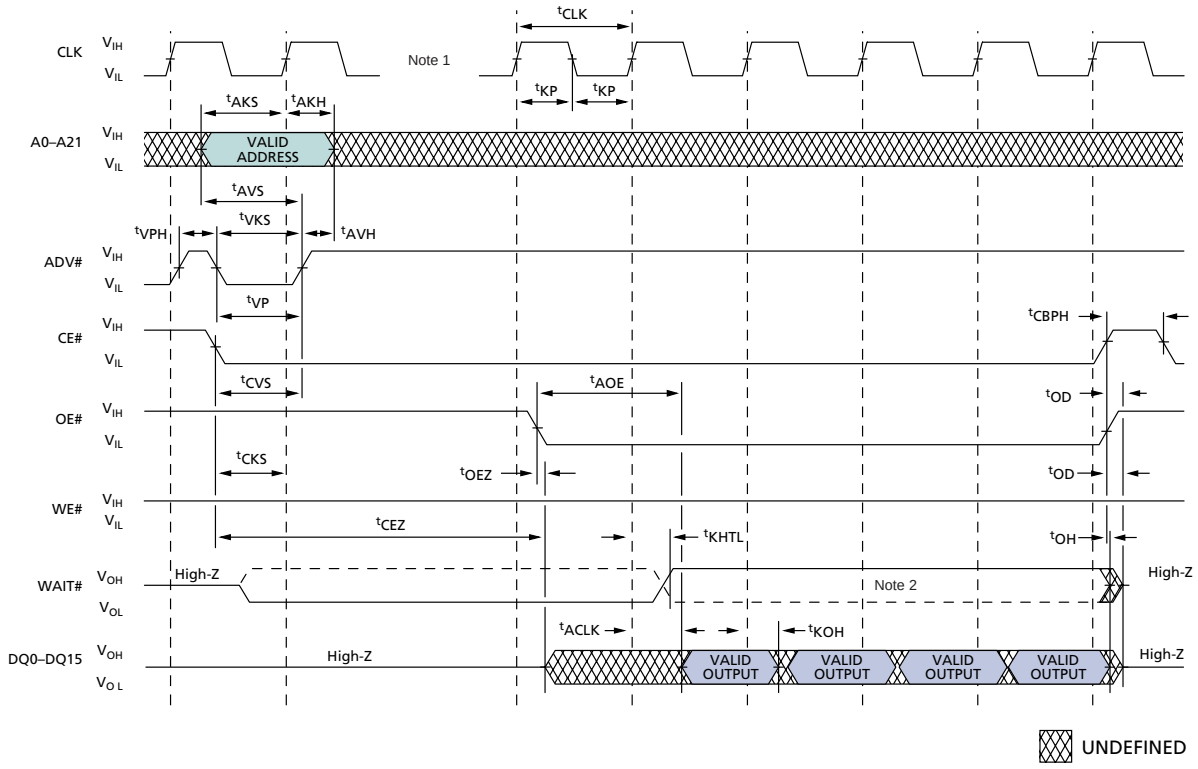
READ Timing Parameters

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{AOE}		20		30		30	ns
t_{OEZ}	0		0		0		ns
t_{OD}		5		20		20	ns
t_{AVS}	7		7		10		ns
t_{CVS}	7		7		10		ns
t_{VP}	7		7		10		ns
t_{VPH}	7		7		10		ns
t_{AVH}	7		7		9		ns
t_{OH}	0		0		0		ns
t_{AKS}	7		7		9		ns
t_{VKS}	7		7		10		ns
t_{CKS}	7		7		9		ns

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{ACLK}[1]		11		14		20	ns
t_{ACLK}[2]		20		20		20	ns
t_{KOH}	3		3		3		ns
t_{AKH}	7		7		10		ns
t_{CEWZ}		TBD		14		20	ns
t_{CLK}	15		18.5		25		ns
t_{CEWV}		14		14		20	ns
t_{KP}	3		6		9.5		

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 25: READ Timing Parameters for Four-Word Burst Operation



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.
2. WAIT# is shown active LOW, and WAIT# configured during delay (RCR8 = 0, RCR10 = 0).

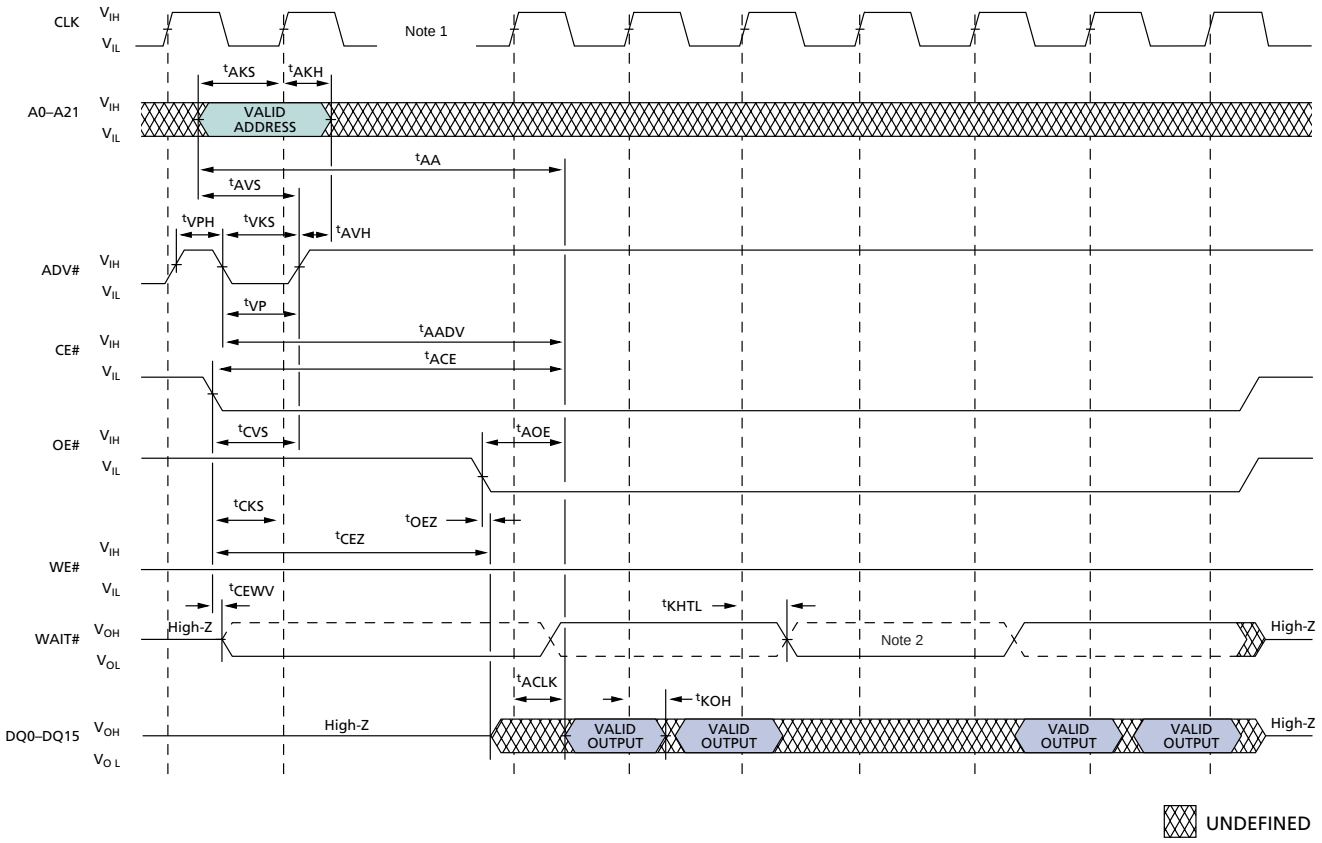
READ Timing Parameters

	-606		-705		-804		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^tAOE		20		30		30	ns
^tOEZ	0		0		0		ns
^tCEZ	0		0		0		ns
^tOD		5		20		20	ns
^tAVS	7		7		10		ns
^tCVS	7		7		10		ns
^tVP	7		7		10		ns
^tVPH	7		7		10		ns
^tAVH	7		7		9		ns
^tOH	0		0		0		ns
^tAKS	7		7		9		ns
^tVKS	7		7		10		ns
^tCKS	7		7		9		ns

	-606		-705		-804		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^tACLK[1]		11		14		20	ns
^tACLK[2]		20		20		20	ns
^tKOH	3		3		3		ns
^tAKH	7		7		10		ns
^tKHTL		11		14		20	ns
^tCLK	15		18.5		25		ns
^tCBPH	14		18		18		ns
^tKP	3		6		9.5		

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 26: WAIT# Functionality for End-of-Word Line (EOWL) Condition



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.
2. WAIT# is shown active LOW, and WAIT# configured during delay (RCR8 = 0, RCR10 = 0).

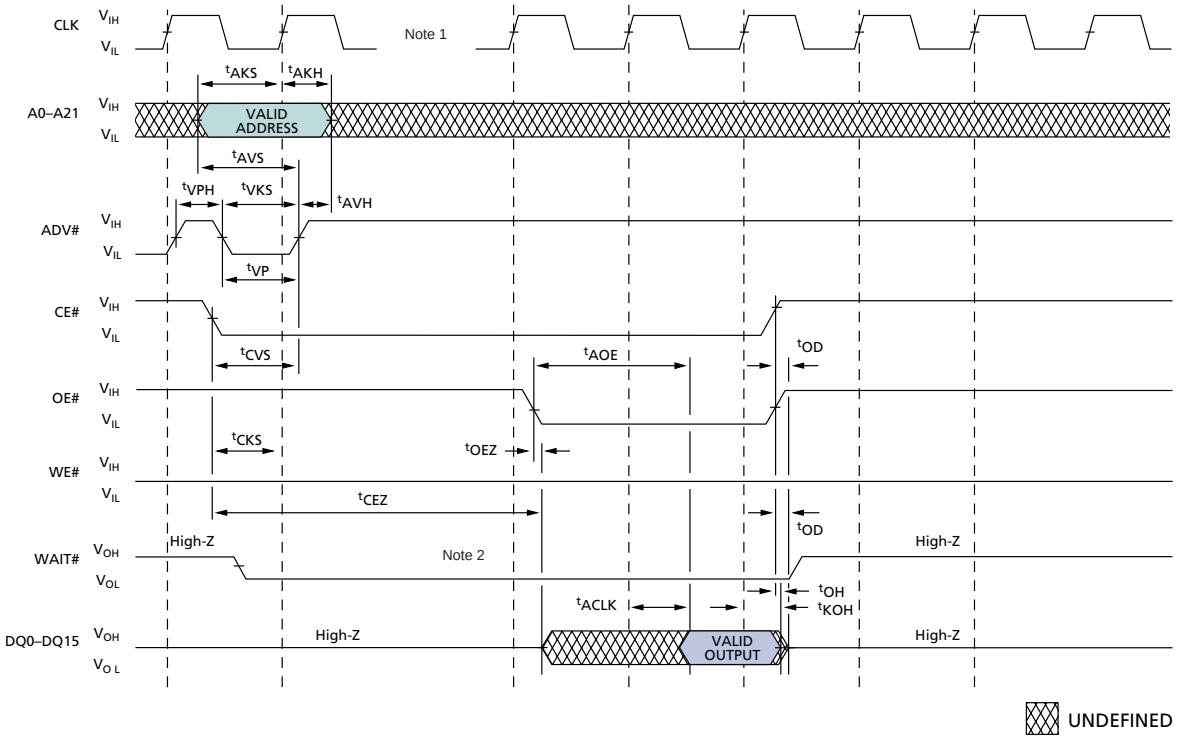
READ Timing Parameters

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{AKS}	7		7		9		ns
t_{VKS}	7		7		10		ns
t_{CKS}	7		7		9		ns
t_{ACLK}[1]		11		14		20	ns
t_{ACLK}[2]		20		20		20	ns
t_{KOH}	3		3		3		ns
t_{AKH}	7		7		10		ns
t_{KHTL}		11		14		20	ns
t_{CEWV}		TBD		14		20	ns
t_{AA}		60		70		80	ns
t_{AVS}	7		7		10		ns
t_{AVH}	7		7		9		ns

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{VP}	7		7		10		ns
t_{VPH}	7		7		10		ns
t_{AADV}		60		70		80	ns
t_{ACE}		60		70		80	ns
t_{AOE}		20		30		30	ns
t_{CVS}	7		7		10		ns
t_{OEZ}	0		0		0		ns
t_{CEZ}	0		0		0		ns

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 27: WAIT# Signal in Burst Non-Read Array Operation



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.
2. WAIT# is shown active LOW, and WAIT# configured during delay (RCR8 = 0, RCR10 = 0).

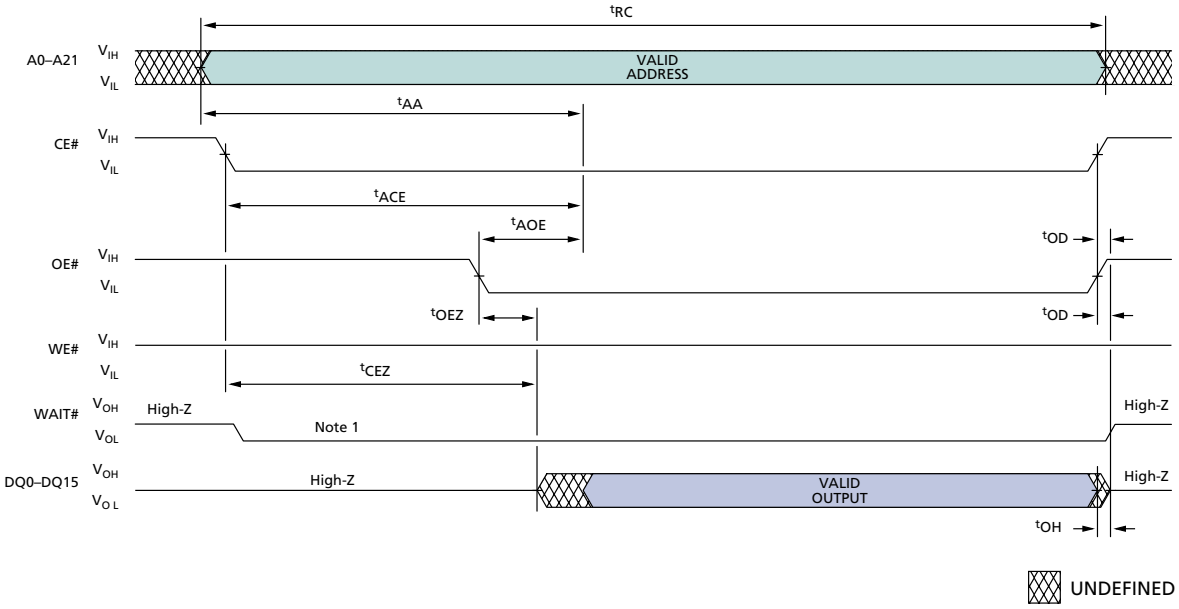
READ Timing Parameters

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{AOE}		20		30		30	ns
t_{OEZ}	0		0		0		ns
t_{CEZ}	0		0		0		ns
t_{OD}		5		20		20	ns
t_{OH}	0		0		0		ns
t_{AVS}	7		7		10		ns
t_{CVS}	7		7		10		ns
t_{VP}	7		7		10		ns
t_{VPH}	7		7		10		ns
t_{AVH}	7		7		9		ns
t_{AKS}	7		7		9		ns

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
t_{VKS}	7		7		10		ns
t_{CKS}	7		7		9		ns
t_{ACLK}[1]		11		14		20	ns
t_{ACLK}[2]		20		20		20	ns
t_{KOH}	3		3		3		ns
t_{AKH}	7		7		10		ns

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 28: WAIT# Signal in Asynchronous READ Operation



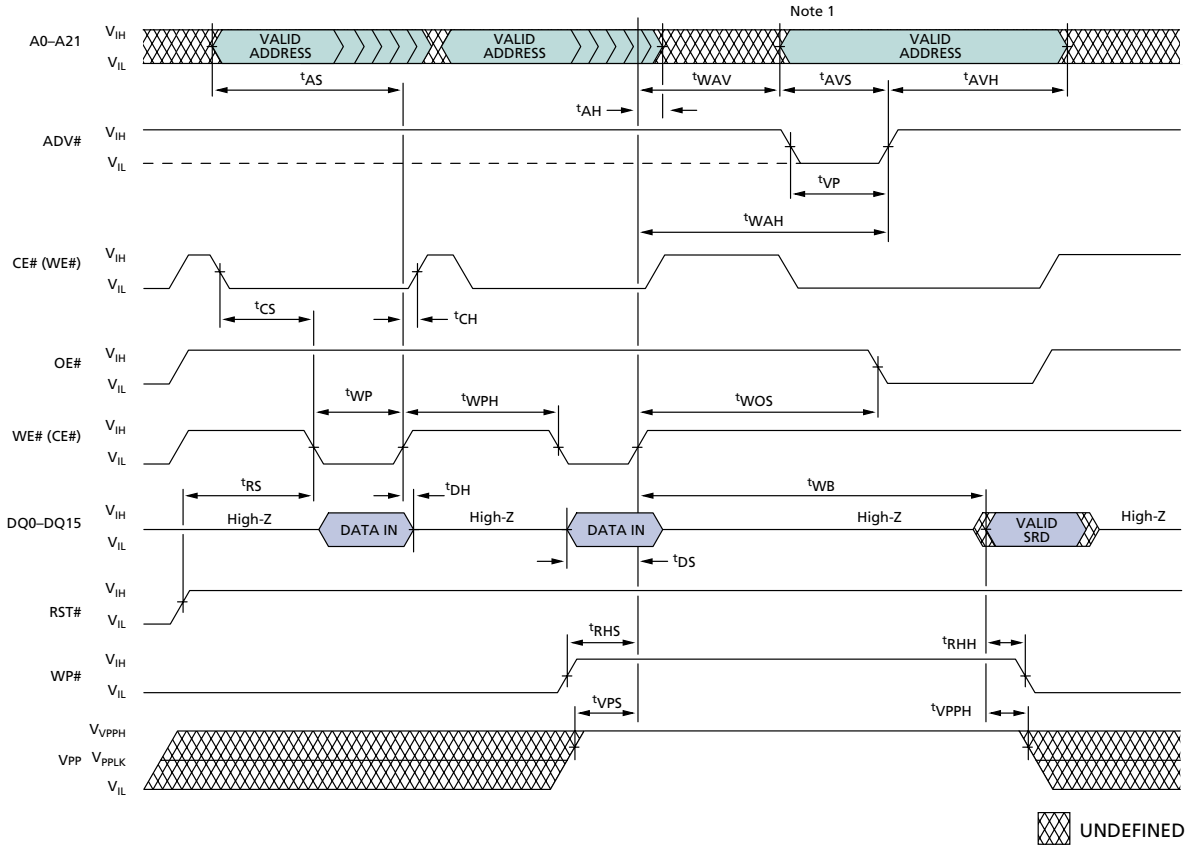
NOTE:
1. WAIT# shown active LOW.

READ Timing Parameters

SYMBOL	-60 MIN	-60 MAX	-70 MIN	-70 MAX	-80 MIN	-80 MAX	UNITS
t_{RC}	60		70		80		ns
t_{AA}		60		70		80	ns
t_{ACE}		60		70		80	ns
t_{AOE}		20		30		30	ns

SYMBOL	-60 MIN	-60 MAX	-70 MIN	-70 MAX	-80 MIN	-80 MAX	UNITS
t_{CEZ}	0		0		0		ns
t_{OEZ}	0		0		0		ns
t_{OD}		5		20		20	ns
t_{OH}	0		0		0		ns

Figure 29: Two-Cycle WRITE Operation



NOTE:

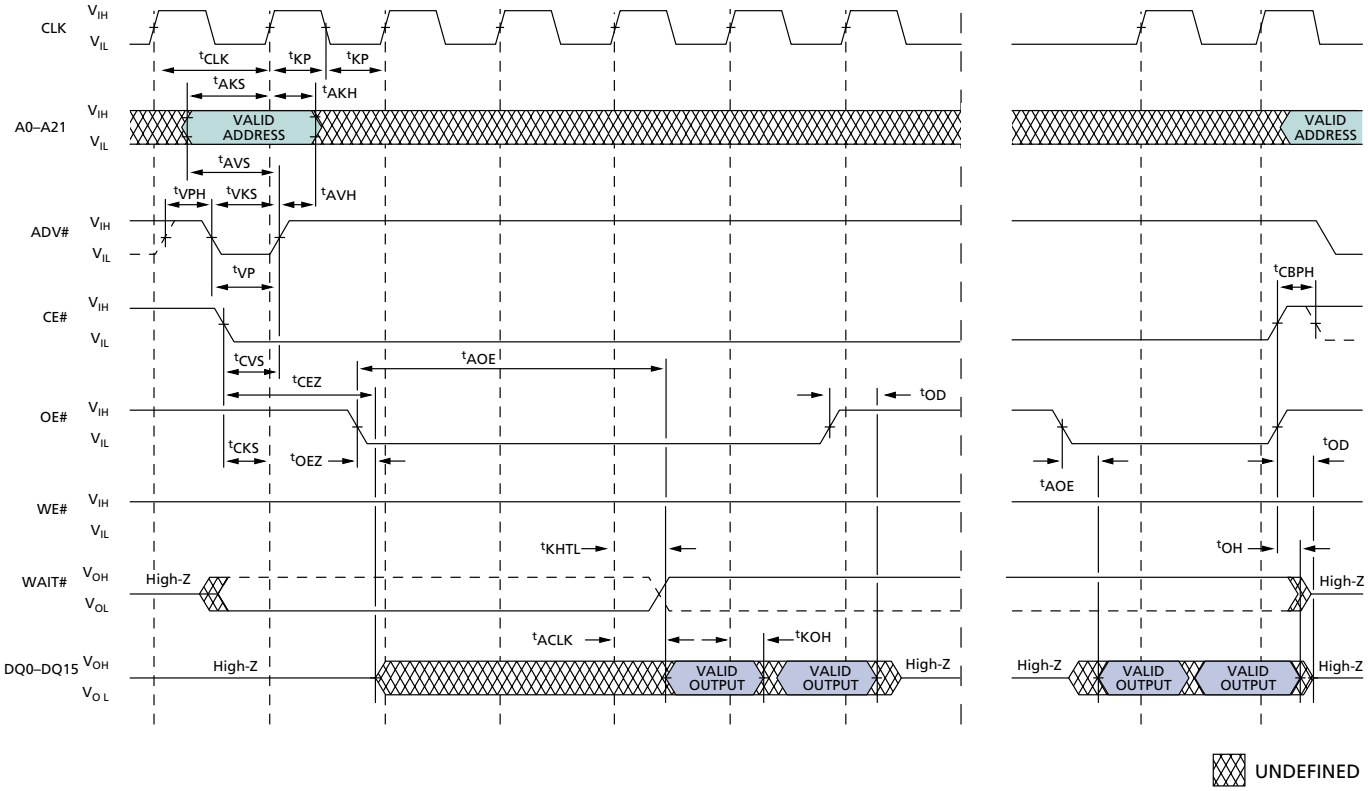
1. Status register data (SRD) may be read after a two-cycle PROGRAM/ERASE sequence to determine completion of the PROGRAM/ERASE algorithm.

WRITE Timing Parameters

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
t_{RS}	150		ns
t_{CS}	0		ns
t_{WP}	40		ns
t_{DS}	40		ns
t_{AS}	40		ns
t_{CH}	0		ns
t_{DH}	0		ns
t_{AH}	0		ns
t_{AVH}	7/ 7/ 9		ns
t_{AVS}	7/ 7/ 10		ns

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
t_{WPH}	20		ns
t_{VP}	7/ 7/ 10		ns
t_{VPS}	200		ns
t_{VPPH}	0		ns
t_{RHH}	0		ns
t_{RHS}	200		ns
t_{WOS}	50		ns
t_{WB}	t_{AA}+20		ns
t_{WAV}	0		ns
t_{WAH}	12		ns

Figure 30: Clock Suspend



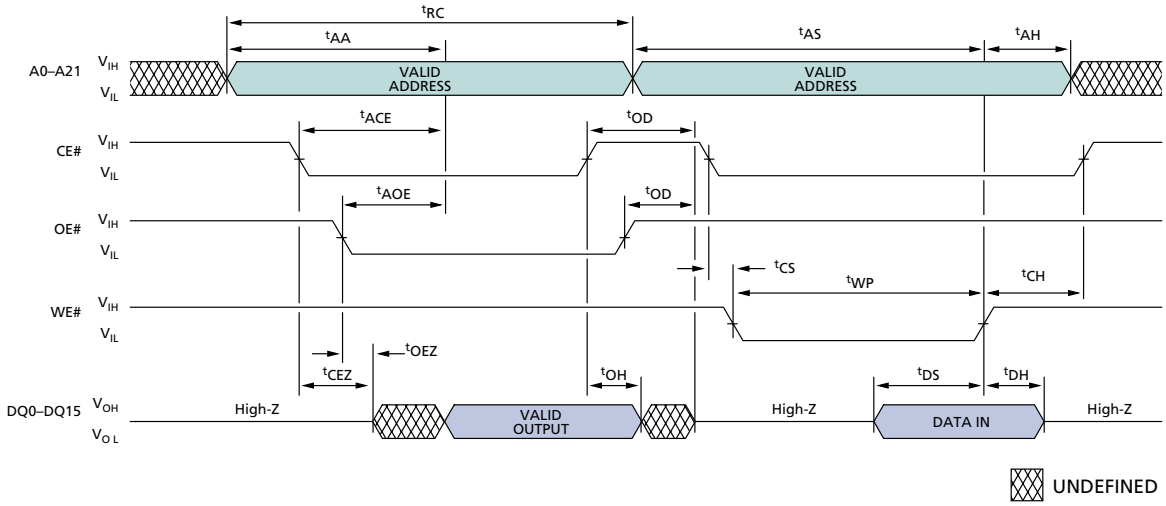
READ Timing Parameters

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
^tAOE		20		30		30	ns
^tOD		5		20		20	ns
^tOH	0		0		0		ns
^tAVS	7		7		10		ns
^tCVS	7		7		10		ns
^tVP	7		7		10		ns
^tVPH	7		7		10		ns
^tAVH	7		7		9		ns
^tOEZ	0		0		0		ns
^tAKS	7		7		9		ns
^tVKS	7		7		10		ns
^tCKS	7		7		9		ns
^tCLK	15		18.5		25		ns

SYMBOL	-606 MIN	-606 MAX	-705 MIN	-705 MAX	-804 MIN	-804 MAX	UNITS
^tACLK[1]		11		14		20	ns
^tACLK[2]		20		20		20	ns
^tKOH	3		3		3		ns
^tAKH	7		7		10		ns
^tKP	3		6		9.5		ns
^tCEZ	0		0		0		ns
^tKHKL		2		3		3	ns
^tCBPH	14		18		18		ns
^tKHTL		11		14		20	ns

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 31: Asynchronous READ-to-WRITE Operation



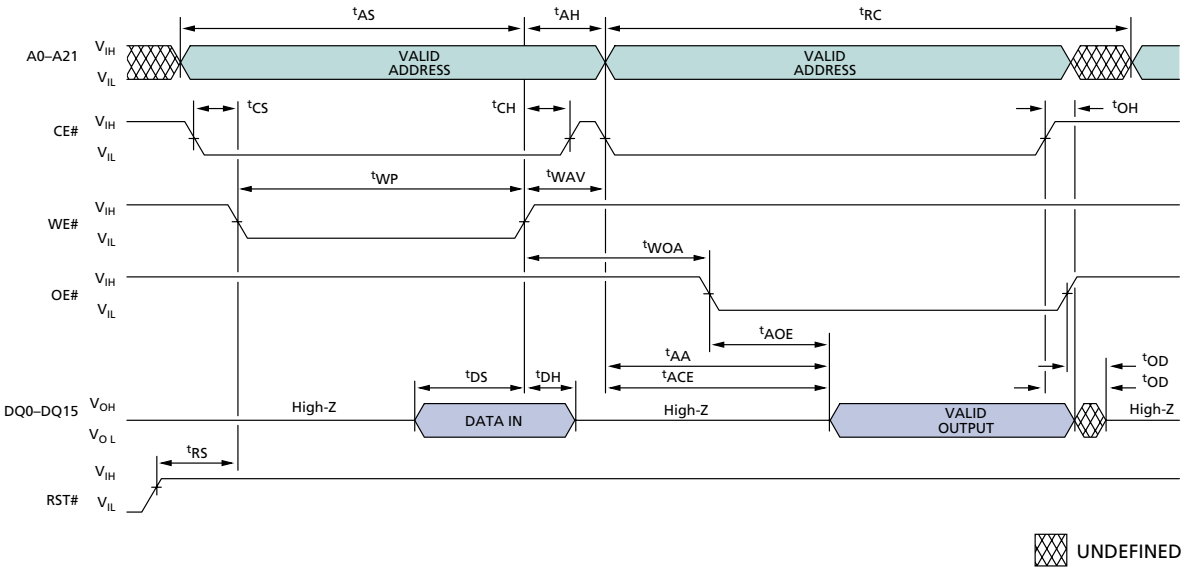
READ Timing Parameters

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	60		70		80		ns
t_{AA}		60		70		80	ns
t_{ACE}		60		70		80	ns
t_{AOE}		20		30		30	ns
t_{OD}		5		20		20	ns
t_{OH}	0		0		0		ns
t_{OEZ}	0		0		0		ns
t_{CEZ}	0		0		0		ns

WRITE Timing Parameters

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
t_{CS}	0		ns
t_{WP}	40		ns
t_{DS}	40		ns
t_{AS}	40		ns
t_{CH}	0		ns
t_{DH}	0		ns
t_{AH}	0		ns

Figure 32: WRITE-to-Asynchronous-READ Operation



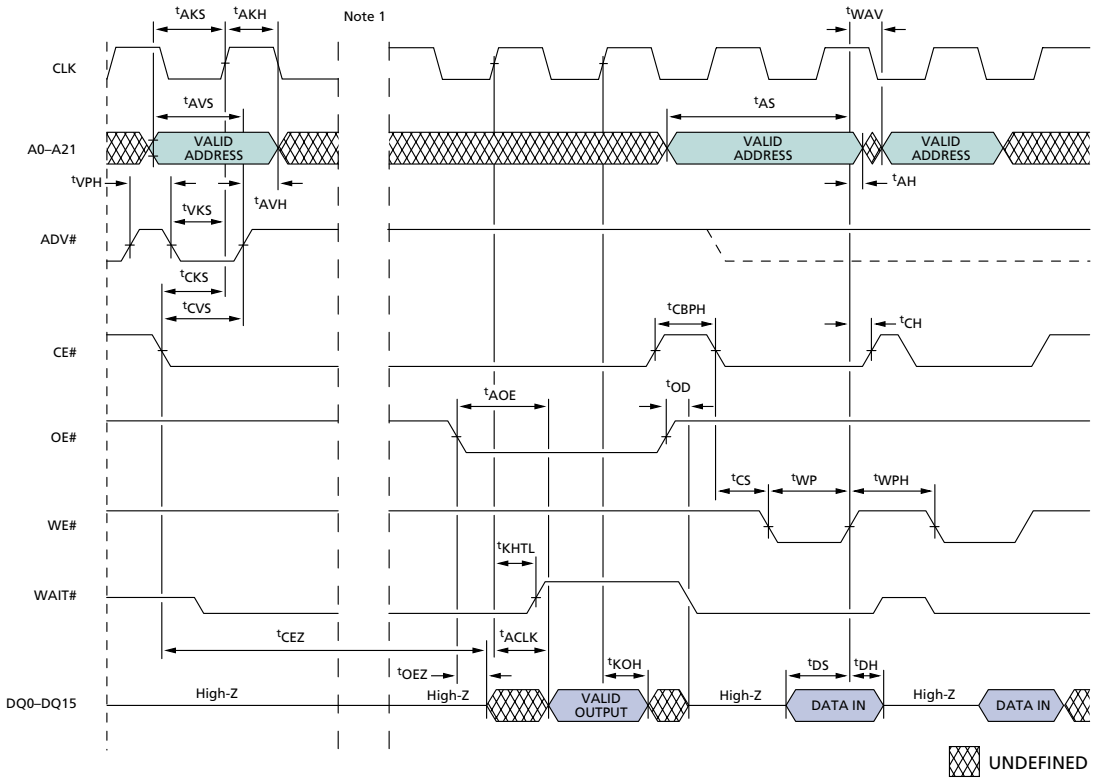
READ Timing Parameters

SYMBOL	-60		-70		-80		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tRC	60		70		80		ns
^tAA		60		70		80	ns
^tACE		60		70		80	ns
^tAOE		20		30		30	ns
^tOD		5		20		20	ns
^tOH	0		0		0		ns

WRITE Timing Parameters

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
^tRS	150		ns
^tCS	0		ns
^tWP	40		ns
^tDS	40		ns
^tAS	40		ns
^tCH	0		ns
^tDH	0		ns
^tAH	0		ns
^tWOA	0		ns
^tWAV	0		ns

Figure 33: Burst READ-to-WRITE Operation



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.

READ Timing Parameters

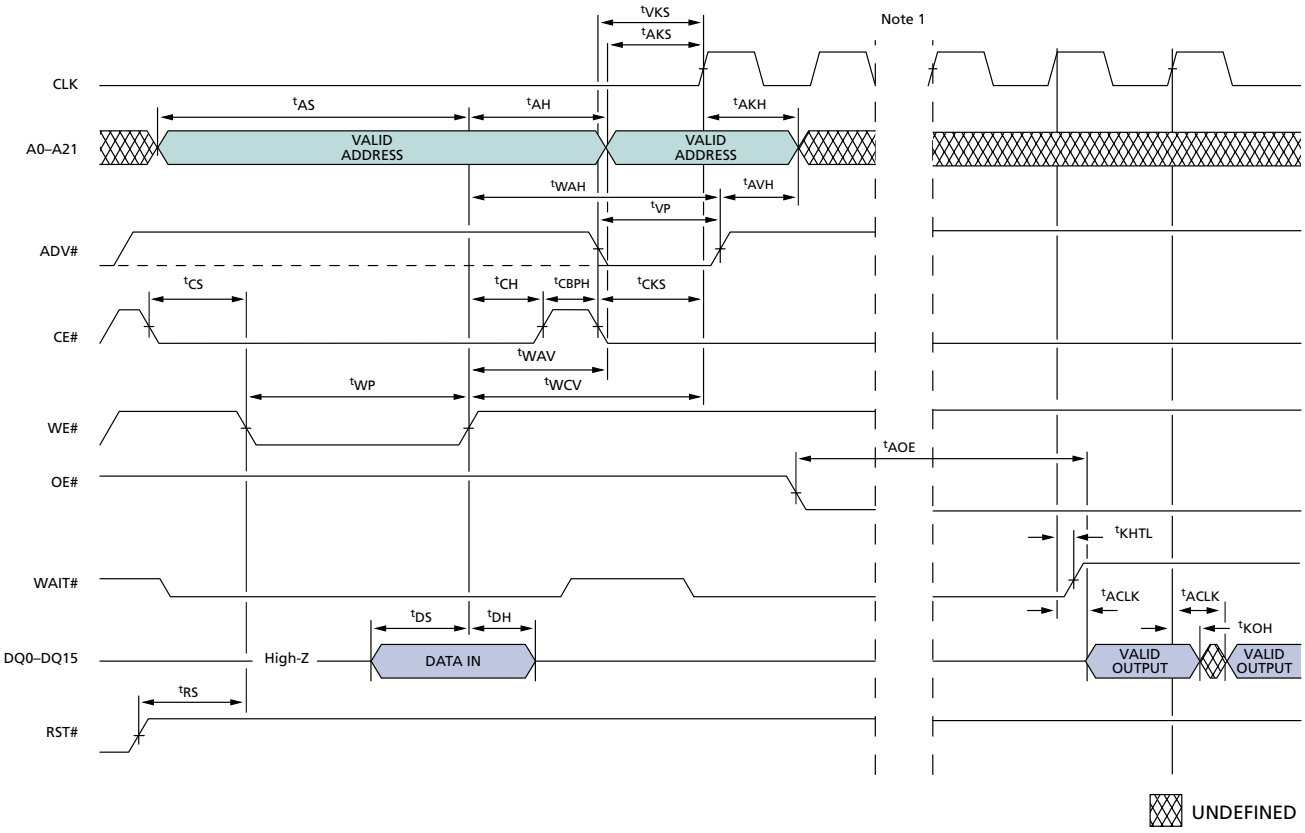
SYMBOL	-606		-705		-804		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tAKS	7		7		9		ns
^tVKS	7		7		10		ns
^tAKH	7		7		10		ns
^tAVS	7		7		10		ns
^tVPH	7		7		10		ns
^tAVH	7		7		9		ns
^tCVS	7		7		10		ns
^tCKS	7		7		9		ns
^tAOE		20		30		30	ns
^tKHTL		11		14		20	ns
^tOEZ	0		0		0		ns
^tCEZ	0		0		0		ns
^tOD		5		20		20	ns
^tKOH	3		3		3		ns
^tCBPH	14		18		18		ns
^tACLK[1]		11		14		20	ns
^tACLK[2]		20		20		20	ns

WRITE Timing Parameters

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
^tCS	0		ns
^tAS	40		ns
^tDS	40		ns
^tCH	0		ns
^tDH	0		ns
^tWP	40		ns
^tAH	0		ns
^tWPH	20		ns
^tWAV	0		ns

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Figure 34: Write-to-Burst READ Operation



NOTE:
1. Figure 6 on page 20 describes how to insert clock cycles during initial access.

READ Timing Parameters

SYMBOL	-606		-705		-804		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tAKS	7		7		9		ns
^tVKS	7		7		10		ns
^tAKH	7		7		10		ns
^tAVH	7		7		9		ns
^tCKS	7		7		9		ns
^tAOE		20		30		30	ns
^tKHTL		11		14		20	ns
^tKOH	3		3		3		ns
^tACLK[1]		11		14		20	ns
^tACLK[2]		20		20		20	ns
^tVP	7		7		10		ns
^tCBPH	14		18		18		ns

WRITE Timing Parameters

SYMBOL	-60/-70/-80		UNITS
	MIN	MAX	
^tRS	150		ns
^tCS	0		ns
^tAS	40		ns
^tCH	0		ns
^tWP	40		ns
^tAH	0		ns
^tDS	40		ns
^tDH	0		ns
^tWAV	0		ns
^tWCV	12		ns
^tWAH	12		ns

NOTE:
1. Latency codes 3, 4, and 5.
2. Latency code 2.

Appendix A: CFI Table

Table 26: CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer's ID (ManID) Micron
	89h	Intel
01	44C6h/8864h	Device ID Code (DevID) Top boot block device ID code (Micron / Intel)
	44C7h/8865h	Bottom boot block device ID code (Micron / Intel)
02 – 0F	reserved	Reserved
10, 11	0051, 0052	"QR"
12	0059	"Y"
13, 14	0003, 0000	Primary OEM command set
15, 16	0039, 0000	Address for primary extended table
17, 18	0000, 0000	Alternate OEM command set
19, 1A	0000, 0000	Address for OEM extended table
1B	0017	V_{CC} MIN for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1C	0019	V_{CC} MAX for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1D	00B4	V_{PP} MIN for Erase/Write; Bit 7–bit 4 volts in Hex; Bit 3–bit 0 100mV in BCD
1E	00C6	V_{PP} MAX for Erase/Write; Bit 7–bit 4 volts in Hex; Bit 3–bit 0 100mV in BCD
1F	0004	Typical timeout for single byte/word program, 2^nµs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2^nµs, 0000 = not supported
21	000A	Typical timeout for individual block erase, 2^ns, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2^ns, 0000 = not supported
23	0004	Maximum timeout for single byte/word program, 2^nµs times typical, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2^nµs, 0000 = not supported
25	0002	Maximum timeout for individual block erase, 2^ns, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2^ns, 0000 = not supported
27	0017	Device size, 2^n bytes
28	0001	Bus interface x8 = 0, x16 = 1, x32 = 2, x64 = 3
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multibyte program or page, 2^n
2C	0002	Number of erase block regions within device (4K words and 32K words)
2D, 2E	007E, 0000	Top boot block device erase block region information 1
	0007, 0000	Bottom boot block device erase block region information 1
2F, 30	0000, 0001	Top boot block device erase block region information 1
	0020, 0000	Bottom boot block device erase block region information 1
31, 32	0007, 0000	Top boot block device erase block region information 2
	007E, 0000	Bottom boot block device erase block region information 2
33, 34	0020, 0000	Top boot block device erase block region information 2
	0000, 0001	Bottom boot block device erase block region information 2
35, 36	0000, 0000	Reserved for future erase block region information
37, 38	0000, 0000	Reserved for future erase block region information
39, 3A	0050, 0052	"PR"

Table 26: CFI (continued)

OFFSET	DATA	DESCRIPTION
3B	0049	"I"
3C	0031	Major version number, ASCII
3D	0033	Minor version number, ASCII
3E 3F 40 41	00E6 0003 0000 0000	Optional Feature and Command Support Bit 0 Chip erase supported no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1 Bit 8 Synchronous read supported = yes = 1 Bit 9 Simultaneous operation supported = yes = 1
42	0001	Program supported after erase suspend = yes
43, 44	0003, 0000	Bit 0 block lock status active = yes; Bit 1 block lock down active = yes
45	0018	V_{CC} supply optimum, 00 = not supported, Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
46	00C0	V_{PP} supply optimum, 00 = not supported, Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
47	0001	Number of protection register fields in JEDEC ID space
48, 49	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
4A, 4B	0003, 0003	2^n factory programmed bytes, 2^n user programmable bytes
4C	0004	Page mode read capability
4D	0003	Number of synchronous mode read configuration fields that follow
4E	0001	Synchronous mode read capability configuration 1
4F	0002	Synchronous mode read capability configuration 2
50	0007	Synchronous mode read capability configuration 3
51	0000	Synchronous mode read capability configuration 4
52	Top:0002 Bot:0002	Number of device hardware partition regions within the device
53	Top: 000F Bot: 0001	Number of identical partitions within the partition region
54	Top: 0000 Bot: 0000	Number of identical partitions within the partition region
55	Top: 0011 Bot: 0011	Number of PROGRAM/ERASE operations allowed in a partition
56	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
57	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
58	Top: 0001 Bot: 0002	Types of erase block regions in this partition region
59	Top: 0007 Bot: 0007	Partition region 1 erase block type 1 information
5A	Top: 0000 Bot: 0000	Partition region 1 erase block type 1 information
5B	Top: 0000 Bot: 0020	Partition region 1 erase block type 1 information

Table 26: CFI (continued)

OFFSET	DATA	DESCRIPTION
5C	Top: 0001 Bot: 0000	Partition region 1 erase block type 1 information
5D	Top: 0064 Bot: 0064	Partition 1 (erase block type 1)
5E	Top: 0000 Bot: 0000	Partition 1 (erase block type 1)
5F	Top: 0001 Bot: 0001	Partition 1 (erase block type 1) bits per cell; internal ECC
60	Top: 0003 Bot: 0003	Partition 1 (erase block type 1) page mode and synchronous mode capabilities
Bot: 61	Bot: 0006	Partition region 1 erase block type 2 information
Bot: 62	Bot: 0000	Partition region 1 erase block type 2 information
Bot: 63	Bot: 0000	Partition region 1 erase block type 2 information
Bot: 64	Bot: 0001	Partition region 1 erase block type 2 information
Bot: 65	Bot: 0064	Partition region 1 (erase block type 2)
Bot: 66	Bot: 0000	Partition region 1 (erase block type 2)
Bot: 67	Bot: 0001	Partition region 1 (erase block type 2) bits per cell
Bot: 68	Bot: 0003	Partition region 1 (erase block type 2) page mode and synchronous mode capabilities
Top: 61 Bot: 69	Top: 0001 Bot: 000F	Number of identical partitions within the partition region
Top: 62 Bot: 6A	Top: 0000 Bot: 0000	Number of identical partitions within the partition region
Top: 63 Bot: 6B	Top: 0011 Bot: 0011	Number of PROGRAM/ERASE operations allowed in a partition
Top: 64 Bot: 6C	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
Top: 65 Bot: 6D	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
Top: 66 Bot: 6E	Top: 0002 Bot: 0001	Types of erase block regions in this partition region
Top: 67 Bot: 6F	Top: 0006 Bot: 0007	Partition region 2 erase block type 1 information
Top: 68 Bot: 70	Top: 0000 Bot: 0000	Partition region 2 erase block type 1 information
Top: 69 Bot: 71	Top: 0000 Bot: 0000	Partition region 2 erase block type 1 information

Table 26: CFI (continued)

OFFSET	DATA	DESCRIPTION
Top: 6A	Top: 0001	Partition region 2 erase block type 1 information
Bot: 72	Bot: 0001	
Top: 6B	Top: 0064	Partition 2 (erase block type 1)
Bot: 73	Bot: 0064	
Top: 6C	Top: 0000	Partition 2 (erase block type 1)
Bot: 74	Bot: 0000	
Top: 6D	Top: 0001	Partition 2 (erase block type 1) bits per cell
Bot: 75	Bot: 0001	
Top: 6E	Top: 0003	Partition 2 (erase block type 1) page mode and synchronous mode capabilities
Bot: 76	Bot: 0003	
Top:6F	Top: 0007	Partition region 2 erase block type 2 information
Top: 70	Top: 0000	Partition region 2 erase block type 2 information
Top: 71	Top: 0020	Partition region 2 erase block type 2 information
Top: 72	Top: 0000	Partition region 2 erase block type 2 information
Top: 73	Top: 0064	Partition 2 (erase block type 2)
Top: 74	Top: 0000	Partition 2 (erase block type 2)
Top: 75	Top: 0001	Partition 2 (erase block type 2) bits per cell
Top: 76	Top: 0003	Partition 2 (erase block type 2) page mode and synchronous mode capabilities
77–7F		Reserved

Appendix B: CSM Table

Table 27: Command State Machine Transition Table

Note that this table shows that the command state transitions are based on incoming commands. Only one partition can actively program or erase at a time.

CURRENT CHIP STATE[8]		DEVICE NEXT STATE AFTER COMMAND INPUT																
		READ ARRAY[3] (FFh)	PROGRAM SETUP[4,5] (10h/40h)	ERASE SETUP[4,5] (20h)	FPA SETUP[4] (30h)	BLOCK ERASE CONFIRM, PROGRAM/ ERASE RESUME, UNLOCK BLOCK CONFIRM[9] (D0h)	PROGRAM/ ERASE SUSPEND (B0h)	READ STATUS (70h)	CLEAR STATUS REGISTER[6] (50h)	READ ID/ QUERY (90h, 98h)	LOCK, UNLOCK, LOCK DOWN, RCR SETUP[5] (60h)	OTP SETUP[5] (C0h)	LOCK BLOCK CONFIRM[9] (01h)	LOCK DOWN BLOCK CONFIRM[9] (2Fh)	WRITE RCR CONFIRM[9] (03h)	FPA EXIT (ADDRESS <> BA) (FFFFh)	ILLEGAL COMMANDS OR FPA DATA (OTHER CODES)[2]	WSM OPERATION COMPLETES
READY		Ready	Program Setup	Erase Setup	FPA Setup	Ready					Lock/RCR Setup	OTP Setup	Ready					N/A
LOCK/RCR SETUP		Ready (Lock Error)				Ready	Ready (Lock Error)						Ready			Ready (Lock Error)		N/A
OTP	SETUP	OTP Busy																N/A
	BUSY																	Ready
PROGRAM	SETUP	Program Busy																N/A
	BUSY	Program Busy					Program Suspend	Program Busy										Ready
	SUSPEND	Program Suspend				Program Busy	Program Suspend											N/A
ERASE	SETUP	Ready (Error)				Erase Busy	Ready (Error)											N/A
	BUSY	Erase Busy					Erase Suspend	Erase Busy										Ready
	SUSPEND	Erase Suspend	Program in Erase Suspend Setup	Erase Suspend	Erase Busy	Erase Suspend					Lock/RCR Setup in Erase Suspend	Erase Suspend						N/A
PROGRAM IN ERASE SUSPEND	SETUP	Program in Erase Suspend Busy																N/A
	BUSY	Program in Erase Suspend Busy					Program Suspend in Erase Suspend	Program in Erase Suspend Busy										Erase Suspend
	SUSPEND	Program Suspend in Erase Suspend				Program in Erase Suspend Busy	Program Suspend in Erase Suspend											N/A
LOCK/RCR SETUP IN ERASE SUPSEND		Erase Suspend (Lock Error)				Erase Suspend	Erase Suspend (Lock Error)						Erase Suspend			Erase Suspend (Lock Error)		N/A
FAST PROGRAM-MING ALGORITHM	SETUP	Ready (Error)				FPA Busy	Ready (Error)											N/A
	FPA BUSY	FPA Busy[7]														FPA Verify	FPA Busy[7]	
	FPA VERIFY	Verify Busy[7]														Ready	FPA Verify[7]	Ready

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Table 27: Command State Machine Transition Table (continued)

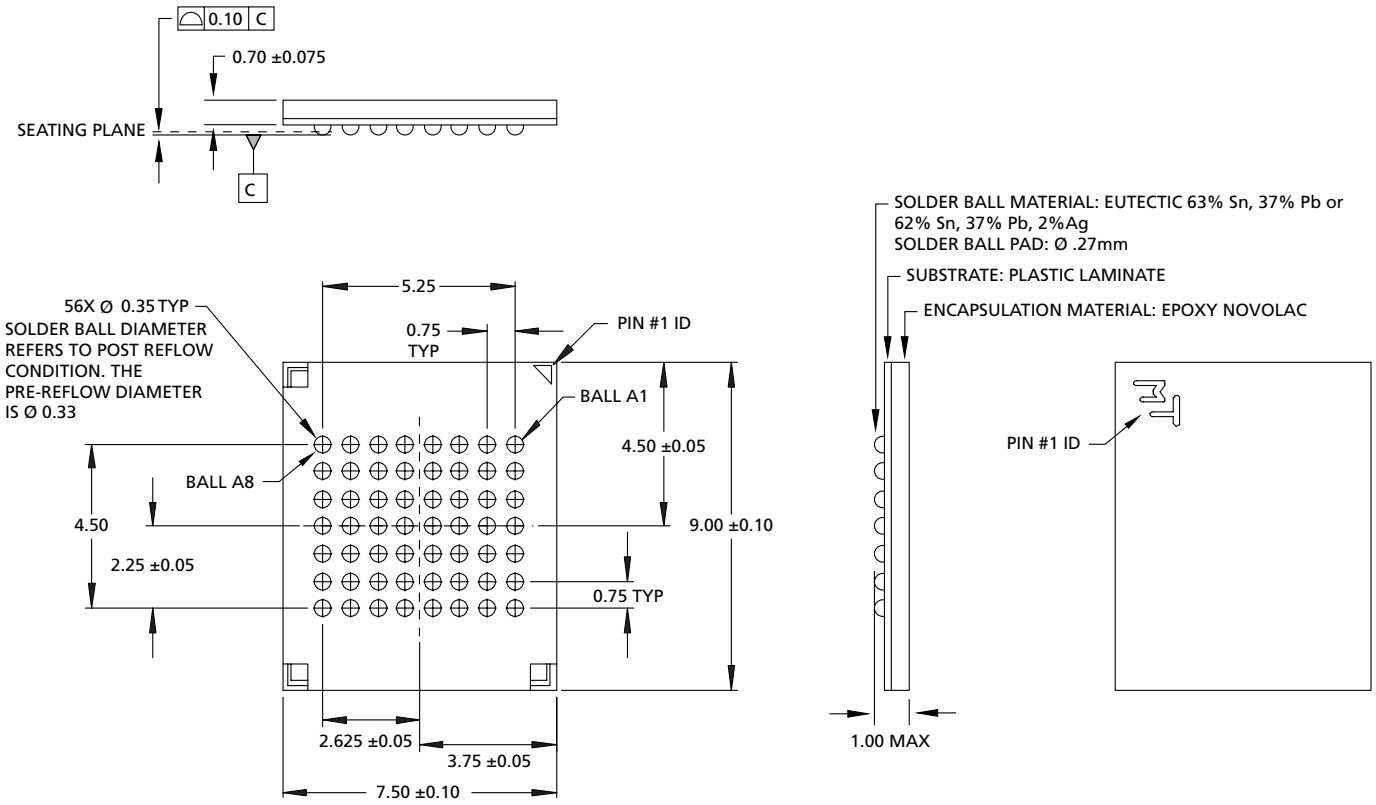
Note that this table shows that the command state transitions are based on incoming commands. Only one partition can actively program or erase at a time.

CURRENT CHIP STATE[8]	DEVICE NEXT STATE AFTER COMMAND INPUT																
	READ ARRAY[3] (FFh)	PROGRAM SETUP[4,5] (10h/40h)	ERASE SETUP[4,5] (20h)	FPA SETUP[4] (30h)	BLOCK ERASE CONFIRM, PROGRAM/ ERASE RESUME, UNLOCK BLOCK CONFIRM[9] (D0h)	PROGRAM/ ERASE SUSPEND (B0h)	READ STATUS (70h)	CLEAR STATUS REGISTER[6] (50h)	READ ID/ QUERY (90h, 98h)	LOCK, UNLOCK, LOCK DOWN, RCR SETUP[5] (60h)	OTP SETUP[5] (C0h)	LOCK BLOCK CONFIRM[9] (01h)	LOCK DOWN BLOCK CONFIRM[9] (2Fh)	WRITE RCR CONFIRM[9] (03h)	FPA EXIT (ADDRESS <> BA) (FFFFh)	ILLEGAL COMMANDS OR FPA DATA (OTHER CODES)[2]	WSM OPERATION COMPLETES
	OUTPUT NEXT STATE AFTER COMMAND INPUT[1]																
PROGRAM SETUP, ERASE SETUP, OTP SETUP, PROGRAM IN ERASE SUSPEND SETUP, FPA SETUP, FPA BUSY, VERIFY BUSY	Status																
LOCK/RCR SETUP, LOCK/RCR SETUP IN ERASE SUSPEND	Status													Array	Status		Output does not change
OTP BUSY	Array[3]	Status			Output does not change		Status	Output does not change	Status	Status		Output does not change			Array	Output does not change	
READY, PROGRAM BUSY, PROGRAM SUSPEND, ERASE BUSY, ERASE SUSPEND, PROGRAM IN ERASE SUSPEND BUSY, PROGRAM SUSPEND IN ERASE SUSPEND									Status ID/ Query								

NOTE:

1. The output state shows the type of data that appears at the outputs if the block address is the same as the command address.
2. Illegal commands are those not defined in the command set.
3. All blocks default to read array mode at power up.
4. Both cycles of two-cycle commands should be issued to the same block address. If they are issued to different blocks, the second WRITE determines the active block.
5. If the CSM is active, both cycles of a two-cycle command are ignored.
6. The CLEAR STATUS command clears the status register error bits except when the CSM is running or during SUSPEND.
7. FPA writes are allowed only when SR0 = 0. FPA is busy if BA = address at FPA CONFIRM command. Any other commands are treated as data.
8. The current state is that of the WSM, not the block.
9. Confirm commands perform the operation and the move to the ready state.

Figure 35: 56-Ball VFBGA



NOTE: 1. All dimensions in millimeters.

Data Sheet Designation

Production: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. C, Production 7/03

- Added Intel ManID variant
- Removed “Interleaved” Burst Option
- Expanded definition for ^{t}ACLK
- Addition of CFI ManID and DevID
- Updated VFBGA package drawing and notes
- Added value for V_{ILKOQ}
- Added value for ^{t}CEWV and ^{t}CEWZ

Rev. B, Preliminary 3/03

- Included W18 specifications
- Reformatted document
- Added Table of Contents, List of Figures, List of Tables

Original document, Rev. A, Preliminary 3/03