



The Infinite Bandwidth Company™

# MICRF005

115kbps, 800MHz - 1GHz UHF Receiver

## Final Information

### General Description

The MICRF005 QwikRadio™ UHF receiver is a single-chip OOK (on-off keyed) receiver IC for remote wireless applications. This device is a true single-chip, "antenna-in, data-out" device. All RF and IF tuning is accomplished automatically within the IC which eliminates manual tuning production costs and results in a highly reliable, extremely low-cost solution for high-volume wireless applications.

The MICRF005 provides two additional key features: (1) A transmit standby mode, and (2) a shutdown mode which may be used for duty-cycle operation. These features make the MICRF005 ideal for low power applications in both one-way and bi-directional wireless links.

All IF and post-detection (demodulator) data filtering is provided on the MICRF005, no external filters are required. Nominal filter bandwidth is fixed a 300kHz allowing a data throughput at rates up to 115kbps.

### Features

- 800MHz to 1000MHz frequency range
- Data rates up to 115kbps
- No filters or inductors required
- Low 10mA operating supply current at 868MHz
- Shutdown mode for >10:1 duty-cycle operation
- Very low RF antenna re-radiation
- CMOS logic interface for standard ICs
- Extremely low external part count
- Transmit standby mode for bi-directional link control

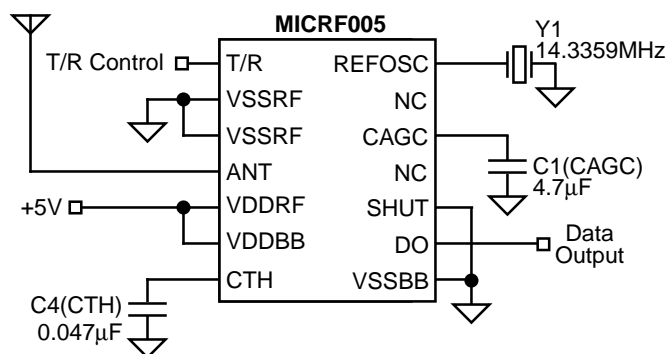
### Applications

- Wireless game controllers
- Security systems
- Medium-rate data modems

### Ordering Information

Part Number	Junction Temp. Range	Package
MICRF005BM	-40°C to +85°C	14-Lead SOIC

### Typical Application

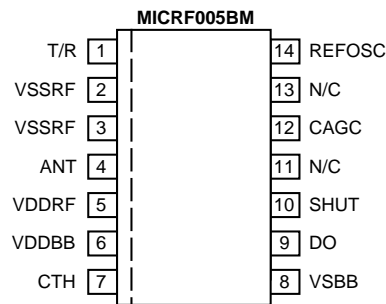


915MHz, 115kbps OOK ISM Band Receiver

QwikRadio is a trademark of Micrel Semiconductor.

The QwikRadio ICs were developed under a partnership agreement with AIT of Orlando, Florida.

## Pin Configuration



**Standard 14-Pin SOP (M) Package**

## Pin Description

Pin Number	Pin Name	Pin Function
1	T/R	Transmit/Receive control switch. Pull low to enable receiver function.
2, 3	VSSRF	This pin is the ground return for the RF section of the IC. The bypass capacitor connected from the VDDRF to VSSRF should have the shortest possible lead length. For best performance, connect VSSRF to VSSBB at the power supply only (i.e. keep VSSBB currents from flowing through VSSRF return paths).
4	ANT	This is the receive RF input, internally ac-coupled. Connect this pin to the receive antenna. For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSSRF to provide additional receive selectivity and input overload protection.
5	VDDRF	This pin is the positive supply input for the RF section of the IC. VDDBB and VDDRF should be connected together directly at the IC pins.
6	VDDBB	This pin is the positive supply input for the baseband section of the IC. VDDBB and VDDRF should be connected together at the IC pins.
7	CTH	This capacitor extracts the (DC) average value from the demodulated waveform which becomes the reference for the internal data slicing comparator. Treat as a low-pass RC filter with source impedance of nominally 30k $\Omega$ . A standard $\pm 20\%$ X7R ceramic capacitor is generally sufficient.
8	VSSBB	This is the ground return for the baseband section of the IC. The bypass and output capacitors connected to VSSBB should have the shortest possible leads lengths. For best performance, connect VSSRF to VSSBB at the power supply only (i.e., keep VSSBB currents from flowing through VSSRF return path).
9	DO	CMOS-level compatible data output signal.
10	SHUT	Shutdown-mode logic-level control input. Pull low to enable the receiver. This pin is internally pulled-up to VDDRF.
11	NC	No connection
12	CAGC	Integrating capacitor for on-chip AGC (Automatic Gain Control). The Decay/Attack time-constant (TC) ratio is nominally set as 10:1. Use of 0.47 $\mu$ F or greater is strongly recommended for best range performance. Use low-leakage type capacitors for duty-cycle operation (Dip Tantalum, Ceramic, Polyester).
13	NC	No connection
14	REFOSC	This is the timing reference for on-chip tuning and alignment. Connect crystal between this pin and VSSBB, or drive the input with an AC coupled 0.5V <sub>pp</sub> input clock.

**Absolute Maximum Ratings (Note 1)**

Supply Voltage ( $V_{DDRF}, V_{DDBB}$ )	+7V
Reference Oscillator Input Voltage ( $V_{REFOSC}$ )	$V_{DDBB}$
Input/Output Voltage ( $V_{I/O}$ )	$V_{SS}-0.3$ to $V_{DD}+0.3$
Junction Temperature ( $T_J$ )	+150°C
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Lead Temperature (soldering, 10 sec.)	+260°C
ESD Rating, <b>Note 3</b>	

**Operating Ratings (Note 2)**

Supply Voltage ( $V_{DDRF}, V_{DDBB}$ )	+4.75V to +5.5V
Ambient Temperature ( $T_A$ )	-40°C to +85°C

**Electrical Characteristics**

$V_{DDRF} = V_{DDBB} = V_{DD}$  where  $4.75V \leq V_{DD} \leq 5.5V$ ,  $V_{SS} = 0V$ ;  $V_{T/R} = V_{SHUT} = 0V$ ;  $C_{AGC} = 0.47\mu F$ ,  $C_{TH} = 4.7nF$ , 115kbps data-rate (Manchester encoded);  $f_{REFOSC} = 14.3359MHz$  ( $f_{RF} = 915MHz$ );  $T_A = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_A \leq +85^\circ C$ ; current flow into device pins is positive; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{OP}$	Operating Current	continuous operation		10	13.5 <b>18.5</b>	mA
		10:1 duty cycle		1		mA
$I_{STBY}$	Standby Current	$V_{T/R} = V_{SHUT} = V_{DD}$		11		$\mu A$

**RF Section, IF Section**

	Receiver Sensitivity	<b>Notes 4, 6</b>	<b>-81</b>	-84		dBm
$f_{IF}$	IF Center Frequency	<b>Note 7</b>		2.496		MHz
$f_{BW}$	IF 3dB Bandwidth	<b>Notes 7</b>		1.2		MHz
	Maximum Receive Data Rate		<b>115</b>			kb/s
$f_{ANT}$	RF Input Range		800		1000	MHz
	Receive Modulation Duty-Cycle		<b>20</b>		<b>80</b>	%
	Maximum Receiver Input	$R_S = 50\Omega$		-10		dBm
	Spurious Reverse Isolation	ANT pin, $R_{SC} = 50\Omega$ , <b>Note 5</b>		30		$\mu V_{rms}$
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$ , <b>Note 9</b>		0.1		
	AGC Leakage Current	$T_A = +85^\circ C$ , $V_{SHUT} = V_{DD}$ or $V_{T/R} = V_{DD}$ , <b>Note 9</b>		$\pm 200$		nA

**Reference Oscillator**

	Synthesizer Stabilization Time	to 1% of final value		1.2		ms
$Z_{REFOSC}$	Reference Oscillator Input Impedance			300		k $\Omega$
	OSC Input Voltage		300			mVp-p

**Demodulator**

$Z_{CTH}$	CTH Source Impedance	<b>Note 8, 9</b>		26		k $\Omega$
$\Delta Z_{CTH}$	CTH Source Impedance Variation	<b>Note 9</b>		$\pm 15$		%
	Demodulator Filter Bandwidth	<b>Notes 7</b>		300		kHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Digital/Control Section</b>						
$I_{IN(pu)}$	$V_{SHUT}$ Pull-Up Current	$V_{SHUT} = V_{SS}$		8.5		$\mu A$
$I_{IN(pd)}$	$V_{T/R}$ Pull-Down Current	$V_{T/R} = V_{DD}$		12		$\mu A$
$V_{IN(high)}$	$V_{T/R}, V_{SHUT}$ , Input-High Voltage		$V_{DD}-0.5$			V
$V_{IN(low)}$	$V_{T/R}, V_{SHUT}$ , Input-Low Voltage				0.5	V
$I_{OUT}$	Output Current	DO, push-pull		90		$\mu A$
$V_{OUT(high)}$	Output-High Voltage	DO, $I_{OUT} = -5\mu A$	$0.9V_{DD}$			V
$V_{OUT(low)}$	Output-Low Voltage	DO, $I_{OUT} = 5\mu A$			$0.1V_{DD}$	V
$t_R, t_F$	Output Rise and Fall Times	DO, $C_{LOAD} = 10pF$		tbd		$\mu s$

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended.

**Note 4:** Sensitivity is defined as the average signal level measured at the input necessary to achieve  $10^{-2}$  BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded data). The RF input is assumed to be matched into  $50\Omega$ .

**Note 5:** Spurious reverse isolation represents the spurious components which appear on the RF input pin (ANT) measured into  $50\Omega$  with an input RF matching network. Parameter guaranteed by device characterization, not production tested.

**Note 6:** Sensitivity, a commonly specified receiver parameter, provides an indication of the receiver's input referred noise, generally input thermal noise. However, it is possible for a more sensitive receiver to exhibit range performance no better than that of a less sensitive receiver if the background noise is appreciably higher than the thermal noise. Background noise refers to other interfering signals, such as FM radio stations, pagers, etc.

A better indicator of achievable receiver range performance is usually given by its selectivity, often stated as intermediate frequency (IF) or radio frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of "ether" noise. More selective receivers will almost invariably provide better range. Only when the receiver selectivity is so high that most of the noise on the receiver input is actually thermal will the receiver demonstrate sensitivity-limited performance.

**Note 7:** Parameter scales linearly with reference oscillator frequency  $f_T$ . For any reference oscillator frequency other than 14.3359MHz, compute new parameter value as the ratio:

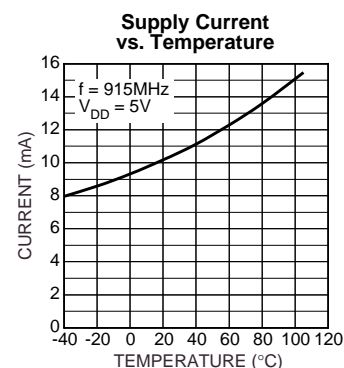
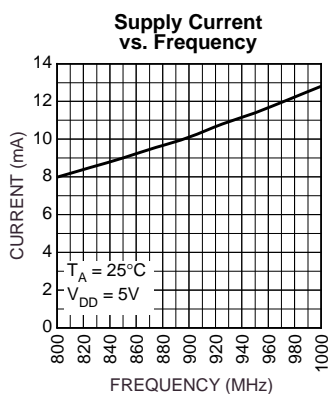
$$\frac{f_{REFOSC}MHz}{14.3359} \times (\text{parameter value at } 14.3359MHz)$$

**Note 8:** Parameter scales inversely with reference oscillator frequency  $f_T$ . For any reference oscillator frequency other than 14.3359MHz, compute new parameter value as the ratio:

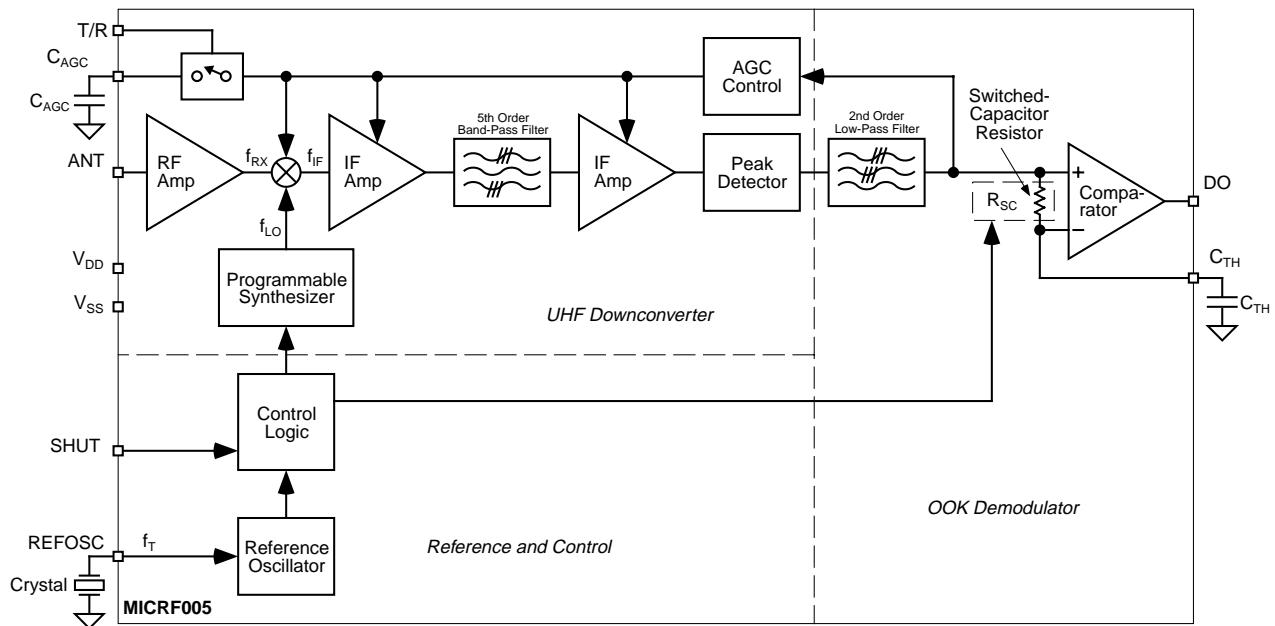
$$\frac{14.3359}{f_{REFOSC}MHz} \times (\text{parameter value at } 14.3359MHz)$$

**Note 9:** Parameter guaranteed by design (not tested).

## Typical Characteristics



## Functional Diagram



MICRF005 Block Diagram

## Functional Description

Refer to "MICRF005 Block Diagram". Identified in the block diagram are the three sections of the IC: UHF Downconverter, OOK Demodulator and Reference and Control. Also shown in the figure are two capacitors ( $C_{TH}$ ,  $C_{AGC}$ ) and one timing component (CR), usually a crystal. With the exception of a supply decoupling capacitor, these are the only external components needed by the MICRF005 to construct a complete UHF receiver. Two control inputs are shown in the block diagram: T/R and SHUT. Through these logic inputs, the user can control the operation of the IC. These inputs are CMOS compatible, and are pulled-up on the IC.

### IF Bandpass Filter

Rolloff response of the IF Filter is 7th order, while the demodulator data filter exhibits a 2nd order response.

### Slicing Level

Extraction of the dc value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor  $C_{TH}$  and the on-chip switched-capacitor "resistor"  $R_{SC}$ , shown in the block diagram. The effective resistance of  $R_{SC}$  is 30k $\Omega$ .

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typical values range from 5ms to 50ms. Optimization of the value of  $C_{TH}$  is required to maximize range.

### Squelch

During quiet periods (no signal) the data output (DO pin) transitions randomly with noise, presenting problems for some decoders. A simple solution is to introduce a small offset, or squelch voltage, on the  $C_{TH}$  pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be introduced by connecting a several-

M $\Omega$  resistor from the  $C_{TH}$  pin to either  $V_{SS}$  or  $V_{DD}$ , depending on the desired offset polarity. Since the MICRF005 has receiver AGC, noise at the internal comparator input is always the same, set by the AGC. The squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce range modestly. Only introduce an amount of offset sufficient to quiet the output.

### Automatic Gain Control

The signal path has AGC (automatic gain control) to increase input dynamic range. An external capacitor,  $C_{AGC}$ , must be connected to the  $C_{AGC}$  pin of the device. The ratio of decay-to-attack time-constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant). However, the attack time constant is set externally by choosing a value for  $C_{AGC}$ .

By adding resistance from the  $C_{AGC}$  pin to  $V_{DDBB}$  or  $V_{SSBB}$  in parallel with the AGC capacitor, the ratio of decay-to-attack time constant may be varied, although the value of such adjustments must be studied on a per-application basis. Generally the design value of 10:1 is adequate for the vast majority of applications.

To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under 10mVpp once the control voltage has attained its quiescent value. For this reason capacitor values of at least 0.47 $\mu$ F are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF005 in excess of 10:1. When the device is placed into shutdown mode (SHUT pin pulled high), the AGC capacitor floats, to retain the voltage. When operation is resumed, only the voltage droop on the capacitor due to leakage must be replenished, therefore a relatively low-leakage capacitor is recommended for

duty-cycled operation. The actual tolerable leakage will be application dependent. Clearly, leakage performance is less critical when the device off-time is low (milliseconds) and more critical when the off-time is high (seconds).

To further enhance duty-cycled operation of the IC, the AGC push and pull currents are increased for a fixed time immediately after the device is taken out of shutdown mode (turned-on). This compensates for AGC capacitor voltage droop while the IC is in shutdown mode, and therefore extends maximum achievable duty ratios. Push-pull currents are increased by 45 times their nominal values. The fixed time period is based on the reference oscillator frequency  $f_T$ , [ms] for  $f_T = 14.3359\text{MHz}$ , and varies inversely as  $f_T$  varies.

### Transmit / Standby Function

The transmit/receive function is controlled by the logic state of T/R. T/R is internally tied to  $V_{SS}$ . When T/R is open circuit or in the low state, the MICRF005 functions in its normal receive operating mode. The T/R pin may be pulled high to Vdd, this will place the receiver in a “stand-by” operating mode. This mode is intended for use during transmit cycles in transceiver applications where the receiver is co-located with a transmitter. In this “transmit” mode, the receiver oscillator remains active but the AGC function is disabled and the CAGC pin is high impedance to hold the AGC capacitor voltage. This function enables the MICRF005 to immediately resume receive operation after a transmit cycle.

### Shutdown Function

The shutdown function is controlled by a logic state applied to the SHUT pin. When  $V_{SHUT}$  is high, the device goes into low-power standby mode, consuming less than  $1\mu\text{A}$ . This pin is pulled high internally. It must be externally pulled low to enable the receiver.

### Reference Oscillator

All timing and tuning operations on the MICRF005 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of two ways:

1. Connect a crystal
2. Drive this pin with an external timing signal

The second approach is attractive for lowering system cost further if an accurate reference signal exists elsewhere in the system, for example, a reference clock from a crystal-controlled microprocessor. An externally applied signal should be ac-coupled and resistively-attenuated, or otherwise limited, to approximately  $0.5\text{Vpp}$ . The specific reference frequency required is related to the system transmit frequency.

### I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF005 are diagrammed in Figures 1 through 6. The ESD protection diodes at all input and output pins are not shown. Integrated into an actual design application with the best results possible.

### CTH Pin

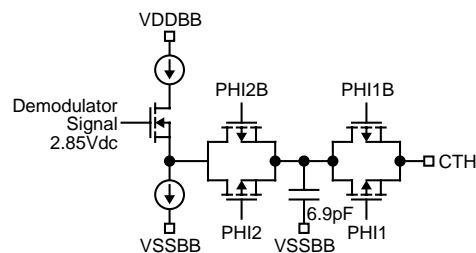


Figure 2.  $C_{TH}$  Pin

Figure 2 illustrates the CTH-pin interface circuit. The CTH pin is driven from a P-channel MOSFET source-follower with approximately  $10\mu\text{A}$  of bias. Transmission gates TG1 and TG2 isolate the  $6.9\text{pF}$  capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a “resistance” of approximately  $100\text{k}\Omega$ . The dc potential at the CTH pin is approximately  $1.6\text{V}$ .

### CAGC Pin

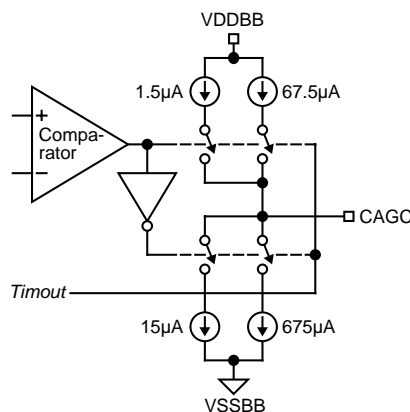
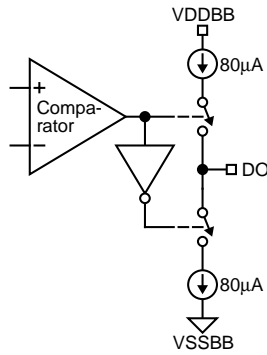


Figure 3.  $C_{AGC}$  Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor  $C_{AGC}$ . The attack current is nominally  $15\mu\text{A}$ , while the decay current is a  $1/10$ th scaling of this, nominally  $1.5\mu\text{A}$ , making the attack/decay timeconstant ratio a fixed  $10:1$ . Signal gain of the RF/IF strip inside the IC diminishes as the voltage at CAGC decreases. Modification of the attack/decay ratio is possible by adding resistance from the CAGC pin to either  $V_{DDBB}$  or  $V_{SSBB}$ , as desired.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across  $C_{AGC}$ , and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 45 times for approximately  $10\text{ms}$  after release of the SHUT pin. This allows rapid recovery of any voltage droop on  $C_{AGC}$  while in shutdown.

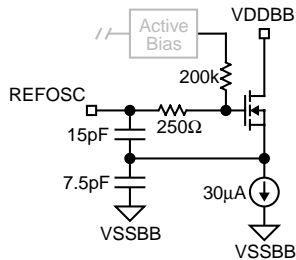
**DO Pin**



**Figure 4. DO Pin**

The output stage for DO (digital output) is shown in Figure 4. The output is a 90µA push and 90µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high-capacitance loads.

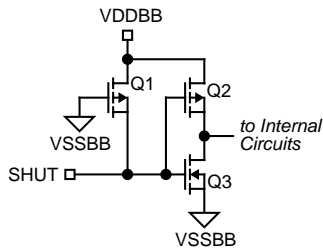
**REFOSC Pin**



**Figure 5. REFOSC Pin**

The REFOSC input circuit is shown in Figure 5. Input impedance is high (300kΩ). This is a Colpitts oscillator with internal capacitors. The nominal dc bias voltage on this pin is 1.4V.

**SHUT Pin**

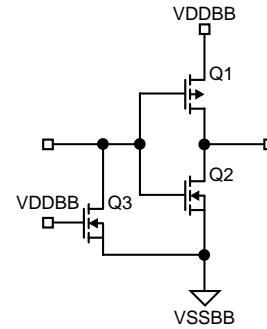


**Figure 6. SHUT Pin**

Control input circuitry is shown in Figures 6. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-channel MOSFET Q1 is a large channel length device which functions essentially as a “weak”

pullup to  $V_{DDBB}$ . Typical pullup current is 8.5µA, leading to an impedance to the  $V_{DDBB}$  supply of typically 1MΩ.

**T/R Pin**



**Figure 7. T/R Pin**

The transmit/receive function is controlled by the logic state of T/R. T/R is internally tied to  $V_{SS}$ . When T/R is open circuit or in the low state, the MICRF005 functions in its normal receive operating mode. The T/R pin may be pulled high to Vdd, this will place the receiver in a “stand-by” operating mode. This mode is intended for use during transmit cycles in transceiver applications where the receiver is co-located with a transmitter. In this “transmit” mode, the receiver oscillator remains active but the AGC function is disabled and the  $C_{AGC}$  pin is tri-stated to hold the AGC capacitor voltage. This function enables the MICRF005 to quickly resume receive operation after a transmit cycle.

## Application Information

### Bypass and Output Capacitors

The bypass and output capacitors connected to  $V_{SSBB}$  should have the shortest possible lead lengths. For best performance, connect  $V_{SSRF}$  to  $V_{SSBB}$  at the power supply only (that is, keep  $V_{SSBB}$  currents from flowing through the  $V_{SSRF}$  return path).  $V_{DDRF}$  and  $V_{DDBB}$  should be connected directly together at the IC pins. A  $10\Omega$  resistor in series with the supply line plus three decoupling capacitors is recommended. The suggested capacitor values are 1nF, 10nF and 100nF.

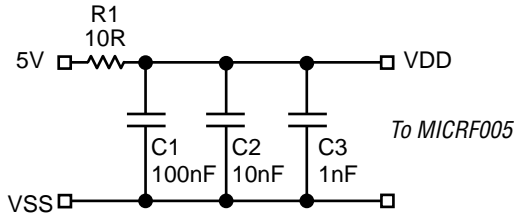


Figure 8. Supply Bypassing

### External Timing Signals

Externally applied signals should be ac-coupled and the amplitude must be limited to approximately 0.5Vpp.

### Optional BandPass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and  $V_{SSRF}$  to provide additional receive selectivity and input overload protection.

### Frequency and Capacitor Selection

Selection of the reference oscillator frequency  $f_T$ , slicing level capacitor ( $C_{TH}$ ), and AGC capacitor ( $C_{AGC}$ ) are briefly summarized in this section.

#### Selecting Reference Oscillator Frequency $f_T$

As with any superheterodyne receiver, the difference between the internal LO (local oscillator) frequency  $f_{LO}$  and the incoming transmit frequency  $f_{TX}$  ideally must equal the IF center frequency. Equation 1 may be used to compute the appropriate  $f_{LO}$  for a given  $f_{TX}$ :

$$(1) \quad f_{LO} = f_{TX} \pm \left( 2.496 \frac{f_{TX}}{915} \right)$$

Frequencies  $f_{TX}$  and  $f_{LO}$  are in MHz. Note that two values of  $f_{LO}$  exist for any given  $f_{TX}$ , distinguished as “high-side mixing” and “low-side mixing,” and there is generally no preference of one over the other.

After choosing one of the two acceptable values of  $f_{LO}$ , use Equation 2 to compute the reference oscillator frequency  $f_T$ :

$$(2) \quad f_T = \frac{f_{LO}}{64}$$

Equations (1) and (2) can be simplified to:

$$f_T = 63.8258 f_{TX}$$

Frequency  $f_T$  is in MHz. Connect a series-mode crystal of frequency  $f_T$  to REFOSC on the MICRF005. Four-decimal-

place accuracy on the frequency is generally adequate. The following table identifies  $f_T$  for some common transmit frequencies when the MICRF005 is operated.

Transmit Frequency ( $f_{TX}$ )	Reference Oscillator Frequency ( $f_T$ )
868.35MHz	13.6050MHz
915MHz	14.3359MHz
916.5MHz	14.3594MHz

Table 2. Common Transmitter Frequencies

#### Selecting Capacitor $C_{TH}$

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure (that is, existence of data preamble, etc.). This issue is covered in more detail in “Application Note 22.”

Source impedance of the  $C_{TH}$  pin is given by equation (3), where  $f_T$  is in MHz:

$$(3) \quad R_{SC} = 30\Omega \frac{14.3359}{f_T}$$

Assuming that a slicing level time constant  $\tau$  has been established, capacitor  $C_{TH}$  may be computed using equation (4).

$$(4) \quad C_{TH} = \frac{\tau}{R_{SC}}$$

A standard  $\pm 20\%$  X7R ceramic capacitor is generally sufficient.

#### Selecting $C_{AGC}$ Capacitor in Continuous Mode

Selection of  $C_{AGC}$  is dictated by minimizing the ripple on the AGC control voltage by using a sufficiently large capacitor. Factory experience suggests that  $C_{AGC}$  should be in the vicinity of 0.47 $\mu$ F to 4.7 $\mu$ F. Large capacitor values should be carefully considered as this determines the time required for the AGC control voltage to settle from a completely discharged condition. AGC settling time from a completely discharged (zero-volt) state is given approximately by equation (5):

$$(5) \quad \Delta t = 1.333 C_{AGC} - 0.44$$

where:

$C_{AGC}$  is in  $\mu$ F, and  $\Delta t$  is in seconds.

#### Selecting $C_{AGC}$ Capacitor in Duty-Cycle Mode

Generally, droop of the AGC control voltage during shutdown should be replenished as quickly as possible after the IC is “turned-on”. As described in the functional description, for about [tbd]ms after the IC is turned on, the AGC push-pull currents are increased to 45 times their normal values. Consideration should be given to selecting a value for  $C_{AGC}$  and a shutdown time period such that the droop can be replenished within this [tbd]ms period.



Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. Worst-case from a recovery standpoint is downward droop, since the AGC pullup current is 1/10th magnitude of the pulldown current. The downward droop is replenished according to the Equation (6):

$$(6) \quad \frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t}$$

where:

$I$  = AGC pullup current for the initial [tbd]ms (67.5 $\mu$ A)

$C_{AGC}$  = AGC capacitor value

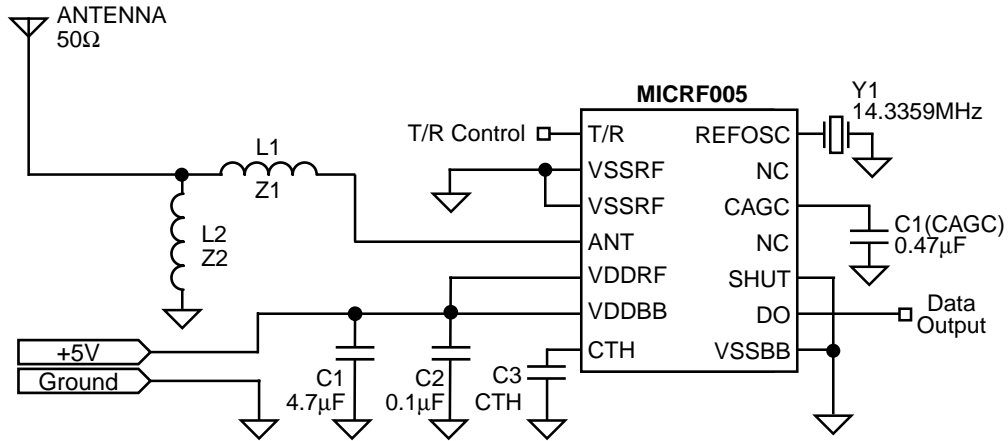
$\Delta t$  = droop recovery time

$\Delta V$  = droop voltage

For example, if user desires  $\Delta t = 10$ ms and chooses a 4.7 $\mu$ F  $C_{AGC}$ , then the allowable droop is about 144mV. Using the same equation with 200nA worst case pin leakage and assuming 1 $\mu$ A of capacitor leakage in the same direction, the maximum allowable  $\Delta t$  (shutdown time) is about 0.56s for droop recovery in 10ms.

### Typical Applications

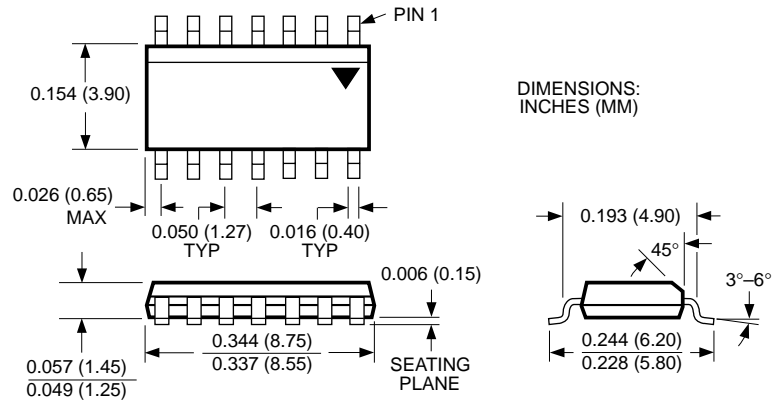
Figure 9 below illustrates a typical application for the MICRF005 UHF receiver IC. Operation in this example is at 916.5MHz



### Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
U1	MICRF005	Micrel	UHF Receiver	1
C1, C4		Panasonic	4.7μF Ceramic Cap	1
C2		Panasonic	0.47μF Ceramic Cap	1
C3		Panasonic	0.1μF Ceramic Cap	1
L1, L2		Coilcraft	[tbd]nH, Wire wound SMT inductors	1
Y1			13.3594MHz crystal	1

**Package Information**



**14-Lead SOIC (M)**

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