

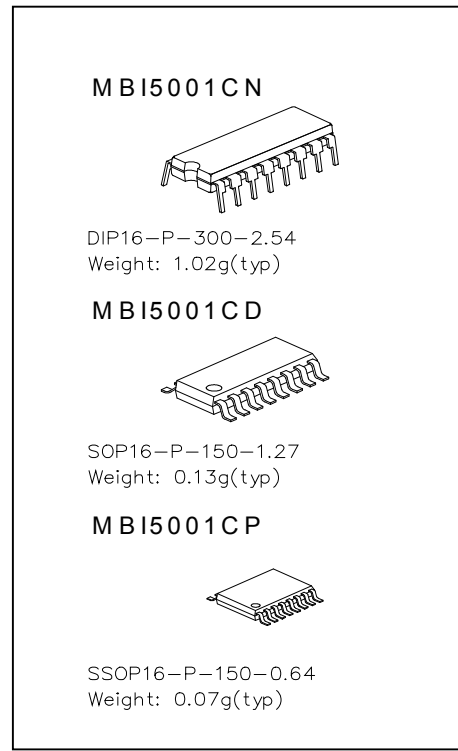


Features

- 8 constant-current output channels
- Output current adjustable through an external resistor
- Serial data in/parallel data out
- Output current: 5-90 mA
- 20 MHz clock frequency

Product Description

MBI5001, utilizing the most advanced Si technology, is targeted for LED panel display. MBI5001 contains CMOS shift registers and latch functions converting serial input data into parallel output format. At the output stage, eight regulated current sources were designed to provide 5-90 mA constant current for driving LEDs.

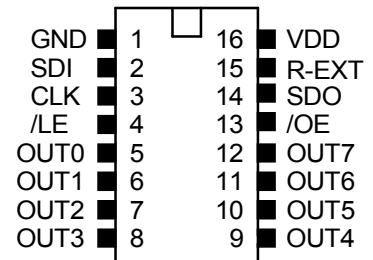


MBI5001 provides users with great flexibility and device performance while using the MBI5001 in their LED panel system design. Users may adjust the output current of the MBI5001 through an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. MBI5001 guarantees to endure maximum 17V at the output port, allowing users to connect more LEDs in series. The high clock frequency, 20 MHz, also satisfies the system requirement of high volume data transmission.

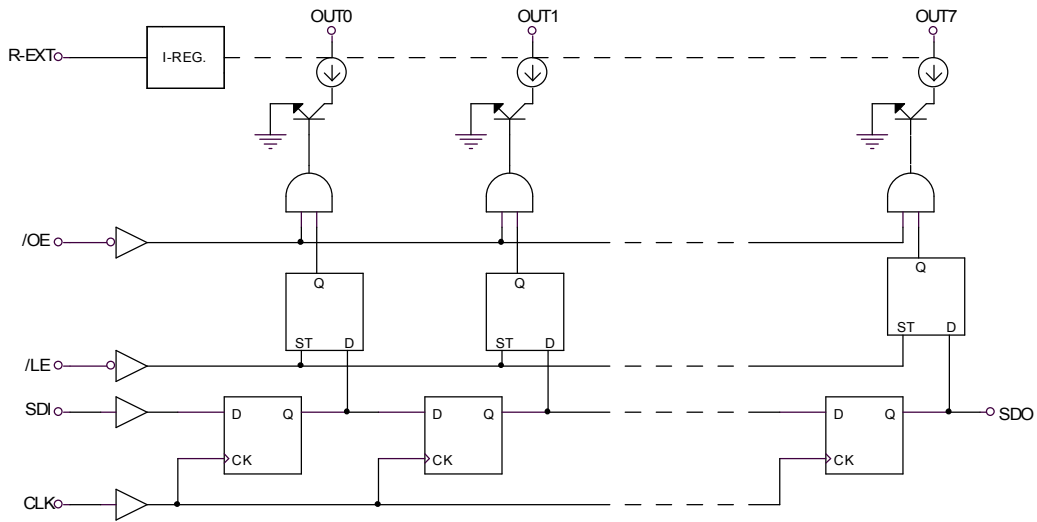
Terminal Description

PIN NO.	PIN NAME	FUNCTION
1	GND	GND terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	/LE	Latch input terminal
5-12	OUT0-7	Output terminal
13	/OE	Output enable input terminal
14	SDO	Serial data out terminal
15	R-EXT	Constant current programming
16	VDD	5V supply voltage terminal

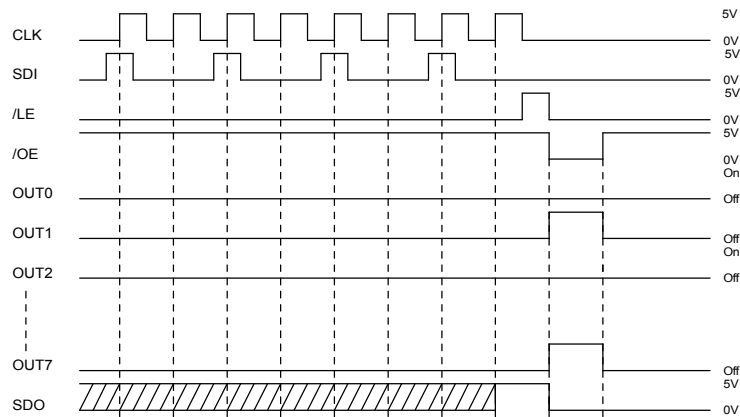
Pin Description



Block Diagram



Timing Diagram

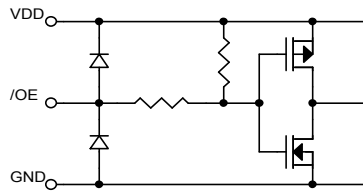


Truth table

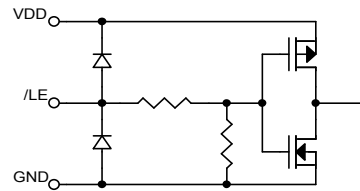
CLK	/LE	/OE	SDI	OUT0	OUT5	OUT7	SDO
UP	H	L	D_n	D_n	D_{n-5}	D_{n-7}	D_{n-7}
UP	L	L	D_{n+1}	NO CHANGE			D_{n-6}
UP	H	L	D_{n+2}	D_{n+2}	D_{n+3}	D_{n+5}	D_{n-5}
DOWN	X	L	D_{n+3}	D_{n+2}	D_{n+3}	D_{n+5}	D_{n-5}
DOWN	X	H	D_{n+3}	Off			D_{n-5}

Equivalent Circuit of Inputs and Outputs:

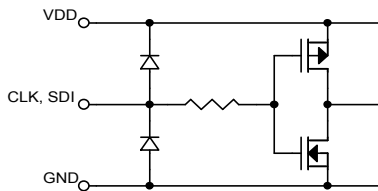
1. /OE terminal



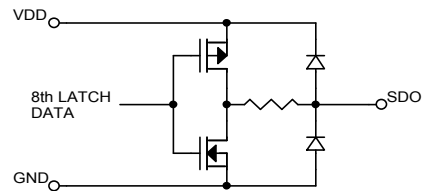
2. /LE terminal



3. CLK, SDI terminal



4. SDO terminal



Maximum Ratings

CHARACTER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~+7.0	V
Output Voltage	V_{CE}	-0.5~+17.0	V
Output Current	I_{OUT}	+90	mA
Input Voltage	V_{IN}	-0.4~ V_{DD} +0.4	V
GND Terminal Current	I_{GND}	720	mA
Clock Frequency	F_{CLK}	20	MHZ
Power Dissipation (ON PCB, $T_a=25^{\circ}C$)	CN – type	P_D	W
	CD – type		
	CP – type		
Thermal Resistance (ON PCB, $T_a=25^{\circ}C$)	CN – type	$R_{th(j-a)}$	$^{\circ}C/W$
	CD – type		
	CP – type		
Operating Temperature	T_{opr}	-40~+85	$^{\circ}C$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}C$

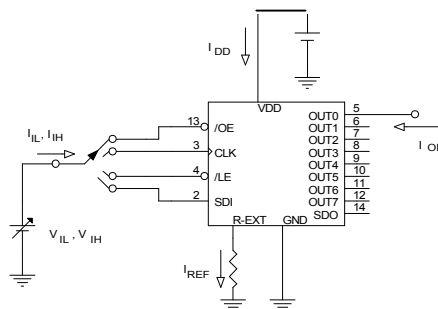
Recommended Operating Condition

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Output Voltage		V_{CE}	-	-	-	17.0	V
Output Current		I_{OUT}	DC Test Circuit	5	-	90	mA
		I_{OH}	SERIAL-OUT	-	-	-1.0	mA
		I_{OL}	SERIAL-OUT	-	-	1.0	mA
Input Voltage		V_{IH}	-	$0.7V_{DD}$	-	$V_{DD}+0.3$	V
		V_{IL}	-	-0.3	-	$0.3V_{DD}$	V
/LE Pulse Width		t_w LAT	$V_{DD}=4.5\sim 5.5V$	25	-	-	ns
CLK Pulse Width		t_w CLK		25	-	-	ns
/OE Pulse Width		t_w EN		400	-	-	ns
Setup Time for DATA		$t_{setup}(D)$		20	-	-	ns
Hold Time for DATA		$t_{hold}(D)$		15	-	-	ns
Setup Time for LATCH		$t_{setup}(L)$		20	-	-	ns
Hold Time for ENABLE		$t_{hold}(E)$		60	-	-	ns
Clock Frequency		F_{CLK}		Cascade Operation	-	-	20.0
Power Dissipation	CN – type	P_D	$T_a=85^{\circ}C$	-	-	0.85	W
	CD – type					0.55	
	CP – type					0.46	

Electrical Characteristics

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Input Voltage	“H” level	V_{IH}	-	$0.7V_{DD}$	V_{DD}	V	
	“L” level	V_{IL}	-	GND	$0.3V_{DD}$		
Output Leakage Current	I_{OH}	$V_{OH}=17.0V$	-	-	10	μA	
Output Voltage	SERIAL-OUT	V_{OL}	$I_{OL}=+1.0mA$	-	-	0.4	V
		V_{OH}	$I_{OH}=-1.0mA$	-	-	-	V
Output Current 1	I_{OL1}	$V_{CE}=0.8V$	$R_{ext}=865\ \Omega$ (include Skew)	-	40.0	-	mA
Current Skew	dI_{OL1}	$I_O = 40mA$ $V_{CE} = 0.8V$	$R_{ext}=865\ \Omega$	-	± 1.5	± 6.0	%
Output Current 2	I_{OL2}	$V_{CE}=1.2V$	$R_{ext}=330\ \Omega$ (include Skew)	-	80.0	-	mA
Current Skew	dI_{OL2}	$I_O = 80mA$ $V_{CE} = 1.2V$	$R_{ext}=330\ \Omega$	-	± 1.5	± 6.0	%
Pull-up Resistor	$R_{IN(up)}$	-	-	150	300	600	K Ω
Pull-down Resistor	$R_{IN(down)}$	-	-	85	200	400	K Ω
Supply Current	“OFF”	$I_{DD(off) 1}$	$R_{ext} = OPEN$ $\overline{OUT0\sim 7} = Off$	-	0.1	1.0	mA
		$I_{DD(off) 2}$	$R_{ext} = 865\ \Omega$ $\overline{OUT0\sim 7} = Off$	0.1	0.2	1.0	
		$I_{DD(off) 3}$	$R_{ext} = 330\ \Omega$ $\overline{OUT0\sim 7} = Off$	0.1	0.2	1.0	
	“ON”	$I_{DD(on) 1}$	$R_{ext} = 865\ \Omega$ $\overline{OUT0\sim 7} = On$	7.0	12.0	18.0	
		$I_{DD(on) 2}$	$R_{ext} = 330\ \Omega$ $\overline{OUT0\sim 7} = On$	10.0	22.0	32.0	

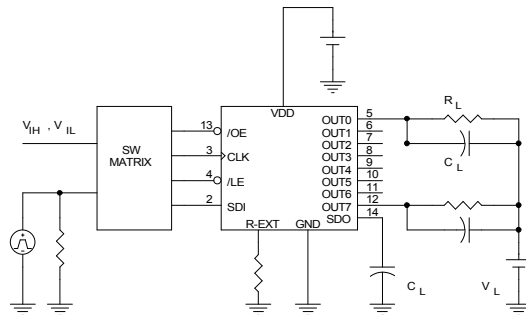
Test Circuit for Electrical Characteristics



Switching Characteristics

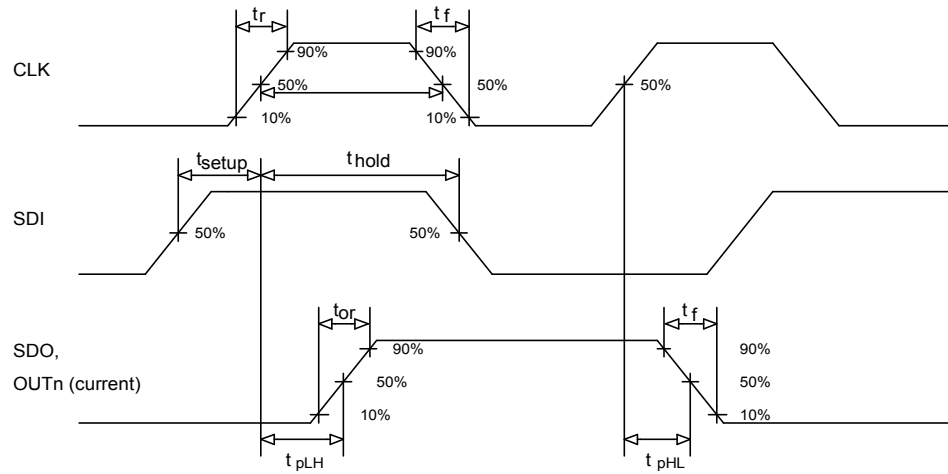
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	INn-OUTn	tpLH	$V_{DD}=5.0V$ $V_{CE}=0.8V$ $V_{IH}=V_{DD}$ $V_{IL}=GND$ $R_{ext}=865\ \Omega$ $I_{OUT}=40mA$ $V_L=3.4V$ $R_L=65\ \Omega$ $C_L=10.5pF$	-	200	300	ns
	/LE-OUTn			-	200	300	ns
	/OE-OUTn			-	200	300	ns
	CLK-SOUT			20	50	70	ns
Propagation Delay Time ("H" to "L")	INn-OUTn	tpHL		-	200	300	ns
	/LE-OUTn			-	200	300	ns
	/OE-OUTn			-	200	300	ns
	CLK-SOUT			20	50	70	ns
Pulse Width	CLK	tw CLK-CLK		15	-	20	ns
	/LE	tw LAT-LAT		20	-	30	ns
Set-up Time for LATCH	tswtup LAT	Set-up Time for LATCH	10	-	20	ns	
Hold Time for ENABLE	thold LAT	Hold Time for ENABLE	10	-	25	ns	
Maximum CLK Rise Time	tr	Maximum CLK Rise Time	-	-	5	ns	
Maximum CLK Fall Time	tf	Maximum CLK Fall Time	-	-	5	ns	
Output Rise Time	tor	Output Rise Time	-	150	200	ns	
Output Fall Time	tof	Output Fall Time	-	150	200	ns	

Test Circuit for Switching Characteristics

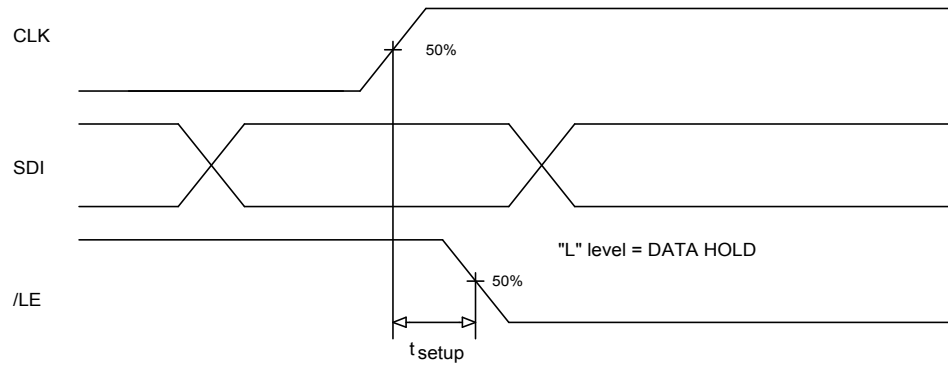


Timing Wave Form

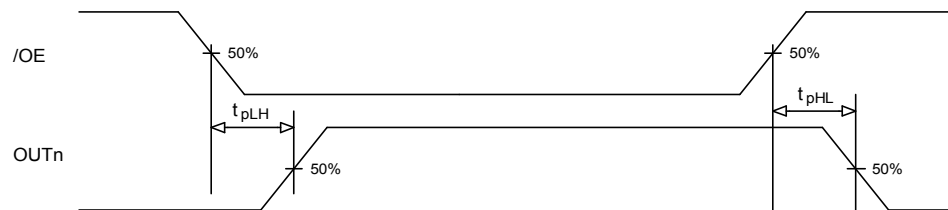
1. CLK, SDI, SDO, OUTn



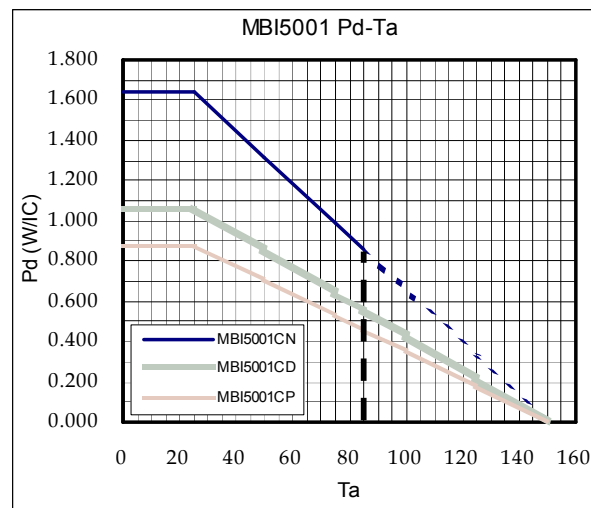
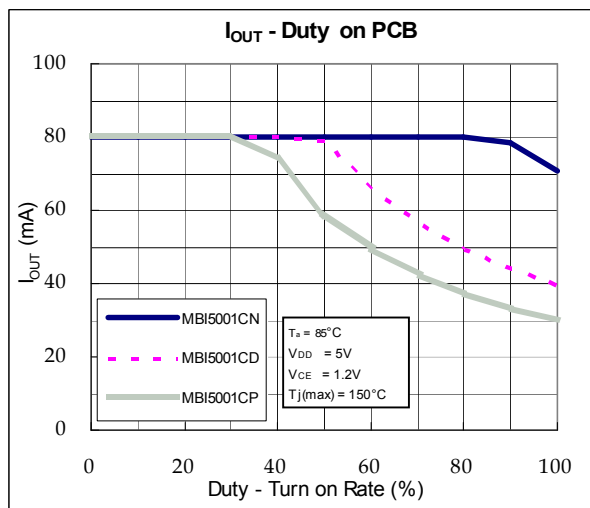
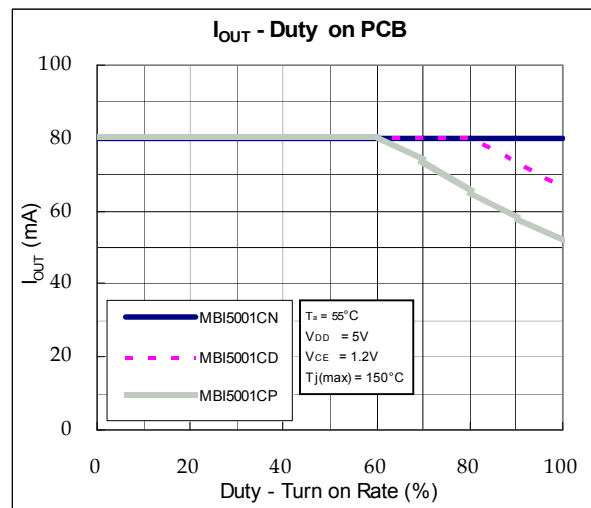
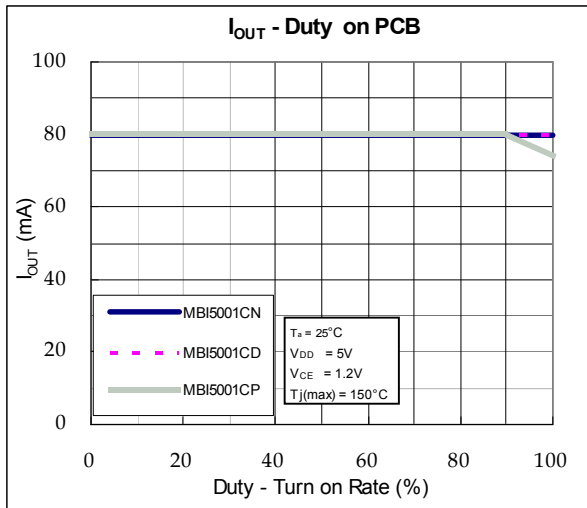
2. CLK - /LE



3. /OE - OUTn

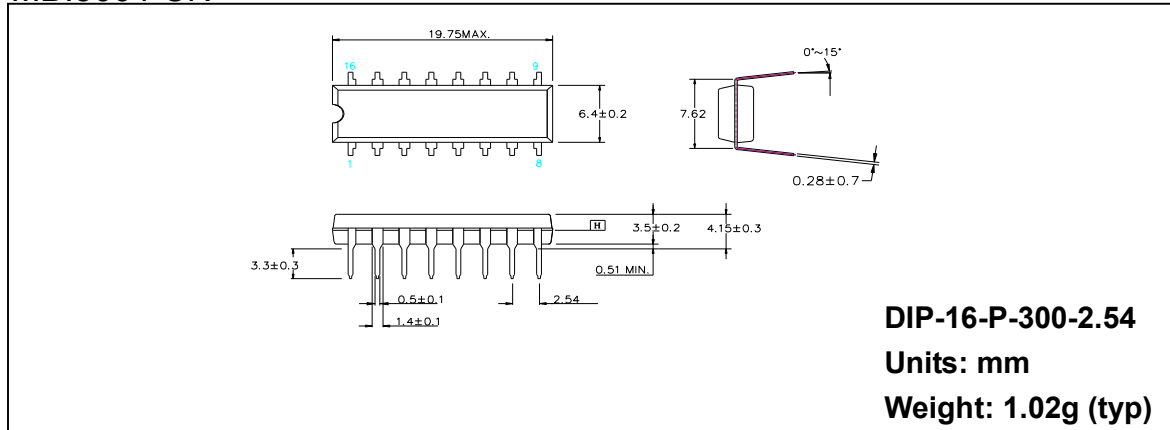


Graphs

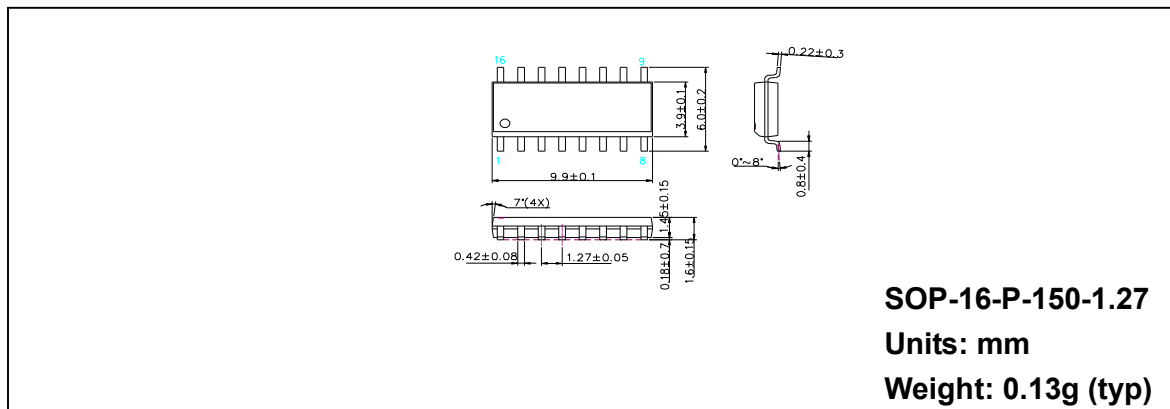


Outline Drawings

MBI5001 CN



MBI5001 CD



MBI5001 CP

