

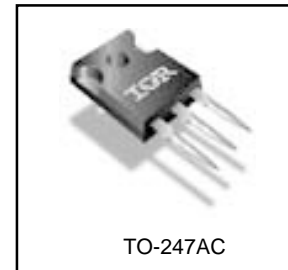
Applications

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

V_{DSS}	R_{DS(on)} typ.	I_D
600V	180mΩ	27A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dv/dt Capability



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	27	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	18	
I _{DM}	Pulsed Drain Current ①	110	
P _D @ T _C = 25°C	Power Dissipation	500	W
	Linear Derating Factor	4.0	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T _{STG}			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	530	mJ
I _{AR}	Avalanche Current①	—	27	A
E _{AR}	Repetitive Avalanche Energy①	—	50	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.29	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.24	—	
R _{θJA}	Junction-to-Ambient	—	40	

IRFP27N60K

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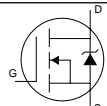
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.64	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	180	220	mΩ	$V_{GS} = 10V, I_D = 16A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 50V, I_D = 16A$
Q_g	Total Gate Charge	—	—	180	nC	$I_D = 27A$
Q_{gs}	Gate-to-Source Charge	—	—	56		$V_{DS} = 480V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	86		$V_{GS} = 10V, \text{See Fig. 6 and 13}$ ④
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	110	—		$I_D = 27A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		$R_G = 4.3\Omega$
t_f	Fall Time	—	38	—		$V_{GS} = 10V, \text{See Fig. 10}$ ④
C_{iss}	Input Capacitance	—	4660	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	460	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	41	—		$f = 1.0MHz, \text{See Fig. 5}$
C_{oss}	Output Capacitance	—	5490	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	120	—		$V_{GS} = 0V, V_{DS} = 480V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	250	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	27	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 27A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	620	920	ns	$T_J = 25^\circ\text{C}, I_F = 27A$
Q_{rr}	Reverse Recovery Charge	—	11	16	μC	$di/dt = 100A/\mu s$ ④
I_{RRM}	Reverse Recovery Current	—	36	53	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.4mH$, $R_G = 25\Omega$, $I_{AS} = 27A$, $dv/dt = 13V/ns$. (See Figure 12a)
- ③ $I_{SD} \leq 27A$, $di/dt \leq 390A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

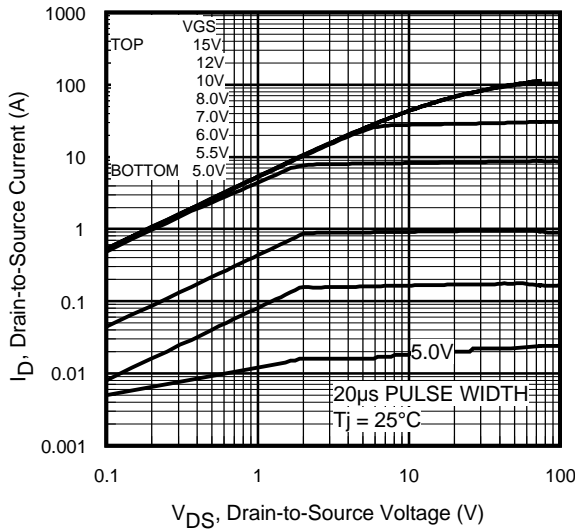


Fig 1. Typical Output Characteristics

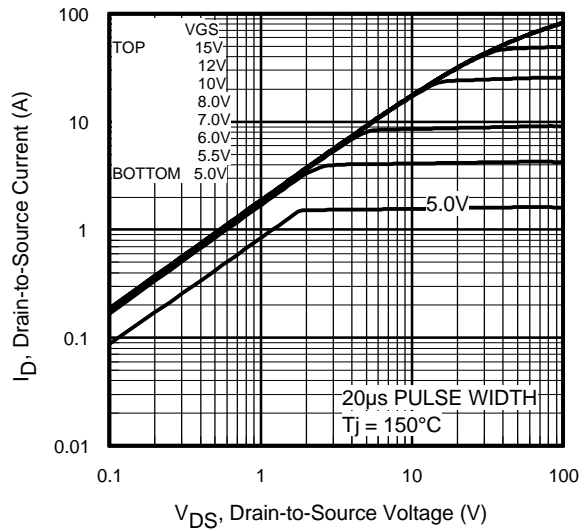


Fig 2. Typical Output Characteristics

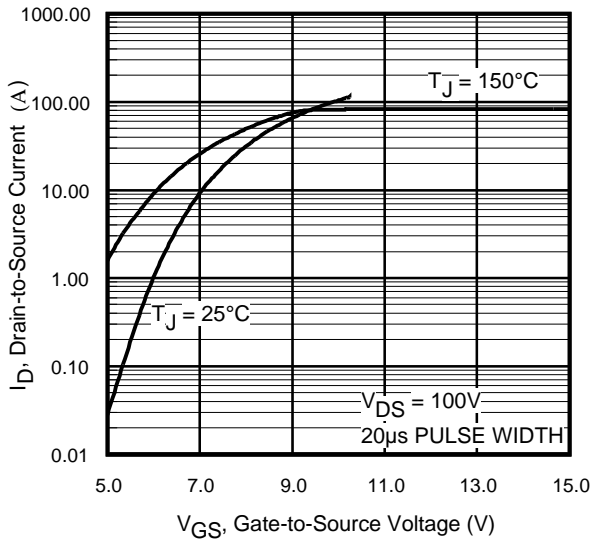


Fig 3. Typical Transfer Characteristics

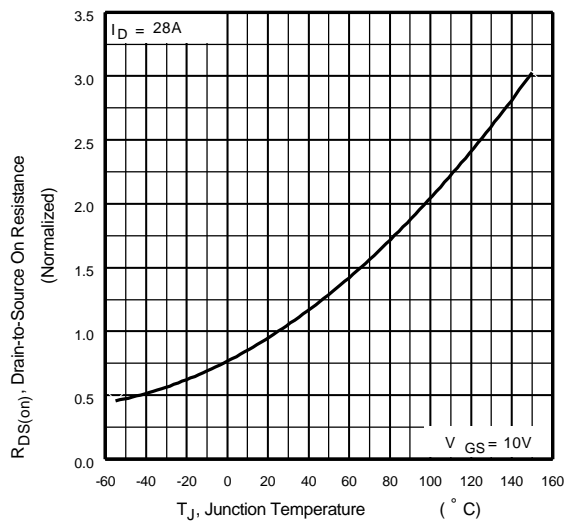


Fig 4. Normalized On-Resistance Vs. Temperature

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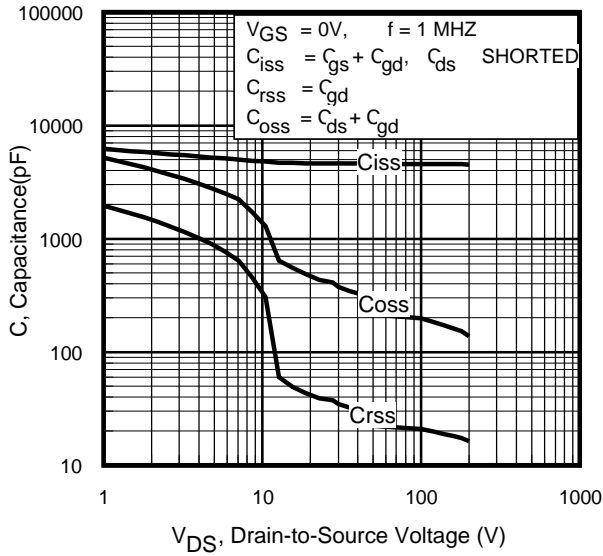


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

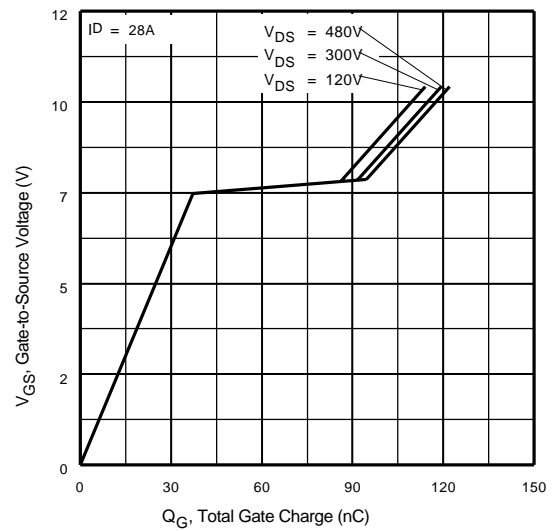


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

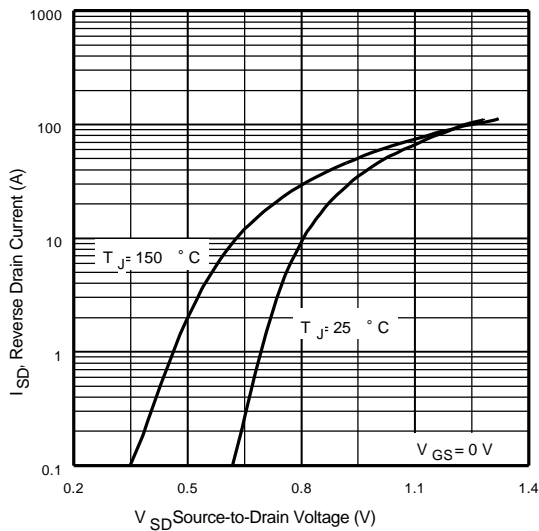


Fig 7. Typical Source-Drain Diode Forward Voltage

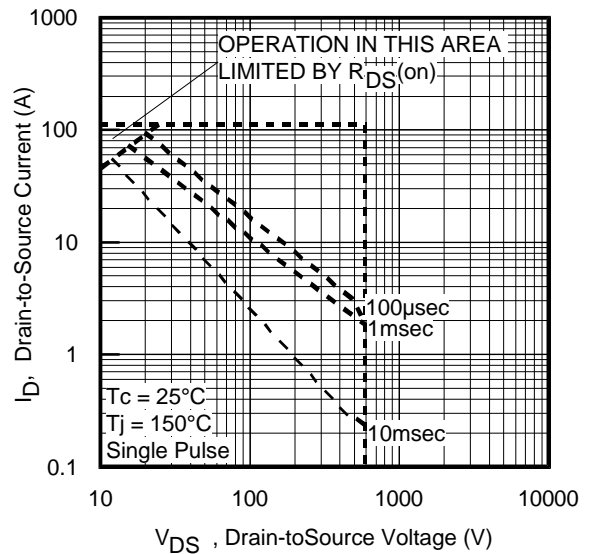


Fig 8. Maximum Safe Operating Area

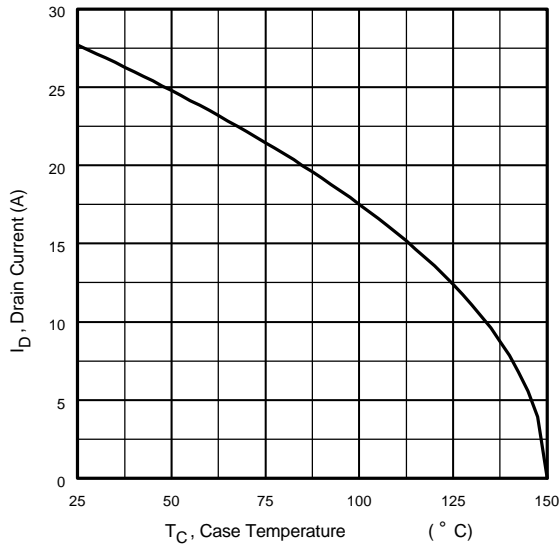


Fig 9. Maximum Drain Current Vs. Case Temperature

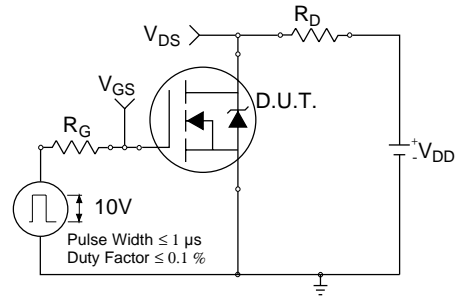


Fig 10a. Switching Time Test Circuit

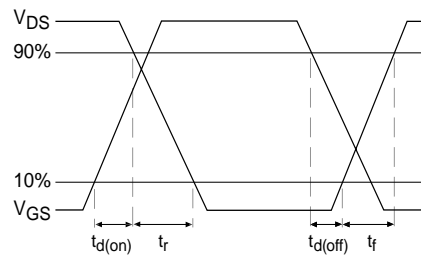


Fig 10b. Switching Time Waveforms

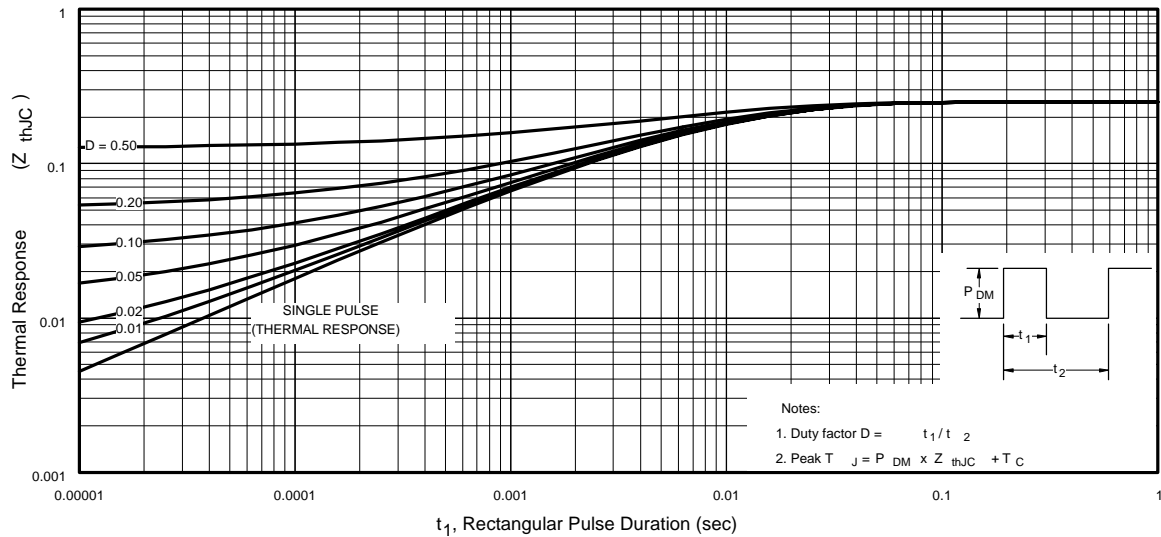


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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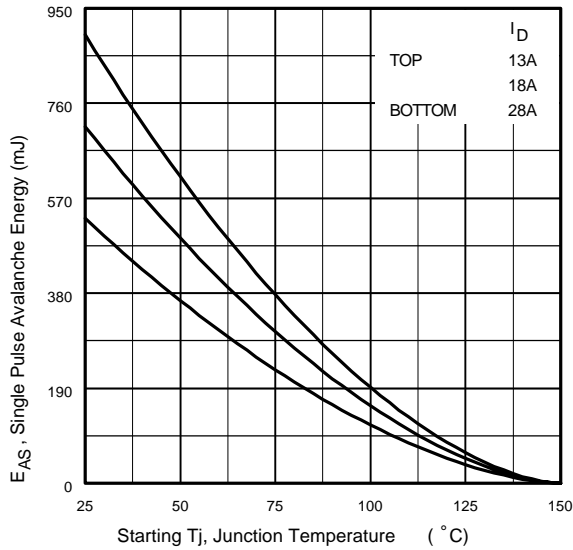


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

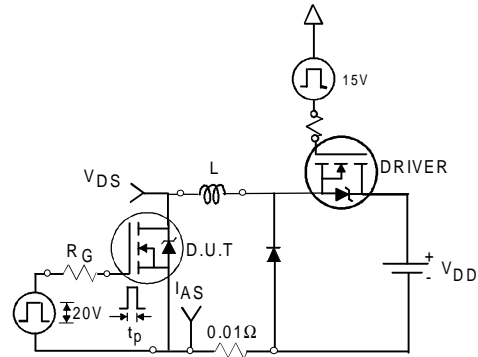


Fig 12c. Unclamped Inductive Test Circuit

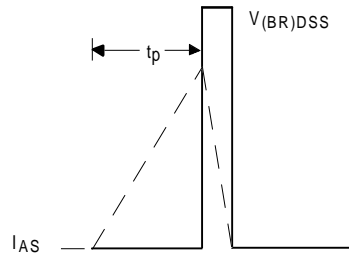


Fig 12d. Unclamped Inductive Waveforms

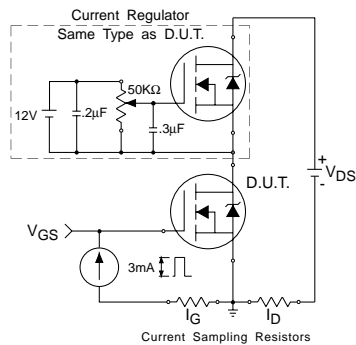


Fig 13a. Gate Charge Test Circuit

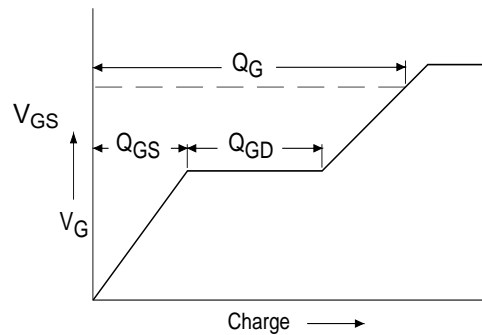
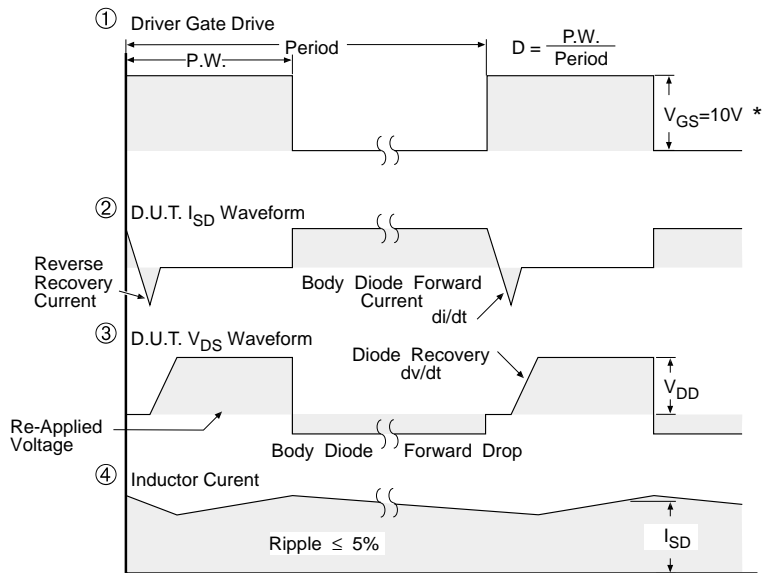
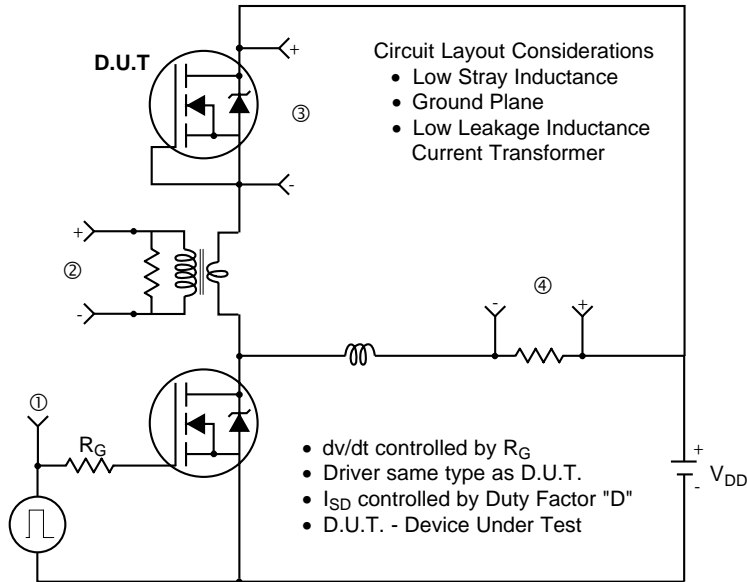


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

