OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

September 26, 2001 FN7034

200MHz Unity-Gain Stable Operational Amplifier

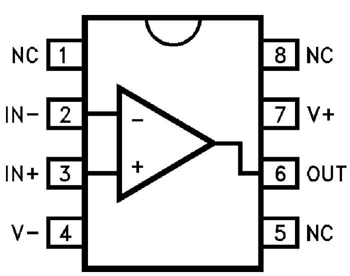
élantec

The EL2073 is a precision voltage-feedback amplifier featuring a 200MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50mA output current drive over temperature.

The EL2073 is unity-gain stable with a -3dB bandwidth of 400MHz. It has a very low 200µV of input offset voltage, only 2µA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2073 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2073 the ideal choice for all op-amp applications requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2073 an ideal amplifier for signal-processing and digitizing systems.

Pinout

EL2073
(8-PIN PDIP, SO)
TOP VIEW



Features

- 200MHz gain-bandwidth product
- Unity-gain stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200µV
- Low bias current = 2µA
- Low offset current = 0.1µA
- Output current = 50mA over temperature
- Fast settling = 13ns to 0.1%
- Low distortion = -60dB HD2, -70dB HD3 @ 20MHz, $2V_{PP}$, $A_V = +1$

Applications

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2073CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2073CS	-40°C to +85°C	8-Pin SO	MDP0027

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright © Intersil Americas Inc. 2003. All Rights Reserved. Elantec is a registered trademark of Elantec Semiconductor, Inc.
All other trademarks mentioned are the property of their respective owners.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S) . . . .±7V
Output Current
Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70mA.

Common-Mode Input . . . . ±V_S
Differential Input Voltage 5V

Thermal Resistance. . . . .θ_{JA} = 95°C/W PDIP
. . . . θ_{JA} = 175°C/W SO-8
Operating Temperature . . . .-40°C to +85°C
Junction Temperature . . . . 175°C
Storage Temperature . . . .-60°C to +150°C
Note: See EL2071/EL2171 for Thermal Impedance curves.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω, unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1.5	mV
			T_{MIN}, T_{MAX}			3	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		µV/°C
I_B	Input Bias Current		25°C		2	6	µA
			T_{MIN}, T_{MAX}		2	6	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	µA
			T_{MIN}, T_{MAX}			2	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	25°C	60	80		dB
			T_{MIN}, T_{MAX}	60			dB
CMRR	Common Mode Rejection Ratio	(Note 3)	25°C	65	90		dB
			T_{MIN}, T_{MAX}	65			dB
I_S	Supply Current—Quiescent	No Load	25°C		21	25	mA
			T_{MIN}, T_{MAX}			25	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		pF
R_{OUT}	Output Resistance		25°C		20		mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		V
			T_{MIN}, T_{MAX}	±2.5			V
I_{OUT}	Output Current		25°C	50	70		mA
			T_{MIN}, T_{MAX}	50			mA
V_{OUT}	Output Voltage Swing	No Load	25°C	±3.5	±4		V
			T_{MIN}, T_{MAX}	±3.5			V
V_{OUT} 100	Output Voltage Swing	100Ω	25°C	±3	±3.6		V
			T_{MIN}, T_{MAX}	±3			V
V_{OUT} 50	Output Voltage Swing	50Ω	25°C	±3	±3.4		V
			T_{MIN}, T_{MAX}	±2.5			
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	500	1000		V/V
			T_{MIN}, T_{MAX}	400			V/V

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω, unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	400	800		V/V
			T_{MIN}, T_{MAX}	300			V/V
eN@ > 1MHz	Noise Voltage 1–100MHz		25°C		2.3		nV/√Hz
iN@ > 100kHz	Noise Current 100k–100MHz		25°C		3.2		pA/√Hz

NOTES:

1. Measured from T_{MIN}, T_{MAX}.
2. ±VCC = ±4.5V to 5.5V.
3. $±V_{IN}$ = ±2.5V, V_{OUT} = 0V

Closed-Loop AC Electrical Specifications

V_S = ±5V, A_V = +1, Rf = 0Ω, R_L = 100Ω unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
SSBW	-3dB Bandwidth (V_{OUT} = $0.4V_{PP}$)	A_V = +1	25°C	150	300		MHz
		A_V = -1	25°C		200		MHz
		A_V = +2	25°C	150	200		MHz
			T_{MIN}, T_{MAX}	125			MHz
		A_V = +5	25°C		40		MHz
		A_V = +10	25°C		20		MHz
GBWP	Gain-Bandwidth Product	A_V = +10	25°C		200		MHz
LSBWa	-3dB Bandwidth	V_{OUT} = $2V_{PP}$ (Note 1)	All	50	85		MHz
LSBWb	-3dB Bandwidth	V_{OUT} = $5V_{PP}$ (Note 1)	All	11	16		MHz
GFPL	Peaking (< 50MHz)	V_{OUT} = $0.4V_{PP}$	25°C		0	0.5	dB
			T_{MIN}, T_{MAX}			0.5	dB
GFPH	Peaking (> 50MHz)	V_{OUT} = $0.4V_{PP}$	25°C		1	3	dB
			T_{MIN}, T_{MAX}			3	dB
GFR	Rolloff (< 100MHz)	V_{OUT} = $0.4V_{PP}$	25°C		0.1	0.5	dB
			T_{MIN}, T_{MAX}			0.5	dB
LPD	Linear Phase Deviation (< 100MHz)	V_{OUT} = $0.4V_{PP}$	All		1	1.8	°
PM	Phase Margin	A_V = +1	25°C		60		°
tr1, tf1	Rise Time, Fall Time	0.4V Step, A_V = +2	25°C		2		ns
tr2, tf2	Rise Time, Fall Time	5V Step, A_V = +2	25°C		15		ns
ts1	Settling to 0.1% (A_V = -1)	2V Step	25°C		13		ns
ts2	Settling to 0.01% (A_V = -1)	2V Step	25°C		25		ns
OS	Overshoot	2V Step	25°C		5		%
SR	Slew Rate	2V Step	All	175	250		V/µs
DISTORTION (Note 2)							
HD2a	2nd Harmonic Distortion	@ 10MHz, A_V = +2	25°C		-65	-55	dBc
HD2b	2nd Harmonic Distortion	@ 20MHz, A_V = +1	25°C		-60	-50	dBc
HD2c	2nd Harmonic Distortion	@ 20MHz, A_V = +2	25°C		-55	-50	dBc
			T_{MIN}, T_{MAX}			-45	dBc
HD3a	3rd Harmonic Distortion	@ 10MHz, A_V = +2	25°C		-72	-60	dBc
HD3b	3rd Harmonic Distortion	@ 20MHz, A_V = +1	25°C		-70	-55	dBc

Closed-Loop AC Electrical Specifications

V_S = ±5V, A_V = +1, Rf = 0Ω, R_L = 100Ω unless otherwise specified **(Continued)**

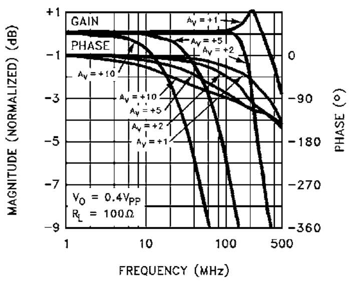
PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
HD3c	3rd Harmonic Distortion	@ 20MHz, A_V = +2	25°C		-70	-60	dBc
			T_{MIN}, T_{MAX}			-60	dBc
VIDEO PERFORMANCE (Note 3)							
dG	Differential Gain	NTSC	25°C		0.01	0.05	$\%_{pp}$
dP	Differential Phase	NTSC	25°C		0.015	0.05	$°_{pp}$
dG	Differential Gain	30MHz	25°C		0.1		$\%_{pp}$
dP	Differential Phase	30MHz	25°C		0.1		$°_{pp}$
VBW	±0.1dB Bandwidth Flatness		25°C	25	50		MHz

NOTES:

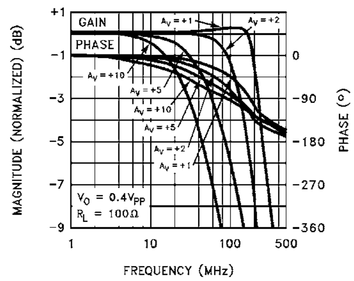
1. Large-signal bandwidth calculated using LSBW = Slew Rate / 2π V_{PEAK}.
2. All distortion measurements are made with V_{OUT} = $2V_{PP}$, R_L = 100Ω.
3. Video performance measured at A_V = +1 with 2 times normal video level across R_L = 100Ω. This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a $1V_{PP}$ video signal across the 50Ω load. For other values of R_L, see curves.

Typical Performance Curves

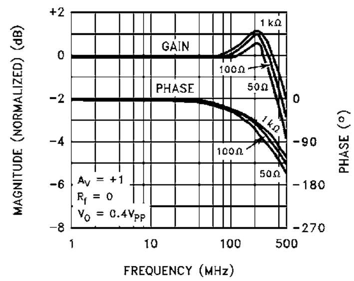
Non-Inverting Frequency Response



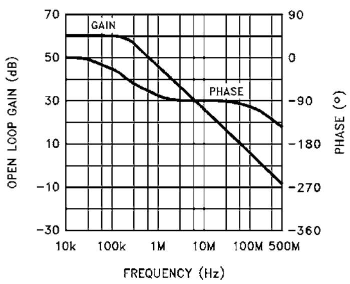
Inverting Frequency Response



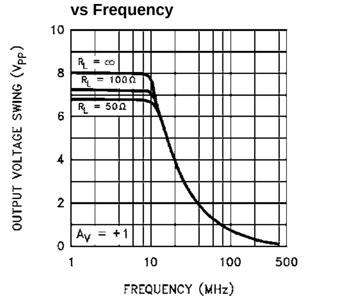
Frequency Response for Various R_Ls



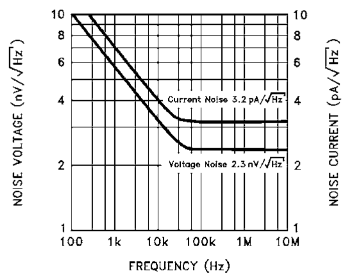
Open Loop Gain and Phase



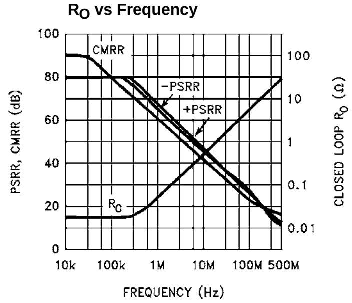
Output Voltage Swing vs Frequency



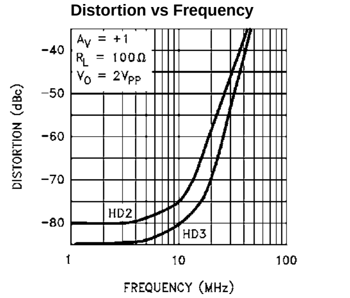
Equivalent Input Noise



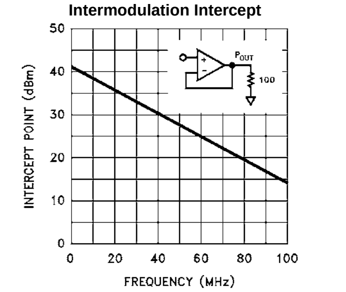
PSRR, CMRR, and Closed-Loop R_O vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency

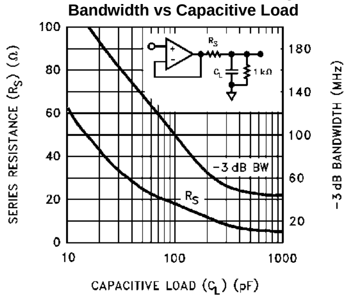


2-Tone, 3rd Order Intermodulation Intercept

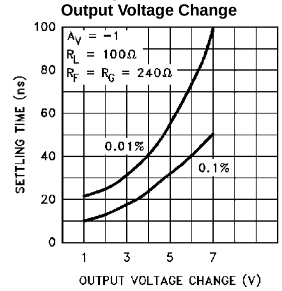


Typical Performance Curves (Continued)

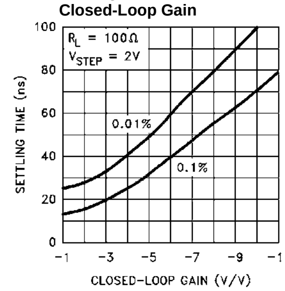
Series Resistor and Resulting Bandwidth vs Capacitive Load



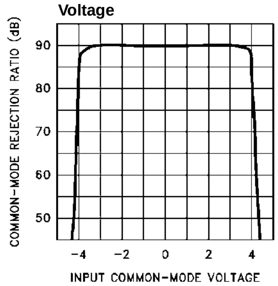
Settling Time vs Output Voltage Change



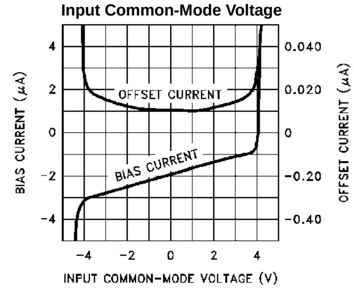
Settling Time vs Closed-Loop Gain



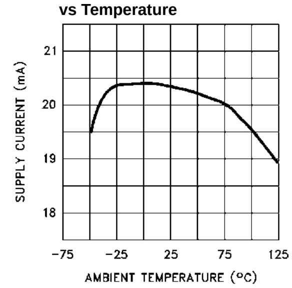
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



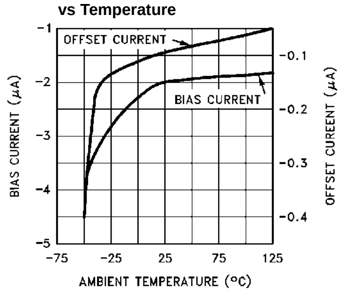
Bias and Offset Current vs Input Common-Mode Voltage



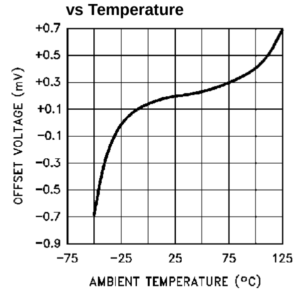
Supply Current vs Temperature



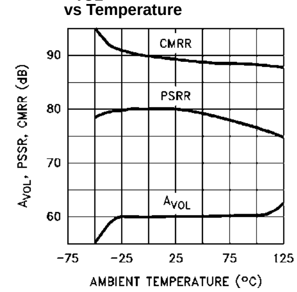
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature

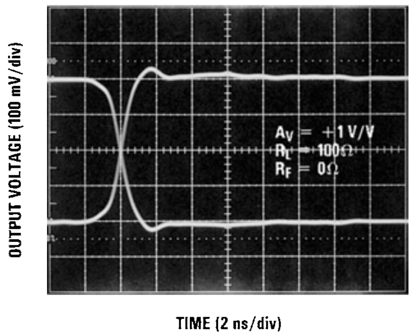


A_{VOL}, PSRR, and CMRR vs Temperature

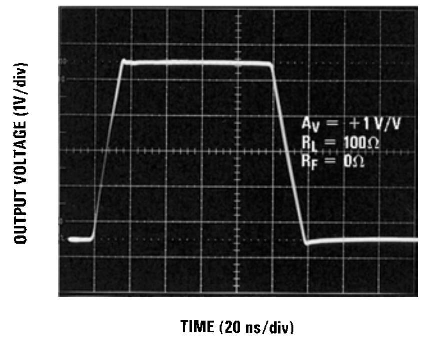


Typical Performance Curves (Continued)

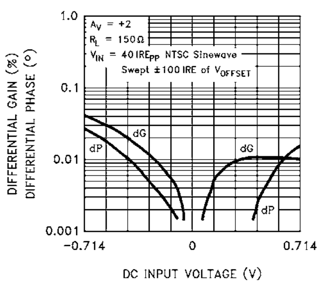
Small Signal Transient Response



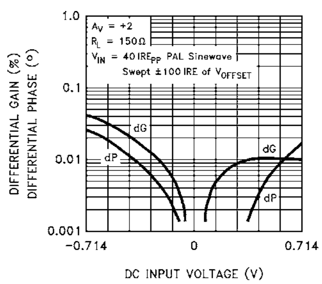
Large Signal Transient Response



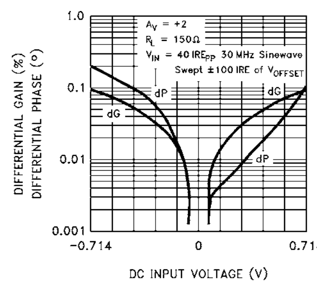
Differential Gain and Phase vs DC Input Offset at 3.58MHz



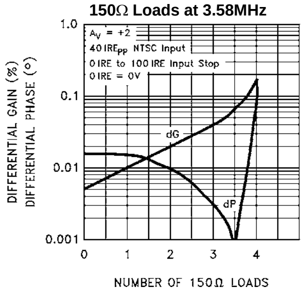
Differential Gain and Phase vs DC Input Offset at 4.43MHz



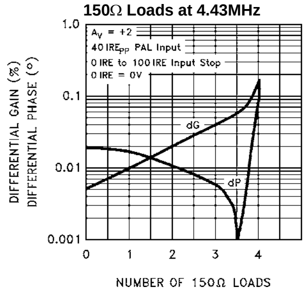
Differential Gain and Phase vs DC Input Offset at 30MHz



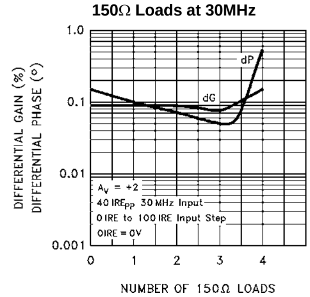
Differential Gain and Phase vs Number of 150Ω Loads at 3.58MHz



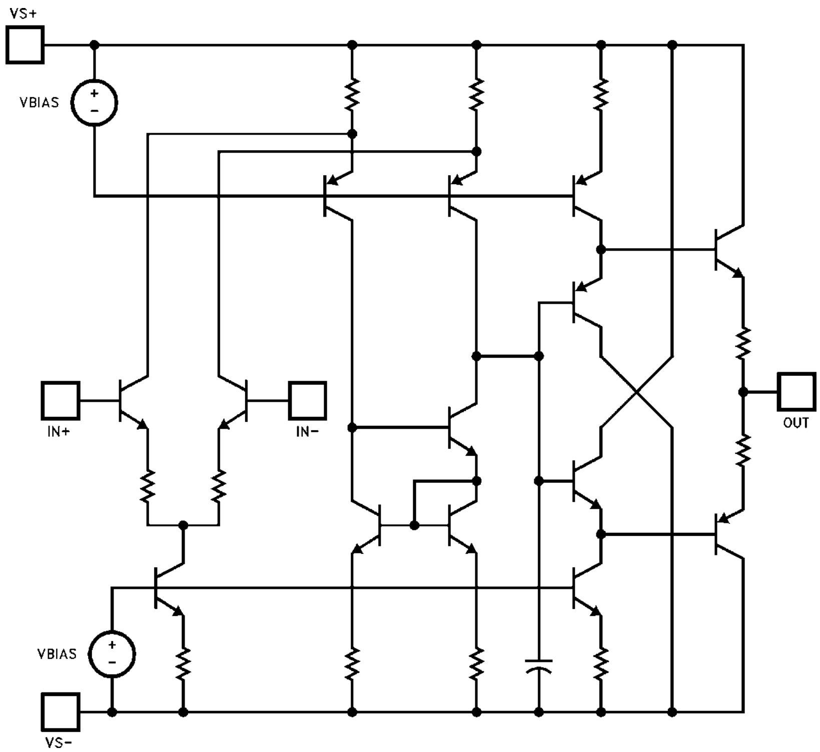
Differential Gain and Phase vs Number of 150Ω Loads at 4.43MHz



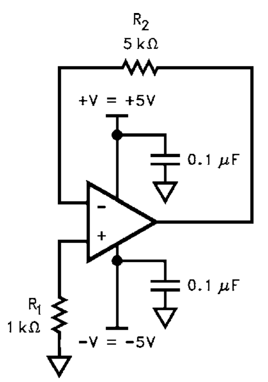
Differential Gain and Phase vs Number of 150Ω Loads at 30MHz



Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC

Applications Information

Product Description

The EL2073 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2073 uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2073 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2073 is an excellent choice for applications such as log amplifiers.

The EL2073 also has excellent DC specifications: 200µV, V_{OS}, 2µA I_B, 0.1µA I_{OS}, and 90dB of CMRR. These specifications allow the EL2073 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2073 is only 3.2pA/√Hz, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2073 has a gain-bandwidth product of 200MHz. For gains greater than 4, its closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2073 has a -3dB bandwidth of 400MHz at a gain of +1, dropping to 200MHz at a gain of +2. It is important to note that the EL2073 has been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2073 in a gain of +1 only exhibits 1dB of peaking with a 100Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2073 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a $0.286V_{PP}$ (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58MHz for NTSC, 4.43MHz for PAL, or 30MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2073 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2073 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2073 has been characterized over the entire DC offset range from -0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2073 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2073 has been optimized to drive 50Ω and 75Ω loads. It can easily drive $6V_{PP}$ into a 50Ω load. This high output drive capability makes the EL2073 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2073 remains a minimum of 50mA at low temperatures. The EL2073 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2073 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1µF–10µF tantalum capacitor is recommended in parallel with a 0.01µF ceramic capacitor. All pin lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2073 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2073 Macromodel

```
*
* Connections:   input
*                |    -input
*                |    |    +Vsupply
*                |    |    |    -Vsupply
*                |    |    |    |    output
*                |    |    |    |    |
.subckt M2073C   3    2    7    4    6
*
*Input Stage
*
ie 37 4 1mA
r6 36 37 125
r7 38 37 125
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 1.2pF
rc 34 40 400
cc 40 0 0.3pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 0.5pF
rpb 42 43 50
cpb 43 0 0.5pF
*
* Output Stage
*
ios1 7 50 3.0mA
ios2 51 4 3.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
Power Supply Current
*
ips 7 4 11.4mA
*
Models
*
.model qna npn(is800e-18 bf170 tf0.2ns)
.model qn  npn(is810e-18 bf200 tf0.2ns)
.model qp  pnp(is800e-18 bf200 tf0.2ns)
.ends
```

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com