

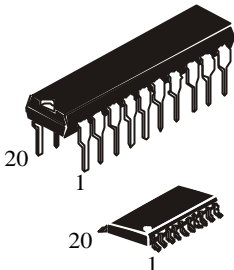
**IN74LV241**

**OCTAL BUFFER/LINE DRIVE; 3-STATE**

The IN74LV241 is a low-voltage Si-gate CMOS device and is pin and function compatible with IN74HC/HCT241.

The IN74LV241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0  $\mu$ A, 0.1  $\mu$ A at  $\theta = 25^\circ\text{C}$
- Output Current: 8 mA at  $V_{CC} = 3.0$  V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX  
PLASTIC DIP

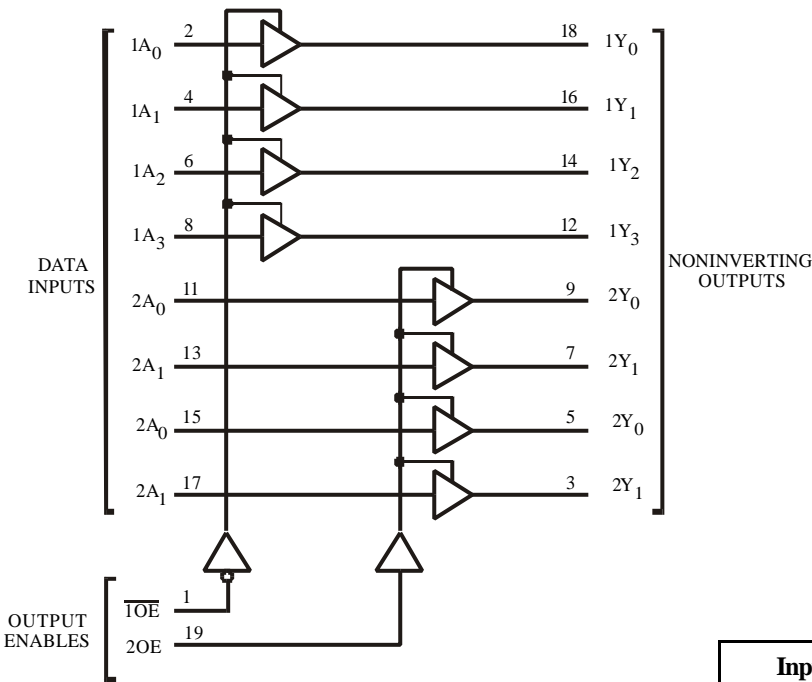
DW SUFFIX  
SO

**ORDERING INFORMATION**

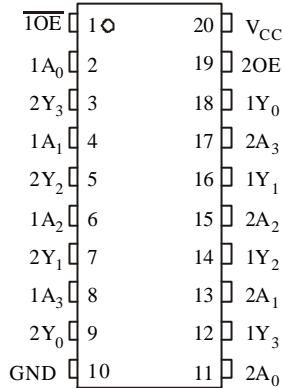
**IN74LV241N** Plastic DIP  
**IN74LV241DW** SOIC  
**IZ74LV241** chip

$T_A = -40^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Input		Output	Input		Output
1OE	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

H= high level  
 L = low level  
 X = don't care  
 Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	-0.5 to +5.0	V
$I_{IK}^{*1}$	DC Input diode current	$\pm 20$	mA
$I_{OK}^{*2}$	DC Output diode current	$\pm 50$	mA
$I_O^{*3}$	DC Output source or sink current	$\pm 35$	mA
$I_{CC}$	DC $V_{CC}$ current	$\pm 70$	mA
$I_{GND}$	DC GND current	$\pm 70$	mA
$P_D$	Power dissipation per package: <sup>*4</sup> Plastic DIP SO	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

<sup>\*1</sup>  $V_I < -0.5$  V or  $V_I > V_{CC} + 0.5$  V.

<sup>\*2</sup>  $V_O < -0.5$  V or  $V_O > V_{CC} + 0.5$  V.

<sup>\*3</sup>  $-0.5$  V  $< V_O < V_{CC} + 0.5$  V.

<sup>\*4</sup> Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C  
SO Package: : - 8 mW/°C from 70° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	1.2	3.6	V
$V_I$	Input Voltage	0	$V_{CC}$	V
$V_O$	Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC}=1.2$ V	0	1000	
	$V_{CC}=2.0$ V	0	700	
	$V_{CC}=3.0$ V	0	500	
	$V_{CC}=3.6$ V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V <sub>IH</sub>	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V <sub>IL</sub>	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
			V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -8 mA	3.0	2.48	-	2.34	-	2.20	-
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.1	-	0.1	
			V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 8 mA	3.0	-	0.33	-	0.4	-	0.5
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or 0 V	*	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	Three state leakage current	3-state outputs V <sub>I</sub> (01,19) = V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> or 0 V	1.2 *	-	±0.5	-	±5	-	±10	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	*	-	8.0	-	80	-	160	μA

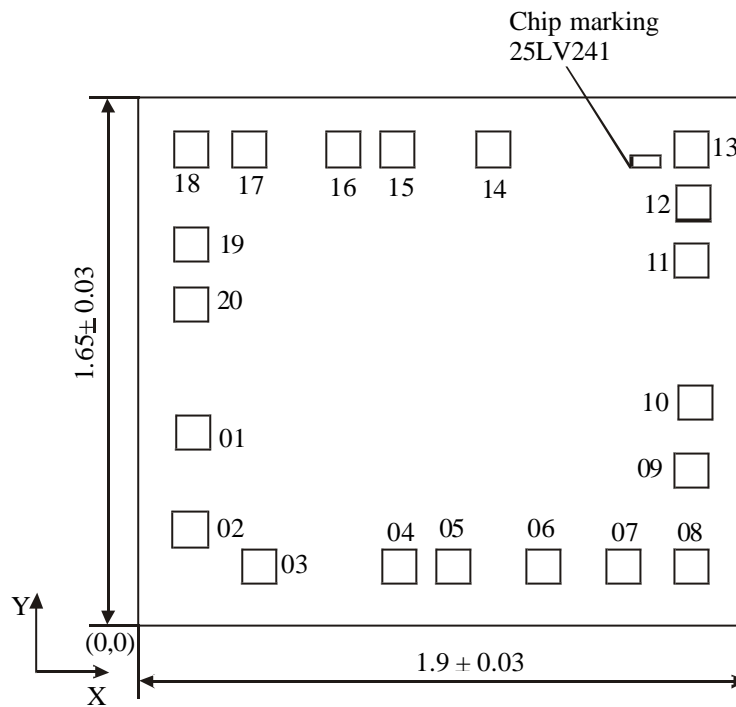
\* V<sub>CC</sub> = 3.3 ± 0.3 V



Figure 3. Test Circuit

Figure 4. Test Circuit

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner  $x=1.539$ ,  $y=1.433$ .

Chip thickness:  $0.46 \pm 0.02$  mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	1OE	0.115	0.55	0.108 x 0.108
02	1A <sub>0</sub>	0.1075	0.246	0.108 x 0.108
03	2Y <sub>3</sub>	0.3215	0.131	0.108 x 0.108
04	1A <sub>1</sub>	0.76	0.131	0.108 x 0.108
05	2Y <sub>2</sub>	0.9285	0.131	0.108 x 0.108
06	2A <sub>2</sub>	1.2115	0.131	0.108 x 0.108
07	2Y <sub>1</sub>	1.4615	0.131	0.108 x 0.108
08	2A <sub>3</sub>	1.674	0.131	0.108 x 0.108
09	2Y <sub>0</sub>	1.674	0.43	0.108 x 0.108
10	GND	1.685	0.643	0.108 x 0.108
11	2A <sub>0</sub>	1.674	1.0855	0.108 x 0.108
12	1Y <sub>3</sub>	1.6795	1.266	0.108 x 0.108
13	2A <sub>1</sub>	1.674	1.4345	0.108 x 0.108
14	1Y <sub>2</sub>	1.0525	1.4345	0.108 x 0.108
15	2A <sub>2</sub>	0.7545	1.4345	0.108 x 0.108
16	1Y <sub>1</sub>	0.586	1.4345	0.108 x 0.108
17	2A <sub>3</sub>	0.293	1.4345	0.108 x 0.108
18	1Y <sub>0</sub>	0.112	1.4345	0.108 x 0.108
19	2OE	0.112	1.1385	0.108 x 0.108
20	V <sub>CC</sub>	0.112	0.949	0.108 x 0.108

Note: Pad location is given as per metallization layer