

IW4021B

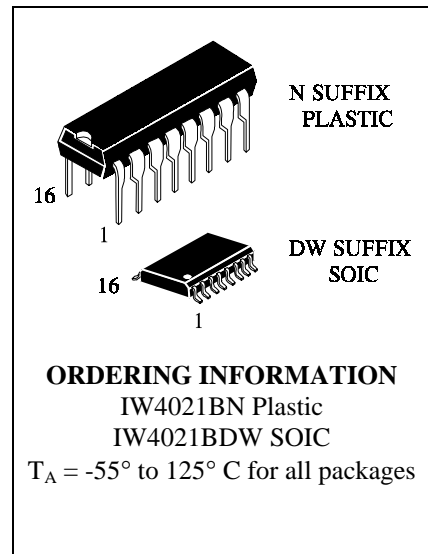
8-Bit Shift Register
High-Voltage Silicon-Gate CMOS

The IW4021B is an Edge-Triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P₀-P₇) and Buffered Parallel Outputs from the last three stages (Q₅-Q₇).

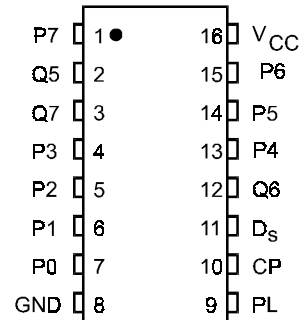
Information on the Parallel Data Inputs (P₀-P₇) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL).

When the Parallel Load Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

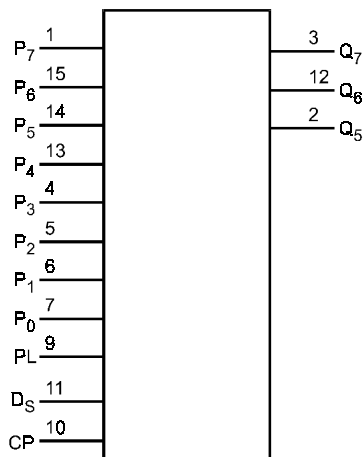
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

SERIAL OPERATION:

| t | CP | D _S | PL | Q ₅ t=n+6 | Q ₆ t=n+7 | Q ₇ t=n+8 |
|-----|----|----------------|----|-------------------------|-------------------------|-------------------------|
| n | ⌊ | 0 | 0 | 0 | | |
| n+1 | ⌋ | 1 | 0 | 1 | 0 | |
| n+2 | ⌊ | 0 | 0 | 0 | 1 | 0 |
| n+3 | ⌋ | 1 | 0 | 1 | 0 | 1 |
| | ⌋ | X | 0 | Q ₅ | Q ₆ | Q ₇ |

PARALLEL OPERATION:

| CP | D _S | PL | P ₅ | P ₆ | P ₇ | Q ₅ | Q ₆ | Q ₇ |
|----|----------------|----|----------------|----------------|----------------|----------------|----------------|----------------|
| X | X | 1 | D | D | D | D | D | D |

X = don't care
D = 1 or 0

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +20 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±10 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| P _D | Power Dissipation per Output Transistor | 100 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 3.0 | 18 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
| | | | | ≥-55°C | 25°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.5 V or V _{CC} - 0.5 V | 5.0 | 3.5 | 3.5 | 3.5 | V |
| | | V _{OUT} =1.0 V or V _{CC} - 1.0 V | 10 | 7 | 7 | 7 | |
| | | V _{OUT} =1.5 V or V _{CC} - 1.5 V | 15 | 11 | 11 | 11 | |
| V _{IL} | Maximum Low -Level Input Voltage | V _{OUT} =0.5 V or V _{CC} - 0.5 V | 5.0 | 1.5 | 1.5 | 1.5 | V |
| | | V _{OUT} =1.0 V or V _{CC} - 1.0 V | 10 | 3 | 3 | 3 | |
| | | V _{OUT} =1.5 V or V _{CC} - 1.5 V | 15 | 4 | 4 | 4 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} =GND or V _{CC} | 5.0 | 4.95 | 4.95 | 4.95 | V |
| | | | 10 | 9.95 | 9.95 | 9.95 | |
| | | | 15 | 14.95 | 14.95 | 14.95 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} =GND or V _{CC} | 5.0 | 0.05 | 0.05 | 0.05 | V |
| | | | 10 | 0.05 | 0.05 | 0.05 | |
| | | | 15 | 0.05 | 0.05 | 0.05 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = GND or V _{CC} | 18 | ±0.1 | ±0.1 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} = GND or V _{CC} | 5.0 | 5.0 | 5.0 | 150 | μA |
| | | | 10 | 10 | 10 | 300 | |
| | | | 15 | 20 | 20 | 600 | |
| | | | 20 | 100 | 100 | 3000 | |
| I _{OL} | Minimum Output Low (Sink) Current | V _{IN} = GND or V _{CC} V _{OL} =0.4 V V _{OL} =0.5 V V _{OL} =1.5 V | 5.0 | 0.64 | 0.51 | 0.36 | mA |
| | | | 10 | 1.6 | 1.3 | 0.9 | |
| | | | 15 | 4.2 | 3.4 | 2.4 | |
| | | | | | | | |
| I _{OH} | Minimum Output High (Source) Current | V _{IN} = GND or V _{CC} V _{OH} =2.5 V V _{OH} =4.6 V V _{OH} =9.5 V V _{OH} =13.5 V | 5.0 | -2.0 | -1.6 | -1.15 | mA |
| | | | 5.0 | -0.64 | -0.51 | -0.36 | |
| | | | 10 | -1.6 | -1.3 | -0.9 | |
| | | | 15 | -4.2 | -3.4 | -2.4 | |

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|-------------------------------------|--|----------------------|------------------|------|--------|------|
| | | | ≥-55°C | 25°C | ≤125°C | |
| f _{max} | Maximum Clock Frequency | 5.0 | 3.0 | 3.0 | 1.5 | MHz |
| | | 10 | 6.0 | 6.0 | 3.0 | |
| | | 15 | 8.5 | 8.5 | 4.25 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, CP to Qn | 5.0 | 320 | 320 | 640 | ns |
| | | 10 | 160 | 160 | 320 | |
| | | 15 | 120 | 120 | 240 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, PL to Qn | 5.0 | 320 | 320 | 640 | ns |
| | | 10 | 160 | 160 | 320 | |
| | | 15 | 120 | 120 | 240 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output | 5.0 | 200 | 200 | 400 | ns |
| | | 10 | 100 | 100 | 200 | |
| | | 15 | 80 | 80 | 160 | |
| C _{IN} | Maximum Input Capacitance | 5.0 | | 7.5 | | pF |

TIMING REQUIREMENTS($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|--|----------------------|------------------|------|--------|------|
| | | | ≥-55°C | 25°C | ≤125°C | |
| t _w | Minimum Pulse Width CP | 5.0 | 160 | 160 | 320 | ns |
| | | 10 | 80 | 80 | 160 | |
| | | 15 | 50 | 50 | 100 | |
| t _w | Minimum Pulse Width PL | 5.0 | 180 | 180 | 360 | ns |
| | | 10 | 80 | 80 | 160 | |
| | | 15 | 50 | 50 | 100 | |
| t _{su} | Minimum Setup Time, D _S to CP | 5.0 | 120 | 120 | 240 | ns |
| | | 10 | 80 | 80 | 160 | |
| | | 15 | 60 | 60 | 120 | |
| t _{su} | Minimum Setup Time, P _n to PL | 5.0 | 50 | 50 | 100 | ns |
| | | 10 | 30 | 30 | 60 | |
| | | 15 | 20 | 20 | 40 | |
| t _h | Minimum Hold Time, D _S to CP | 5.0 | 0 | 0 | 0 | ns |
| | | 10 | 0 | 0 | 0 | |
| | | 15 | 0 | 0 | 0 | |
| t _h | Minimum Hold Time, P _n to PL | 5.0 | 0 | 0 | 0 | ns |
| | | 10 | 0 | 0 | 0 | |
| | | 15 | 0 | 0 | 0 | |
| t _{rec} | Minimum Recovery Time PL | 5.0 | 280 | 280 | 560 | ns |
| | | 10 | 140 | 140 | 240 | |
| | | 15 | 100 | 100 | 200 | |
| t _r , t _f | Maximum Input Rise or Fall Time | 5.0 | 15 | 15 | 15 | μs |
| | | 10 | 15 | 15 | 15 | |
| | | 15 | 15 | 15 | 15 | |

EXPANDED LOGIC DIAGRAM

