

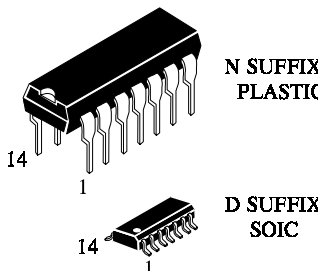
**IN74LV32**

**Quad 2-Input OR Gate**

The IN74LV32 is low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT32A.

The IN74LV32 provides the 2-input AND function.

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7\text{ V}$  and  $V_{CC} = 3.6\text{ V}$
- Low Input Current

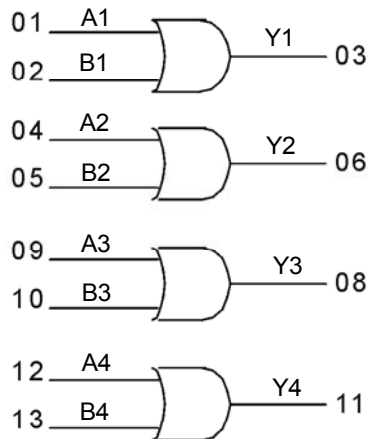


**ORDERING INFORMATION**

IN74LV32N	Plastic
IN74LV32D	SOIC
IZ74LV32	Chip

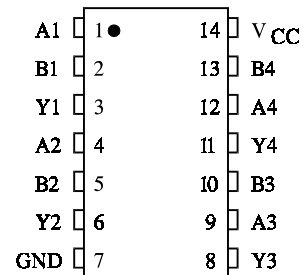
$T_A = -40^\circ \div 125^\circ\text{ C}$  for all packages

**LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Input		Output
A	B	$Y = A*B$
L	L	L
L	H	H
H	L	H
H	H	H

H - high level  
L - low level



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage (Referenced to GND)	-0.5 ÷ +5.0	V
$I_{IK}^{*1}$	DC input diode current	±20	mA
$I_{OK}^{*2}$	DC output diode current	±50	mA
$I_O^{*3}$	DC output source or sink current -bus driver outputs	±25	mA
$I_{CC}$	DC $V_{CC}$ current for types with - bus driver outputs	±50	mA
$I_{GND}$	DC GND current for types with - bus driver outputs	±50	mA
$P_D$	Power dissipation per package, plastic DIP+ SOIC package+	750 500	mW
Tstg	Storage temperature	-65 ÷ +150	°C
$T_L$	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP ), 0.3 mm (SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SOIC Package: : - 8 mW/°C from 70° to 125°C

\*<sup>1</sup>:  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$

\*<sup>2</sup>:  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$

\*<sup>3</sup>:  $-0.5V < V_O < V_{CC} + 0.5V$

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	1.2	3.6	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+125	°C
$t_r, t_f$	Input Rise and Fall Time			ns
	$V_{CC} = 1.2 V$	0	1000	
	$V_{CC} = 2.0 V$	0	700	
	$V_{CC} = 3.0 V$	0	500	
	$V_{CC} = 3.6 V$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.



## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> , V	Guaranteed Limit						Unit	
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C			
				min	max	min	max	min	max		
V <sub>IH</sub>	High-Level Input Voltage		1.2	0.9	-	0.9	-	0.9	-	V	
			2.0	1.4	-	1.4	-	1.4	-		
			3.0	2.1	-	2.1	-	2.1	-		
			3.6	2.5	-	2.5	-	2.5	-		
V <sub>IL</sub>	Low-Level Input Voltage		1.2	-	0.3	-	0.3	-	0.3	V	
			2.0	-	0.6	-	0.6	-	0.6		
			3.0	-	0.9	-	0.9	-	0.9		
			3.6	-	1.1	-	1.1	-	1.1		
V <sub>OH</sub>	High-Level Output Voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V	
			2.0	1.92	-	1.9	-	1.9	-		
			3.0	2.92	-	2.9	-	2.9	-		
			3.6	3.52	-	3.5	-	3.5	-		
	V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>O</sub> = -6.0 mA	3.0	2.48	-	2.34	-	2.20	-	V
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V	
			2.0	-	0.09	-	0.1	-	0.1		
			3.0	-	0.09	-	0.1	-	0.1		
			3.6	-	0.09	-	0.1	-	0.1		
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>O</sub> = 6.0 mA	3.0	-	0.33	-	0.4	-	0.5	V	
I <sub>IL</sub>	Low-Level Input Leakage Current	V <sub>I</sub> = 0 V	3.6	-	-0.1	-	-1.0	-	-1.0	μA	
I <sub>IH</sub>	High-Level Input Leakage Current	V <sub>I</sub> = V <sub>CC</sub>	3.6	-	0.1	-	1.0	-	1.0	μA	
I <sub>CC</sub>	Quiescent Supply Current (per Package)	V <sub>I</sub> = 0 B or V <sub>CC</sub> I <sub>O</sub> = 0 μA	3.6	-	2.0	-	20	-	40	μA	

**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50$  pF,  $t_{LH} = t_{HL} = 6.0$  ns,  $V_{IL} = 0V$ ,  $V_{IH}=V_{CC}$ ,  $R_L=1k\Omega$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit						Unit
			25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
			min	max	min	max	min	max	
t <sub>THL</sub> , (t <sub>TLH</sub> )	Output Transition Time, Any Output (Figure 1)	1.2	-	60	-	75	-	90	ns
		2.0	-	16	-	20	-	24	
		*	-	10	-	13	-	15	
t <sub>PHL</sub> , (t <sub>PLH</sub> )	Propagation Delay, Input A to Output Y (Figure 1)	1.2	-	125	-	360	-	360	
		2.0	-	20	-	25	-	30	
		*	-	12	-	15	-	18	
C <sub>I</sub>	Input Capacitance	3.0	-	7.0	-	-	-	-	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate)	T <sub>A</sub> =25°C, V <sub>I</sub> =0V÷V <sub>CC</sub>						pF
		44						

\* - V<sub>CC</sub>= (3.3±0.3) V

$$P_D = C_{PD}V_{CC}^2f_i + \sum(C_LV_{CC}^2f_o), f_i\text{-input frequency, } f_o\text{- output frequency (MHz)}$$

$\sum(C_LV_{CC}^2f_o)$  – sum of the outputs

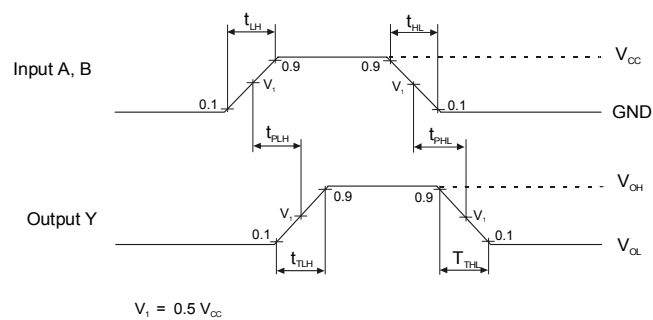


Figure 1. Switching Waveforms

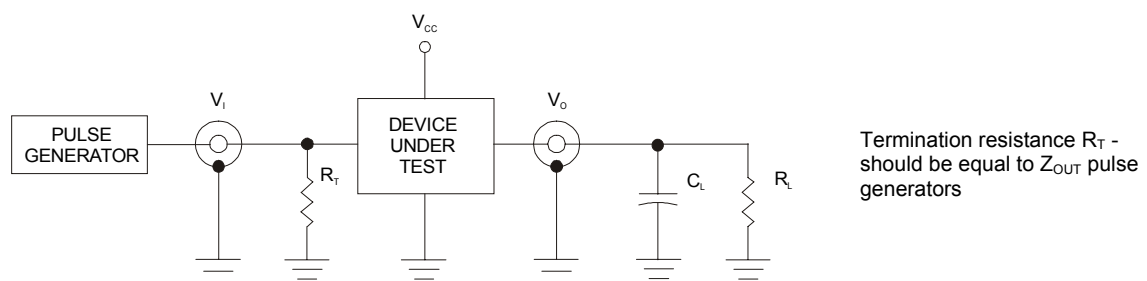
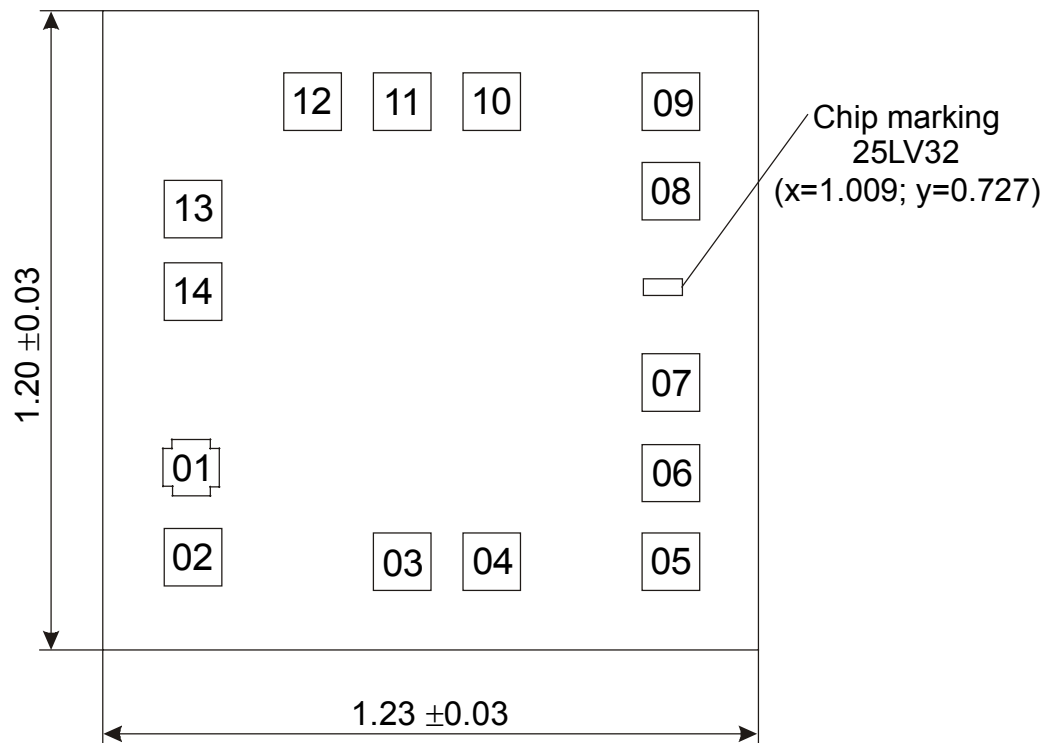


Figure 2. Test Circuit

## CHIP PAD DIAGRAM IZ74LV32



Pad size 0.108 x 0.108 mm (Pad size is given as per metallization layer)

Thickness of chip  $0.46 \pm 0.02$  mm

## PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.111	0.287
02	B1	0.111	0.119
03	Y1	0.504	0.111
04	A2	0.672	0.111
05	B2	1.009	0.111
06	Y2	1.009	0.277
07	GND	1.009	0.447
08	Y3	1.009	0.806
09	A3	1.009	0.974
10	B3	0.672	0.974
11	Y4	0.504	0.974
12	A4	0.336	0.974
13	B4	0.111	0.772
14	Vcc	0.111	0.618

