Integrated Device Technology, Inc.

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
  FST163xxx – 5Ω
  FST163Pxxx – 5Ω with precharge
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP

DESCRIPTION:

The FST163245/163P245 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163245 and FST163P245 are 16-bit TTL-compatible bus switches. The $\overline{OE}$ pins provide enable control. The FST163P245 supports precharge on the B port. So when $\overline{OE}$ is high, A and B ports are isolated and B outputs are precharged to the bias voltage through the equivalent of a 10KΩ resistor ($1B_{1-8}$ precharged to V_{BIAS1} and $2B_{1-8}$ precharged to V_{BIAS1}).

FUNCTIONAL BLOCK DIAGRAM

FST163245

FST163P245
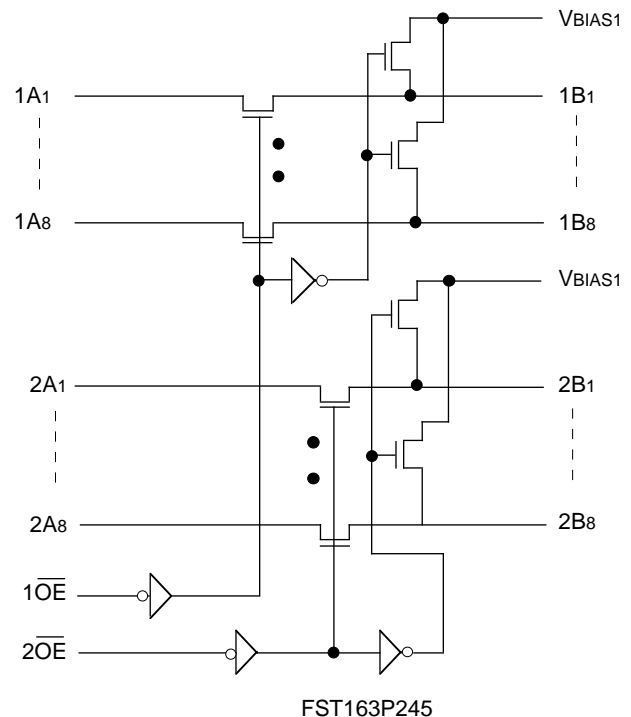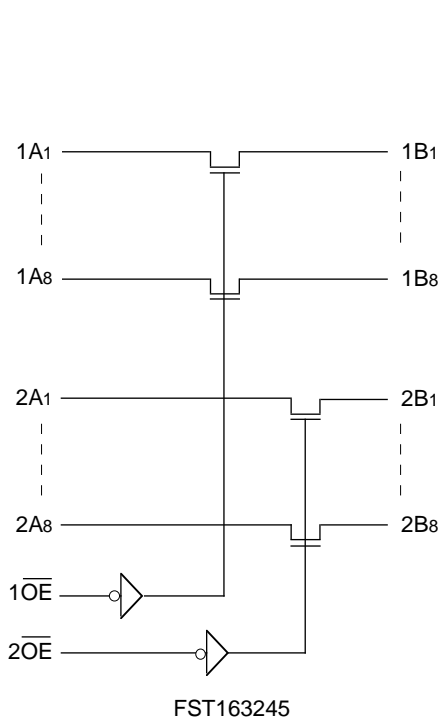
3513 drw 01

PIN DESCRIPTION

Pin Names	I/O	Description
$1A_{1-8}$, $2A_{1-8}$	I/O	Bus A
$1B_{1-8}$, $2B_{1-8}$	I/O	Bus B
$1\overline{OE}$, $2\overline{OE}$	I	Bus Switch Enable (Active LOW)
V_{BIAS1}	I	Precharge Reference Voltage

3513 tbl 01

COMMERCIAL TEMPERATURE RANGE

FEBRUARY 1997

DSC-3513/-

PIN CONFIGURATION

*NC/**V$_{BIAS1}$	1	48	1$\overline{OE}$
1B$_1$	2	47	1A$_1$
1B$_2$	3	46	1A$_2$
GND	4	45	GND
1B$_3$	5	44	1A$_3$
1B$_4$	6	43	1A$_4$
V$_{CC}$	7	42	V$_{CC}$
1B$_5$	8	41	1A$_5$
1B$_6$	9	40	1A$_6$
GND	10	39	GND
1B$_7$	11	38	1A$_7$
1B$_8$	12	37	1A$_8$
2B$_1$	13	36	2A$_1$
2B$_2$	14	35	2A$_2$
GND	15	34	GND
2B$_3$	16	33	2A$_3$
2B$_4$	17	32	2A$_4$
V$_{CC}$	18	31	V$_{CC}$
2B$_5$	19	30	2A$_5$
2B$_6$	20	29	2A$_6$
GND	21	28	GND
2B$_7$	22	27	2A$_7$
2B$_8$	23	26	2A$_8$
*NC/**GND	24	25	2$\overline{OE}$

SO48-1
SO48-2
SO48-3
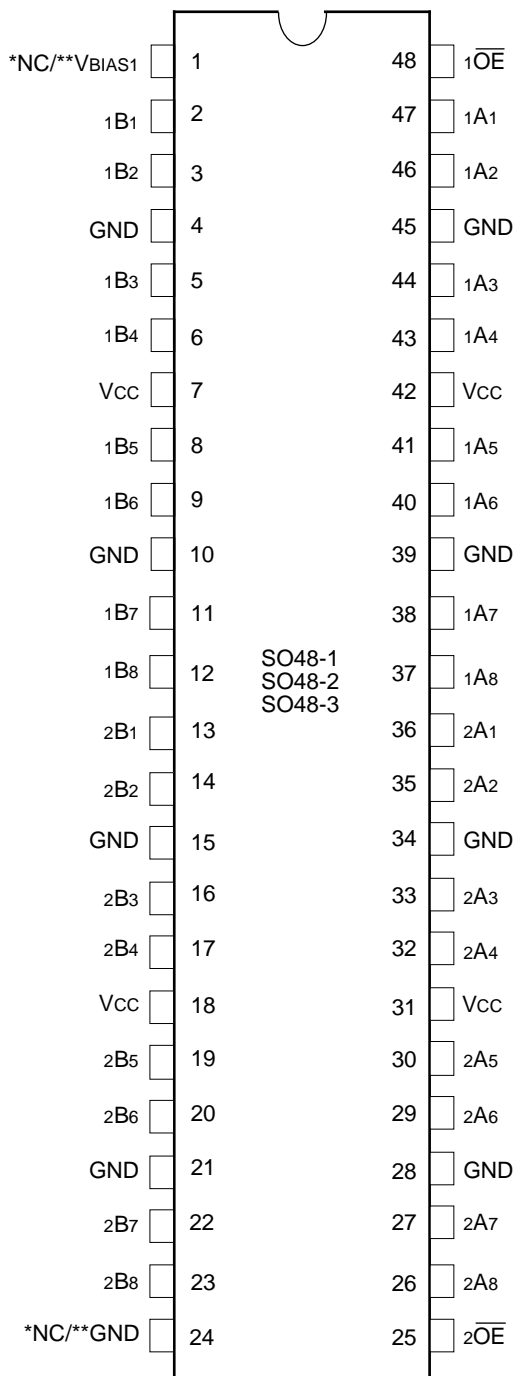
**SSOP/
TSSOP/TVSOP
TOP VIEW**

3513 drw 02

*FST163245
**FST163P245

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max.	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T$_{STG}$	Storage Temperature	−65 to +150	°C
I$_{OUT}$	Maximum Continuous Channel Current	128	mA

3513 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-
INGS may cause permanent damage to the device. This is a stress rating
only and functional operation of the device at these or any other conditions
above those indicated in the operational sections of this specification is not
implied. Exposure to absolute maximum rating condiitions for extended
periods may affect reliability.

2. V$_{CC}$, Control and Switch terminals.

CAPACITANCE[1]

Symbol	Parameter	Conditions[2]	Typ.	Unit
C$_{IN}$	Control Input Capacitance		4	pF
C$_{I/O}$	Switch Input/Output Capacitance	Switch Off		pF

3513 tbl 04

NOTES:
1. Capacitance is characterized but not tested
2. T$_A$ = 25°C, f = 1MHz, V$_{IN}$ = 0V, V$_{OUT}$ = 0V

FUNCTION TABLE

Inputs x$\overline{OE}$	Outputs
L	Bus B Data to Bus A
H	High Z State (163245) Precharge Bus B to V$_{BIAS}$ (163P245)

3513 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	μA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	μA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance[4]	V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 30mA	163xxx, 163Pxxx	—	5	7	Ω
		V_{CC} = Min. V_{IN} = 2.4V I_{ON} = 15mA	163xxx, 163Pxxx	—	10	15	Ω
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	1	μA
I_O	Precharge Output Current[5]	V_{CC} = Min., $_{BIAS}V$ = 2.4V, V_O = 0V		0.15	—	—	mA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	μA

3513 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.
5. This parameter applies to the FST163P245 only.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔICC	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max. VIN = 3.4V[3]		—	0.5	1.5	mA
ICCD	Dynamic Power Supply Current[4]	VCC = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	VIN = VCC VIN = GND	—	30	40	μA/ MHz/ Switch
IC	Total Power Supply Current[6]	VCC = Max. Outputs Open Enable Pins Toggling (16 Switches Toggling) fi = 10MHz 50% Duty Cycle	VIN = VCC VIN = GND	—	4.8	6.4	mA
			VIN = 3.4 VIN = GND	—	5.3	7.9	

3513 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient.
3. Per TTL driven input (VIN = 3.4V). All other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   ICC = Quiescent Current
   ΔICC = Power Supply Current for a TTL High Input (VIN = 3.4V)
   DH = Duty Cycle for TTL Inputs High
   NT = Number of TTL Inputs at DH
   ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fi = Input Frequency
   N = Number of Switches Toggling at fi
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = −40°C to +85°C, VCC = 5.0V ±10%

| Symbol	Description	Condition[1]	Min.[2]	Typ.	Max.	Unit
tPLH tPHL	Data Propagation Delay Ai to Bi, Bi to Ai[3,4]	CL = 50pF RL = 500Ω	—	—	0.25	ns
tPZH tPZL	Switch Turn on Delay OE to Ai, Bi		1.5	—	6.5	ns
tPHZ tPLZ	Switch Turn off Delay OE to Ai, Bi		1.5	—	5.5	ns
|QCI|	Charge Injection[5,6]		—	1.5	—	pC

3513 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10MΩ scope probe, VIN = 0.0 volts.
6. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS
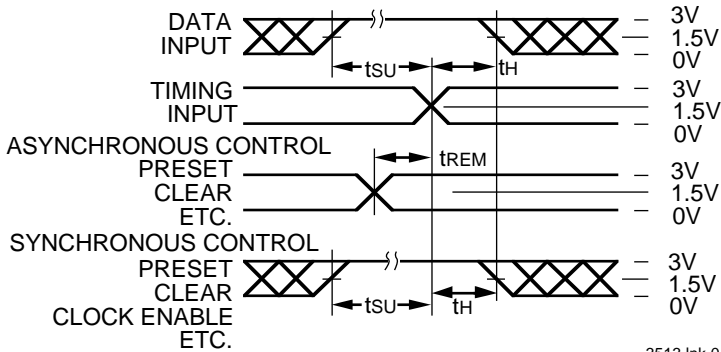## TEST CIRCUITS FOR ALL OUTPUTS
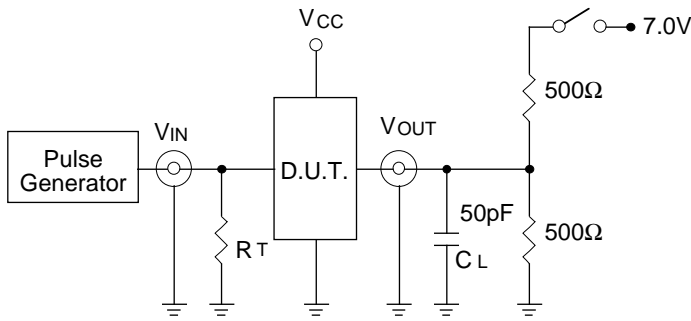
3513 lnk 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3513 lnk 08

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

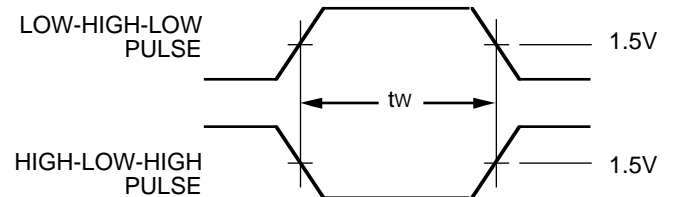R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
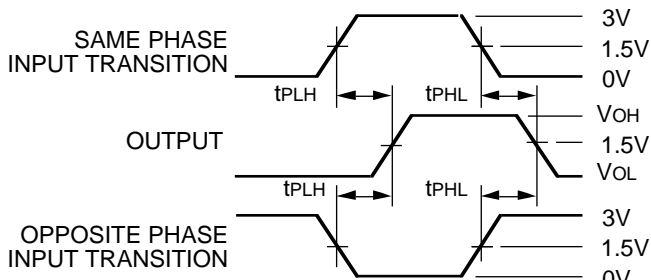
SET-UP, HOLD AND RELEASE TIMES
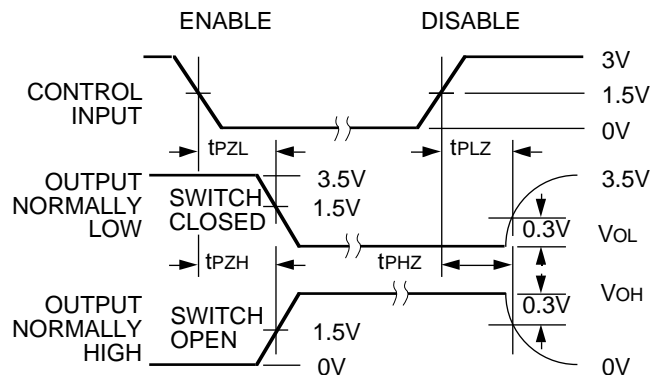

3513 lnk 04

PULSE WIDTH

3513 lnk 05

PROPAGATION DELAY

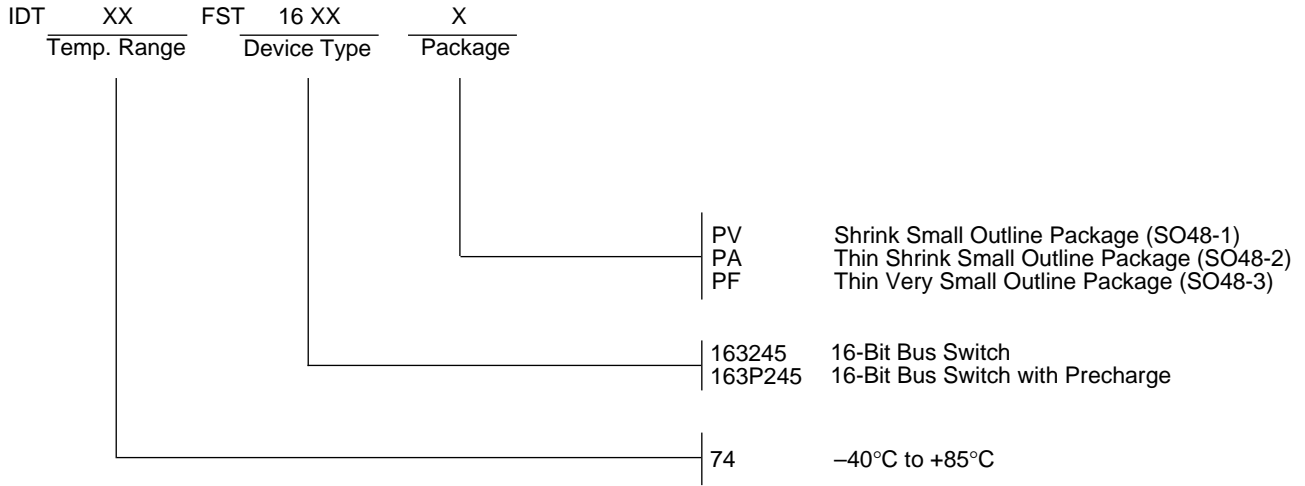
3513 lnk 06

ENABLE AND DISABLE TIMES

3513 lnk 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

2. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns

ORDERING INFORMATION

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IDT    XX     FST   16 XX        X
    Temp. Range     Device Type    Package
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PV	Shrink Small Outline Package (SO48-1)
PA	Thin Shrink Small Outline Package (SO48-2)
PF	Thin Very Small Outline Package (SO48-3)

163245	16-Bit Bus Switch
163P245	16-Bit Bus Switch with Precharge

74	–40°C to +85°C

3513 drw 08