MK2771-15
VCXO and Set-Top Clock Source

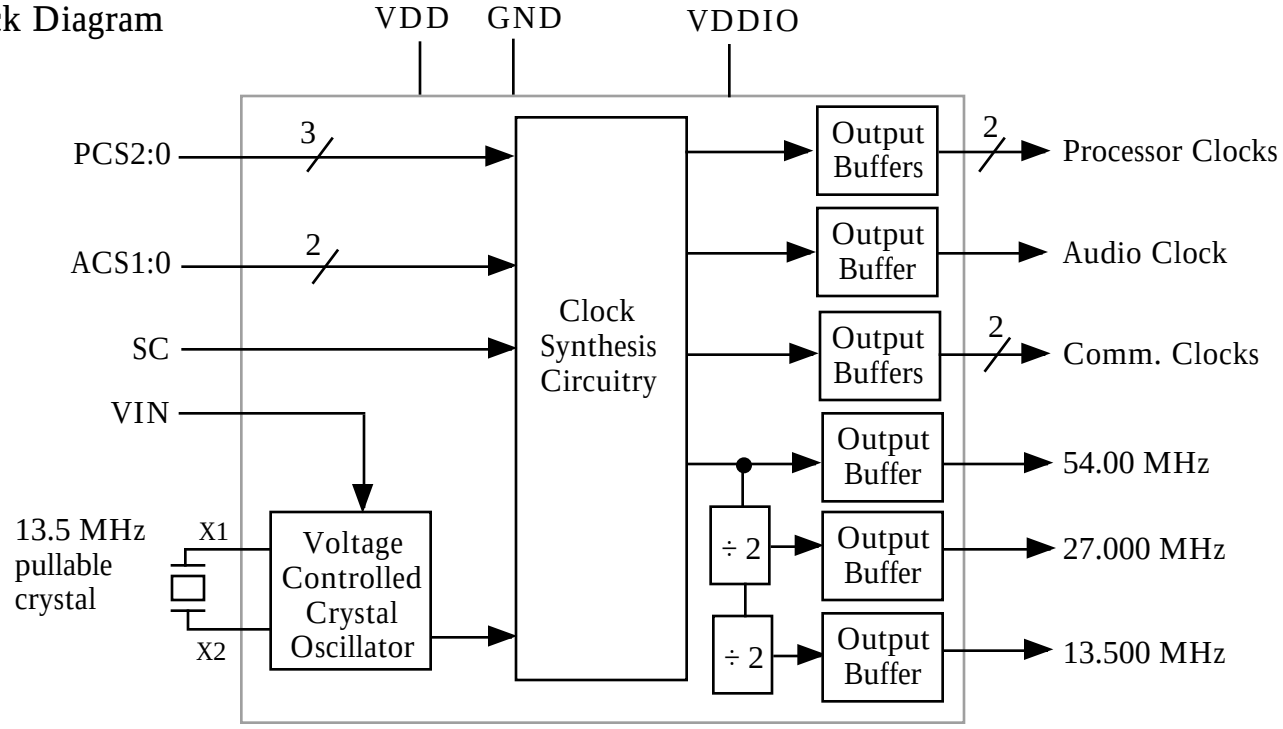
Description

The MK2771-15 is a low cost, low jitter, high performance VCXO and clock synthesizer designed for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3V input voltage to cause the output clocks to vary by ±100 ppm. Using ICS/MicroClock's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz pullable crystal input to produce multiple output clocks including two selectable processor clocks, a selectable audio clock, two communications clocks, and three fixed clocks. All clocks are frequency locked to the 27.00MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

Features

- Packaged in 28 pin SSOP (QSOP)
- Ideal for systems using Oak's MPEG decoders
- On-chip patented VCXO with pull range of 200ppm
- VCXO tuning voltage of 0 to 3 V
- Processor frequencies include 33.3, 40, 50, 66.6, 81, and 100 MHz
- Audio clocks of 8.192 MHz, 11.2896 MHz, 12.288 MHz and 18.432 MHz
- Zero ppm synthesis error in all clocks (all exactly track 27 MHz VCXO)
- Uses an inexpensive 13.5 MHz pullable crystal
- Full CMOS output swings with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5 V operating voltage with 3.3 V capable I/O

Block Diagram



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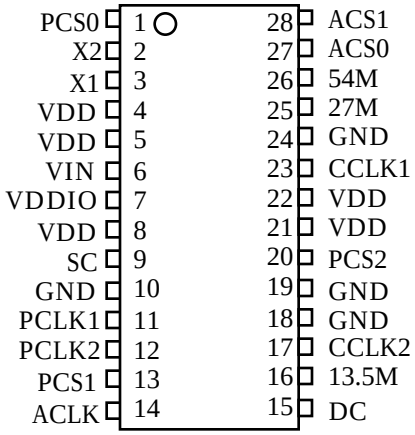
Pin Assignment



Processor Clock Select Table (MHz)

PCS2	PCS1	PCS0	PCLK1	PCLK2
0	0	0	27.500	Off
0	0	1	33.333	66.666
0	1	0	33.326	83.314
0	1	1	50.000	100.000
1	0	0	32.400	81.000
1	0	1	40.000	33.333
1	1	0	TEST	TEST
1	1	1	TEST	TEST

Audio Clock Table

ACS1	ACS0	ACLK (MHz)
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	18.432

Comm Clock Table (MHz)

SC	CCLK1	CCLK2
0	18.432	24.576
M	11.0592	18.432
1	11.0592	24.576

0 = connect directly to ground, 1 = connect directly to VDDIO, M = leave floating or unconnected

Pin Descriptions

Number	Name	Type	Description
1	PCS0	I	Processor Clock Select 0. Selects PCLKs on pins 11 and 12. See table above. Int. pull-up.
2	X2	XO	Crystal connection. Connect to a pullable 13.5 MHz crystal.
3	X1	XI	Crystal connection. Connect to a pullable 13.5 MHz crystal.
4, 5, 8	VDD	P	Connect to +5V.
6	VIN	I	Voltage Input to VCXO. Zero to 3V signal which controls the frequency of the VCXO.
7	VDDIO	P	Connect to +3.3V or +5V. Amplitude of inputs must, and outputs will, match this.
9	SC	TI	Communications clock select pin. Biased to M level if floating.
10, 18, 19, 24	GND	P	Connect to ground.
11	PCLK1	O	Processor Clock output number 1. Determined by status of PCS2:0
12	PCLK2	O	Processor Clock output number 2. Determined by status of PCS2:0
13	PCS1	I	Processor Clock Select 1. Selects PCLKs on pins 11 and 12. See table above. Int. pull-up.
14	ACLK	O	Audio Clock Output. Determined by status of ACS1, ACS0 per table above.
15	DC	-	Don't Connect anything to this pin.
16	13.5M	O	13.50 MHz VCXO clock output.
17	CCLK2	O	Communications Clock Output 2 determined by status of SC per table above.
20	PCS2	I	Processor Clock Select 2. Selects PCLKs on pins 11 and 12. See table above. Int. pull-up.
21, 22	VDD	P	Connect to +5V.
23	CCLK1	O	Communications Clock Output 1 determined by status of SC per table above.
25	27M	O	27.00 MHz VCXO clock output.
26	54M	O	54.00 MHz VCXO clock output.
27	ACS0	I	Audio Clock Select 0. Selects ACLK on pin 14. See table above. Internal pull-up.
28	ACS1	I	Audio Clock Select 1. Selects ACLK on pin 14. See table above. Internal pull-up.

Key: I = Input; TI = Tri-level input; O = output; P = power supply connection; XI, XO = crystal connections

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDDIO+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD, VDDIO = 5.0V unless noted)					
Operating Voltage, VDD		4.75		5.25	V
Operating Voltage, VDDIO	for all inputs/outputs	3.15		5.25	V
Input High Voltage, VIH, X1 pin only		3.5	2.5		V
Input Low Voltage, VIL, X1 pin only			2.5	1.5	V
Input High Voltage, VIH (except SC & PCS2)		2			V
Input Low Voltage, VIL (except SC & PCS2)				0.8	V
Input High Voltage, VIH, SC & PCS2 only		VDDIO-0.5			V
Input Low Voltage, VIL, SC & PCS2 only				0.5	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDDIO-0.4			V
Operating Supply Current, IDD+IDDIO (3.3V)	No Load, note 2		46+27		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance	Except X1, X2		7		pF
Frequency synthesis error	All clocks			0	ppm
VIN, VCXO control voltage		0		3	V
AC CHARACTERISTICS (VDD, VDDIO = 5.0V unless noted)					
Input Frequency			13.500000		MHz
Output Clock Rise Time	0.8 to 2.0V, no load			1.5	ns
Output Clock Fall Time	2.0 to 0.8V, no load			1.5	ns
Output Clock Duty Cycle	At VDDIO/2	40	50	60	%
Maximum Absolute Jitter, short term			300		ps
VCXO Pullability	Note 3	-100		100	ppm

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With PCLK at 100 MHz.
3. With a pullable crystal that conforms to ICS' specifications

External Components

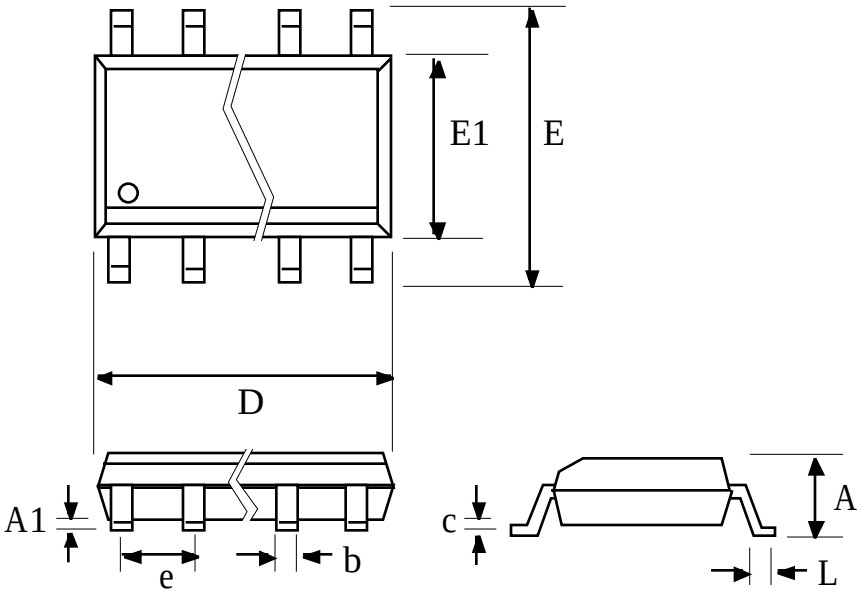
The MK2771-15 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD (or VDDIO) and GND on pins 5 and 24, 7 and 10, 22 and 19, and 21 and 18, as close to the MK2771-15 as possible. VDD on pin 8 can be connected directly to the VDD on pin 21. A series termination resistor of 33 Ω may be used for each clock output.The 13.500 MHz crystal must be connected as close to the chip as possible. The crystal should be a parallel mode, pullable, with load capacitance of 14 pF. Consult ICS/MicroClock for recommended suppliers. See MAN05 for recommended layout of the chip and external components.

Pullable Crystal Specifications

Frequency	13.500000 MHz
Correlation (load) Capacitance	14 pF
CO/C1	240 max
ESR	35 Ω max
Operating Temperature	0 to 70 °C
Initial Accuracey	±20 ppm
Temperature plus Aging Stability	±50 ppm

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.102	0.254
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.386	0.394	9.804	10.008
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
L	0.016	0.050	0.406	1.270

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2771-15R	MK2771-15R	tubes	28 pin SSOP (QSOP)	0-70 °C
MK2771-15RTR	MK2771-15R	tape and reel	28 pin SSOP (QSOP)	0-70 °C