

September 1997 Revised December 1999

FST16209 18-Bit Bus Exchange Switch

General Description

The Fairchild Switch FST16209 provides 18-bits of highspeed CMOS TTL-compatible bus switching or exchanging. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device operates as a 18-bit bus switch or a 9-bit bus exchanger, which allows data exchange between the four signal ports via the data-select terminals.

Features

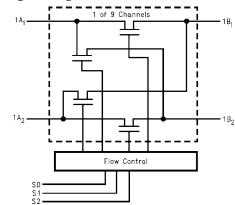
- \blacksquare 4 Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

Order Number	Package Number	Package Description
FST16209MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16209MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Truth Table

S2	S1	S0	A ₁	A ₂	Function
L	L	L	Z	Z	Disconnect
L	L	Н	B ₁	Z	$A_1 = B_1$
L	Н	L	B ₂	Z	$A_1 = B_2$
L	Н	Н	Z	B_1	$A_2 = B_1$
Н	L	L	Z	B_2	$A_2 = B_2$
Н	L	Н	Z	Z	Disconnect
Н	Н	L	B ₁	B_2	$A_1 = B_1, A_2 = B_2$
Н	Н	Н	B ₂	B_1	$A_1 = B_2, A_2 = B_1$

Connection Diagram



Pin Descriptions

Pin Name	Description
S2, S1, S0	Data-select inputs
A ₁ , A ₂	Bus A
B ₁ , B ₂	Bus B

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions (Note 3)

 $\begin{array}{ll} \mbox{Power Supply Operating (V_{CC})} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \end{array}$

Input Rise and Fall Time (t_r, t_f)

Switch Control Input 0nS/V to 5nS/V Switch I/O 0nS/V to DC Free Air Operating Temperature (T_A) -40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

		V _{CC} (V)	T _A	= -40 °C to +8	5 °C	Units	
Symbol	Parameter		Min	Typ (Note 4)	Max		Conditions
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18mA$
V _{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V _{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I _I	Input Leakage Current	5.5			±1.0	μΑ	$0 \le V_{IN} \le 5.5V$
		0			10	μΑ	$V_{IN} = 5.5V$
I _{OFF}	OFF-STATE Leakage Current	5.5			±1.0	μΑ	$0 \le A, B \le V_{CC}$
R _{ON}	Switch On Resistance	4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 64mA$
	(Note 5)	4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 30mA$
		4.5		8	12	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
		4.0		14	20	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
I _{CC}	Quiescent Supply Current	5.5			3	μА	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
ΔI _{CC}	Increase in I _{CC} per Input	5.5			2.5	mA	One input at 3.4V
							Other inputs at V _{CC} or GND

Note 4: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^{\circ}C$

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40$ °C to $+85$ °C, $C_L = 50$ pF, $R_U = R_D = 500\Omega$				Units	Conditions	Figure No.
Syllibol		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$		Units	Conditions	i iguie No.
		Min	Max	Min	Max			
t _{PHL} , t _{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V _I = OPEN	Figure 1 Figure 2
t _{PHL} , t _{PLH}	Prop Delay S to Bus	1.5	7.0		7.0	ns	V _I = OPEN	Figure 1 Figure 2
t _{PZH} , t _{PZL}	Output Enable Time, S to A or B	1.5	7.5		8.0	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figure 1 Figure 2
t _{PHZ} , t _{PLZ}	Output Disable Time S to A or B	1.0	8.5		9.0	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figure 1 Figure 2

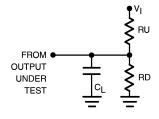
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control pin Input Capacitance	3		pF	V _{CC} = 5.0V
C _{I/O}	Input/Output Capacitance	10		pF	V _{CC} = 5.0V,
					S0, S1, and S2 = GND

Note 7: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

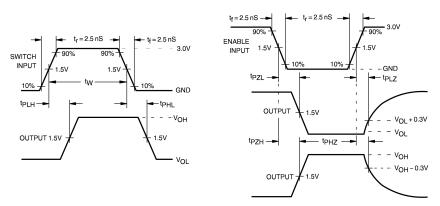
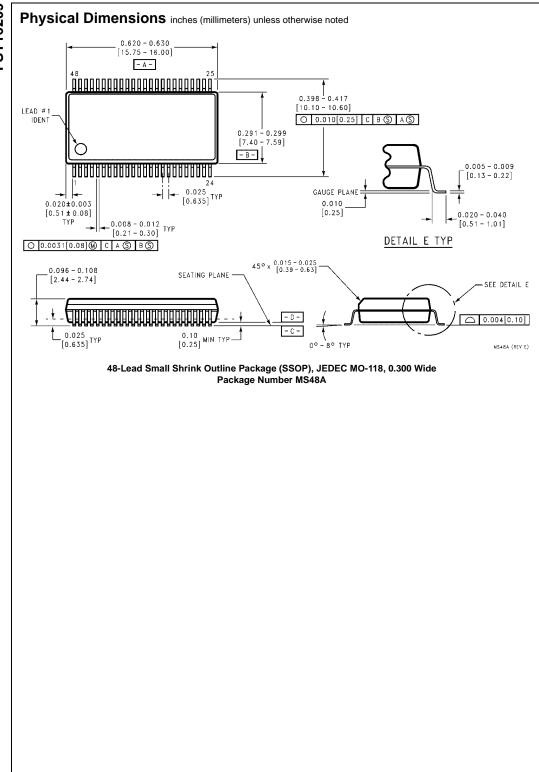


FIGURE 2. AC Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.40 TYP ĤAAAAĤ 9.20 8.10 -В-0.2 C B A PIN #1 IDENT - 0.30 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.50 Ф 0.13 W A BS CS - 12.00° TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS R0.16 NOTES: NOTES: A CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE 0.60±0.10

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Technology Description

MTD48RevB1

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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