FAN5090

Two Phase Interleaved Synchronous Buck Converter for VRM 9.x Applications

Features

- Programmable output from 1.10V to 1.85V in 25mV steps using an integrated 5-bit DAC
- Two interleaved synchronous phases for maximum performance
- 100nsec transient response time
- Built-in current sharing between phases
- Remote sense
- Programmable Active Droop™ (Voltage Positioning)
- Programmable switching frequency from 100KHz to 300KHz per phase
- Adaptive delay gate switching
- Integrated high-current gate drivers
- Integrated Power Good, OV, UV, Enable/Soft Start functions
- Drives N-channel MOSFETs
- Operation optimized for 12V operation
- Overcurrent protection using MOSFET sensing
- 24 pin TSSOP package

Applications

- Power supply for Pentium® IV
- Power supply for Athlon®
- VRM for Pentium IV processor
- Programmable step-down power supply

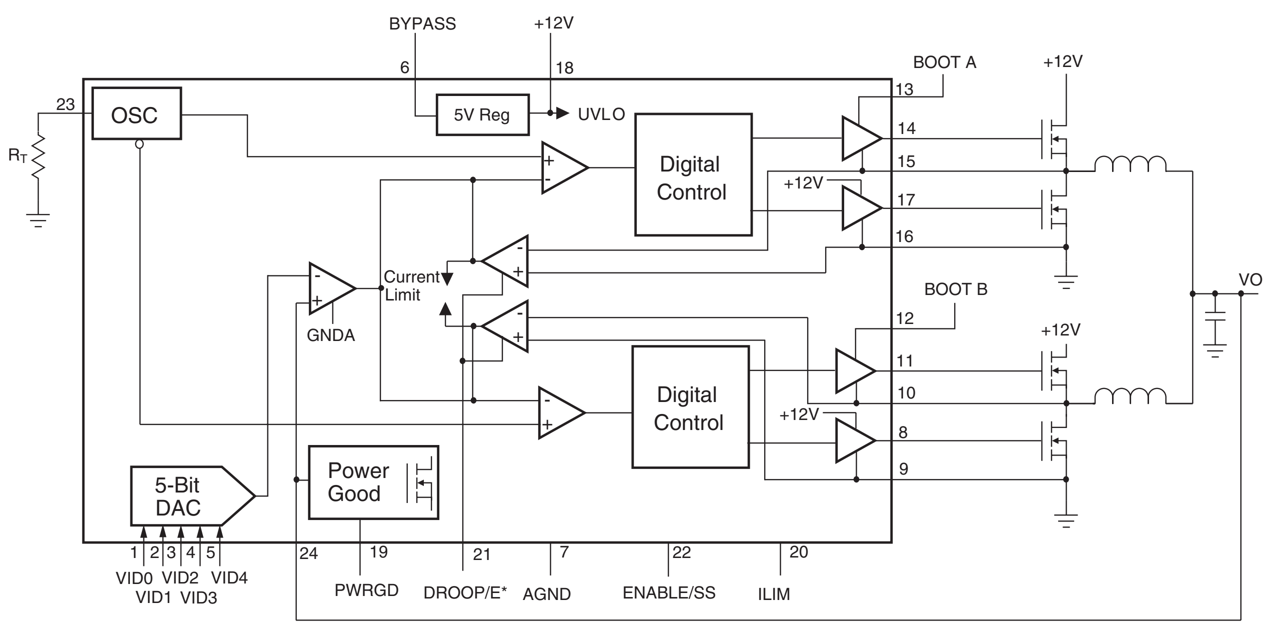
Description

The FAN5090 is a synchronous two-phase DC-DC controller IC which provides a highly accurate, programmable output voltage for VRM 9.x processors. Two interleaved synchronous buck regulator phases with built-in current sharing operate 180° out of phase to provide the fast transient response needed to satisfy high current applications while minimizing external components.

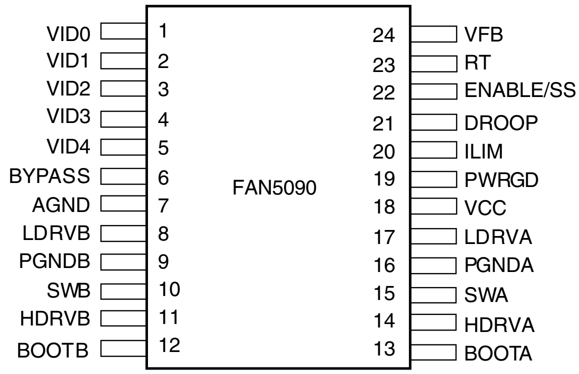
The FAN5090 features Programmable Active Droop™ for transient response with minimum output capacitance. It has integrated high-current gate drivers, with adaptive delay gate switching, eliminating the need for external drive devices. The FAN5090 uses a 5-bit D/A converter to program the output voltage from 1.10V to 1.85V in 25mV steps with an accuracy of 1%. The FAN5090 uses a high level of integration to deliver load currents in excess of 50A from a 12V source with minimal external circuitry.

The FAN5090 also offers integrated functions including Power Good, Output Enable/Soft Start, under-voltage lockout, over-voltage protection, and adjustable current limiting with independent current sense on each phase. It is available in a 24 pin TSSOP package.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1-5	VID0-4	**Voltage Identification Code Inputs.** Internally pulled-up open collector/TTL compatible inputs program the output voltage over range specified in Table 1.
6	BYPASS	**5V Rail.** Bypass this pin with a 0.1µF ceramic capacitor to AGND.
7	AGND	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
8	LDRVB	**Low Side FET Driver for B.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should optimally be <0.5".
9	PGNDB	**Power Ground B.** Return pin for high currents flowing in low-side MOSFET. Connect directly to low-side MOSFET source.
10	SWB	**High Side Driver Source and Low Side Driver Drain Switching Node B.** Gate drive return for high side MOSFET, and negative input for low-side MOSFET current sense.
11	HDRVB	**High Side FET Driver B.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should optimally be <0.5".
12	BOOTB	**Bootstrap B.** Input supply for high-side MOSFET.
13	BOOTA	**Bootstrap A.** Input supply for high-side MOSFET.
14	HDRVA	**High Side FET Driver A.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should optimally be <0.5".
15	SWA	**High Side Driver Source and Low Side Driver Drain Switching Node A.** Gate drive return for high side MOSFET, and negative input for low-side MOSFET current sense.
16	PGNDA	**Power Ground A.** Return pin for high currents flowing in low-side MOSFET. Connect directly to low-side MOSFET source.
17	LDRVA	**Low Side FET Driver for A.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should optimally be <0.5".
18	VCC	**VCC.** Internal IC supply. Connect to system 12V supply, and decouple with a 10Ω resistor and 1µF ceramic capacitor.
19	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is less than 350mV less than the nominal output voltage setpoint. Power Good is prevented from going low until the output voltage is out of spec for 500µsec.

Pin Number	Pin Name	Pin Function Description
20	ILIM	**Current Limit.** A resistor from this pin to ground sets the over current trip level.
21	DROOP	**Droop Control.** A resistor from this pin to ground sets the amount of droop by controlling the gain of the current sense amplifier.
22	ENABLE/SS	**Output Enable/Softstart.** A logic LOW on this pin will disable the output. An 10μA internal current source allows for open collector control. This pin also doubles as soft start.
23	RT	**Frequency Set.** A resistor from this pin to ground sets the switching frequency.
24	VFB	**Voltage Feedback.** Connect to the desired regulation point at the output of the converter.

Absolute Maximum Ratings (Absolute Maximum Ratings are the values beyond which the device may be damaged or have it's useful life impaired. Functional operation under these conditions is not implied.)

Parameter	Min.	Max.	Unit
Supply Voltage VCC		15	V
Supply Voltages BOOT to PGND		24	V
BOOT to SW		24	V
Voltage Identification Code Inputs, VID0-VID4		6	V
VFB, ENABLE/SS, PWRGD, DROOP		6	V
SWA, SWB to AGND (<1μs)	-3	15	V
PGNDA, PGNDB to AGND	-0.5	0.5	V
Gate Drive Current, peak pulse		3	A
Junction Temperature, T_J	-55	150	°C
Storage Temperature	-65	150	°C

Thermal Ratings

Parameter	Min.	Typ.	Max.	Unit
Lead Soldering Temperature, 10 seconds			300	°C
Power Dissipation, P_D			650	mW
Thermal Resistance Junction-to-Case, Θ_{JC}		16		°C/W
Thremal Resistance Junction-to-Ambient, Θ_{JA}		84		°C/W

Recommended Operating Conditions (See Figure 2)

Parameter	Conditions	Min.	Max.	Units
Output Driver Supply, BOOTA, B		16	22	V
Ambient Operating Temperature		0	70	°C
Supply Voltage V_{CC}		10.8	13.2	V

Electrical Specifications

(V_{CC} = 12V, VID = [01111] = 1.475V, and T_A = +25°C using circuit in Figure 2, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter		Conditions		Min.	Typ.	Max.	Units
Input Supply							
UVLO Hysteresis					1.0		V
12V UVLO		Rising Edge	•	8.5	9.5	10.3	V
12V Supply Current		PWM Output Open			15	20	mA
Internal Voltage Regulator							
BYPASS Voltage				4.75	5	5.25	V
BYPASS Capacitor				100			nF
VREF and DAC							
Output Voltage		See Table 1	•	1.100		1.850	V
Initial Voltage Setpoint[1]		I_{LOAD} = 0A, VID = [01111]		1.460	1.475	1.490	V
Output Temperature Drift		T_A = 0 to 70°C			5		mV
Line Regulation		V_{CC} = 11.4V to 12.6V	•		130		µV
Droop[2]		I_{LOAD} = 69A, R_{DROOP} = 13.3kΩ			56		mV
Programmable Droop Range				0		1.25	mΩ
Response Time		ΔV_{out} = 10mV			100		nsec
Current Mismatch		$R_{DS,on}$ (A) = $R_{DS,on}$ (B), I_{LOAD} = 69A Droop = 1mΩ			5		%
VID Inputs							
Input LOW current, VID pins		V_{VID} = 0.4V		-60			µA
VID V_{IH}				2.0			V
VID V_{IL}						0.8	V
Oscillator							
Oscillator Frequency		RT = 54.9KΩ	•	440	500	560	kHz
Oscillator Range		RT = 137KΩ to 46.4KΩ		200		600	kHz
Maximum Duty Cycle		RT = 137KΩ			90		%
Minimum LDRV on-time		RT = 46.4KΩ			330		nsec
Gate Drive							
Gate Drive On-Resistance		HS Source			5	6.5	Ω
		HS Sink			1.5	2	Ω
		LS Source			5	6.5	Ω
		LS Sink			1.5	2	Ω
Output Driver	Rise Time	See Figure 1, C_L = 3000pF			50		nsec
	Fall Time				25		nsec
Enable/Soft Start							
Soft Start Current					10		µA
Enable Threshold		ON OFF		1.0		 0.4	V
Power Good							
PWRGD Threshold		Logic LOW, $V_{VID} - V_{PWRGD}$	•	85	88	92	%V_{OUT}
PWRGD Output Voltage		I_{sink} = 4mA				0.4	V
PWRGD Delay		High → Low			500		µsec

Electrical Specifications (continued)

(V_{CC} = 12V, VID = [01111] = 1.475V, and T_A = +25°C using circuit in Figure 2, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
OVP and OTP						
Output Overvoltage Detect		•	2.1	2.2	2.3	V
Over Temperature Shutdown			130	140	150	°C
Over Temperature Hysteresis				40		°C

Notes:

1. As measured at the VFB (pin 24) sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
2. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with VRM 9.x specification.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
1	1	1	1	1	OFF
1	1	1	1	0	1.100V
1	1	1	0	1	1.125V
1	1	1	0	0	1.150V
1	1	0	1	1	1.175V
1	1	0	1	0	1.200V
1	1	0	0	1	1.225V
1	1	0	0	0	1.250V
1	0	1	1	1	1.275V
1	0	1	1	0	1.300V
1	0	1	0	1	1.325V
1	0	1	0	0	1.350V
1	0	0	1	1	1.375V
1	0	0	1	0	1.400V
1	0	0	0	1	1.425V
1	0	0	0	0	1.450V
0	1	1	1	1	1.475V
0	1	1	1	0	1.500V
0	1	1	0	1	1.525V
0	1	1	0	0	1.550V
0	1	0	1	1	1.575V
0	1	0	1	0	1.600V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

Note:

1. 0 = VID pin is tied to GND.
   1 = VID pin is pulled up internally to 5V.

Gate Drive Test Circuit

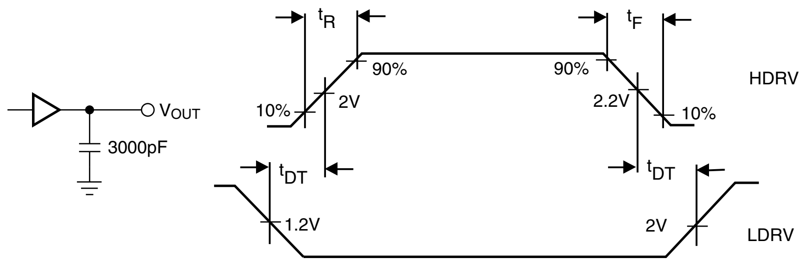
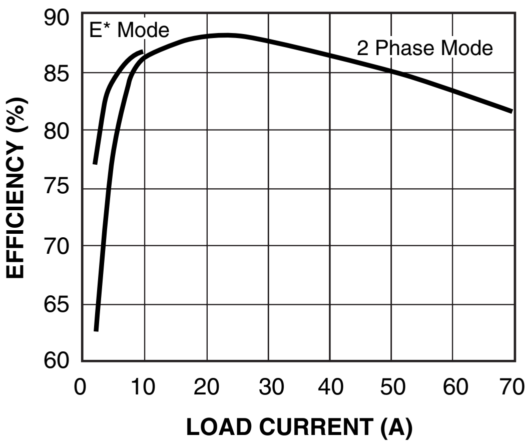


Figure 1. Output Drive Timing Diagram

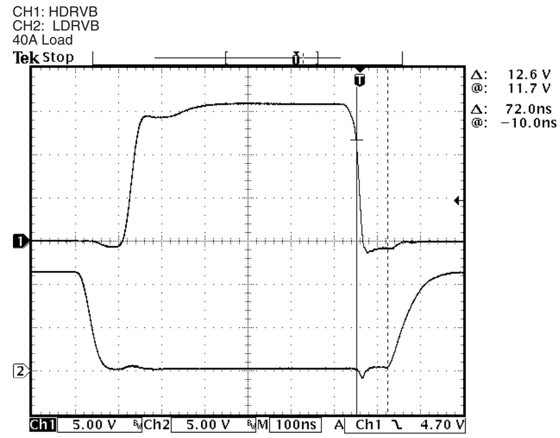
Typical Operating Characteristics

(V_{CC} = 12V, V_{OUT} = 1.475V, and T_A = +25°C using circuit in Figure 2, unless otherwise noted.)

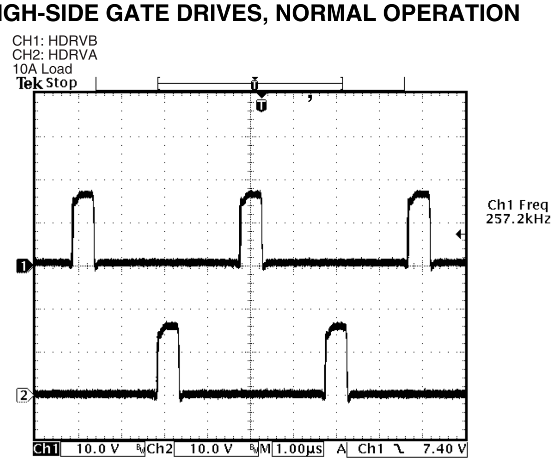
EFFICIENCY VS. OUTPUT CURRENT



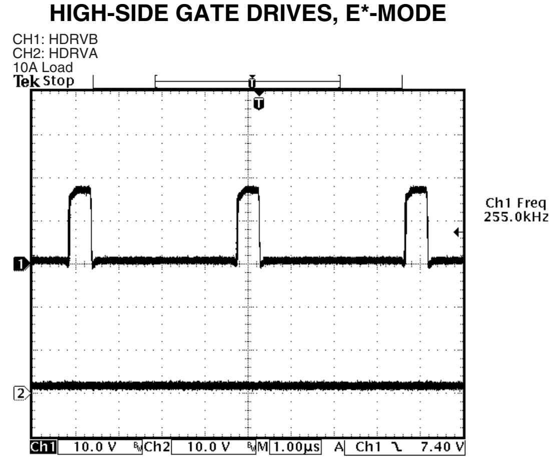
ADAPTIVE GATE DELAY



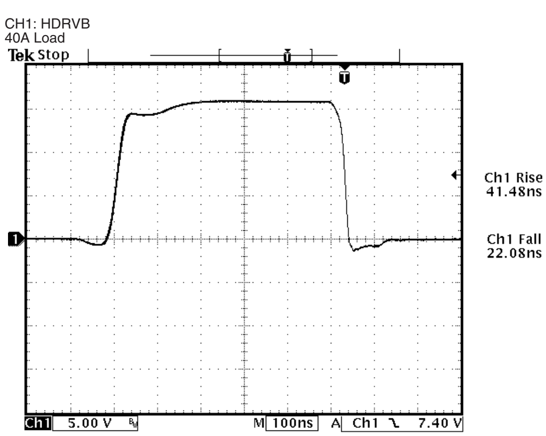
HIGH-SIDE GATE DRIVES, NORMAL OPERATION



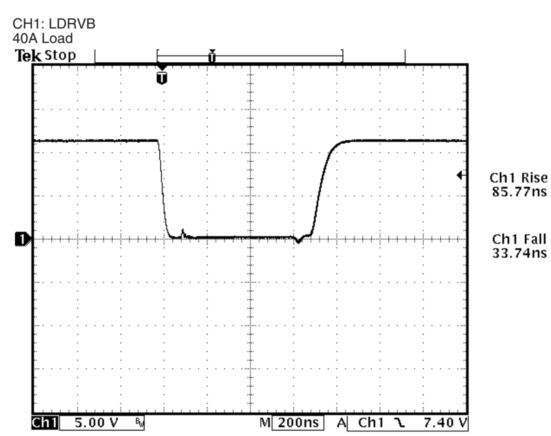
HIGH-SIDE GATE DRIVES, E*-MODE



HIGH-SIDE GATE DRIVES, RISE / FALL TIME



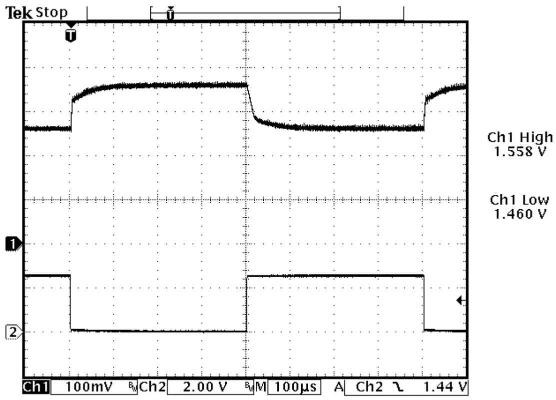
LOW-SIDE GATE DRIVES, RISE / FALL TIME



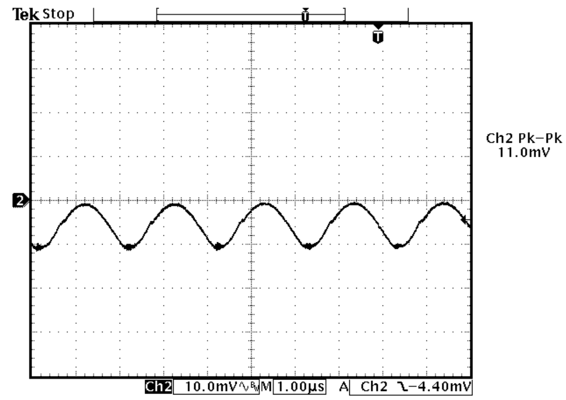
Typical Operating Characteristics (Continued)

DYNAMIC VID CHANGE (1.475–1.575V)

CH1: V_{OUT} (1.20V Offset)
CH2: VID2
40A Load

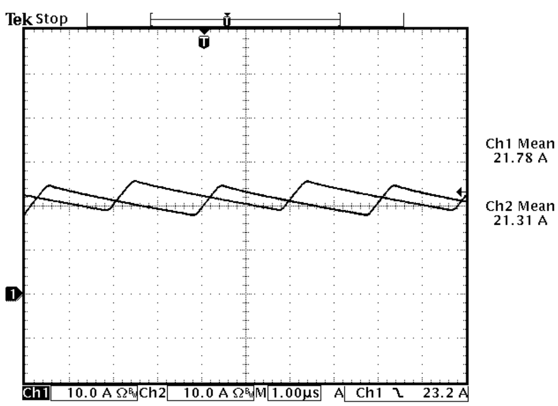


OUTPUT RIPPLE, 60A LOAD



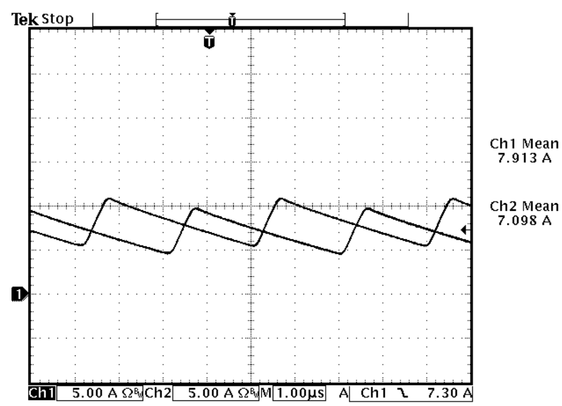
CURRENT SHARING, 50A LOAD

CH1: I_{LB}
CH2: I_{LA}



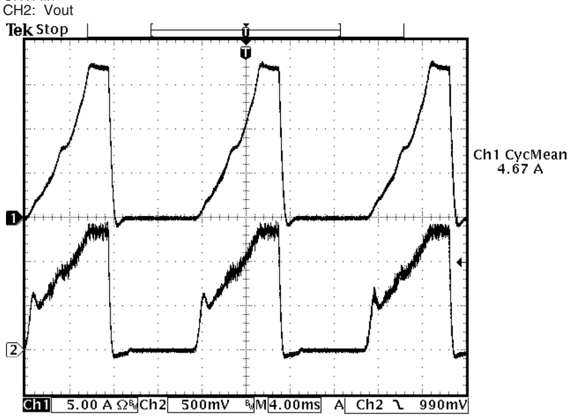
CURRENT SHARING, 15A LOAD

CH1: I_{LA}
CH2: I_{LB}

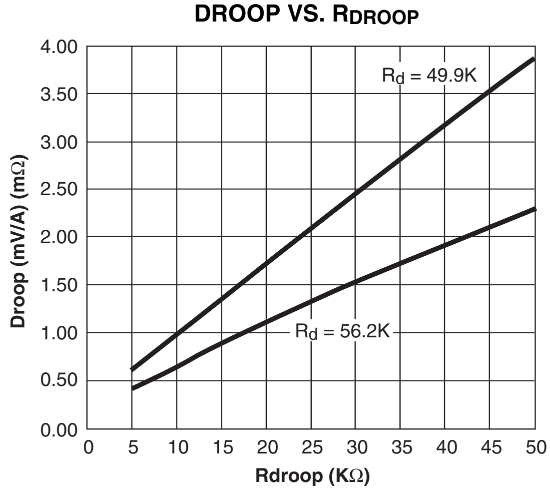


CURRENT LIMIT

CH1: Iin
CH2: Vout

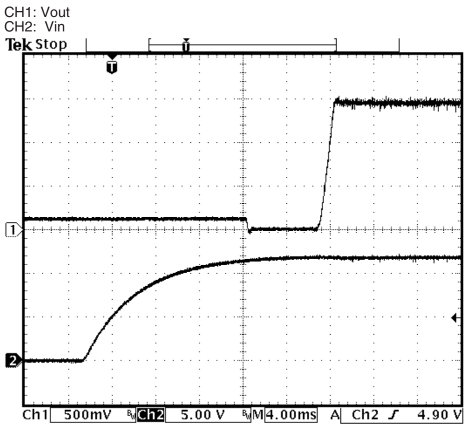


DROOP VS. R_{DROOP}

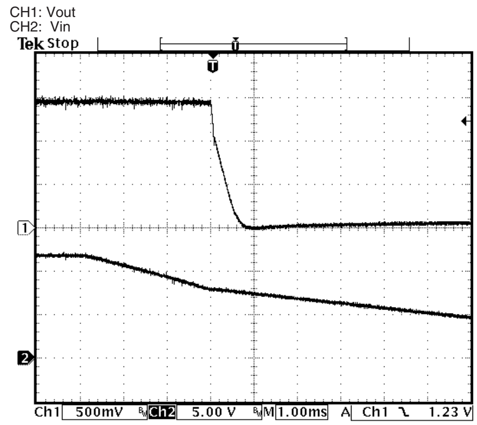


Typical Operating Characteristics (Continued)

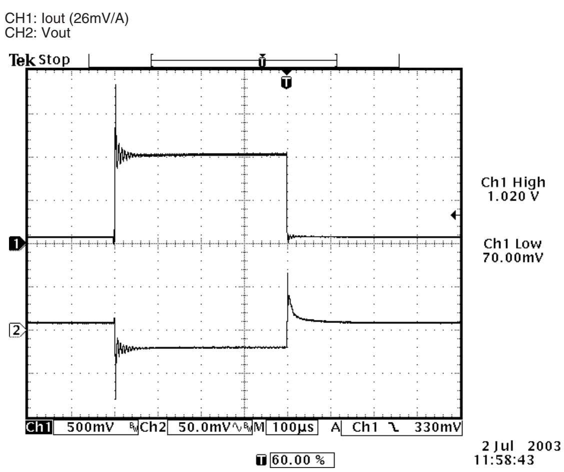
START-UP, 40A LOAD



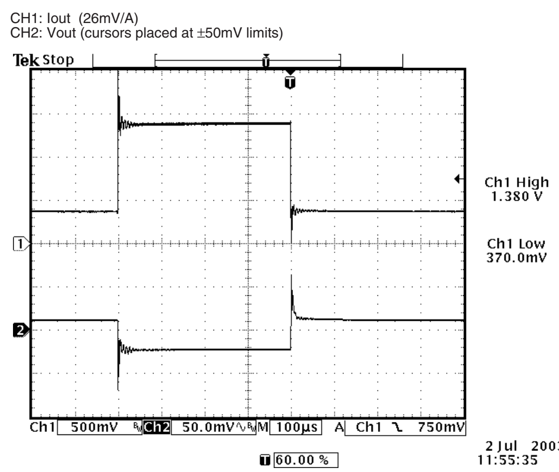
POWER-DOWN, 40A LOAD



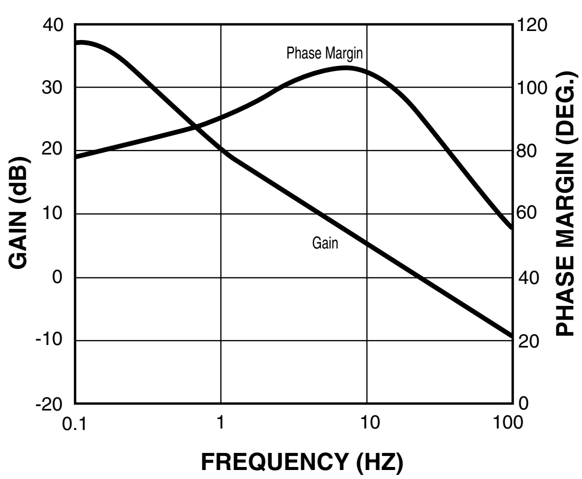
LOAD TRANSIENT, 0-40A



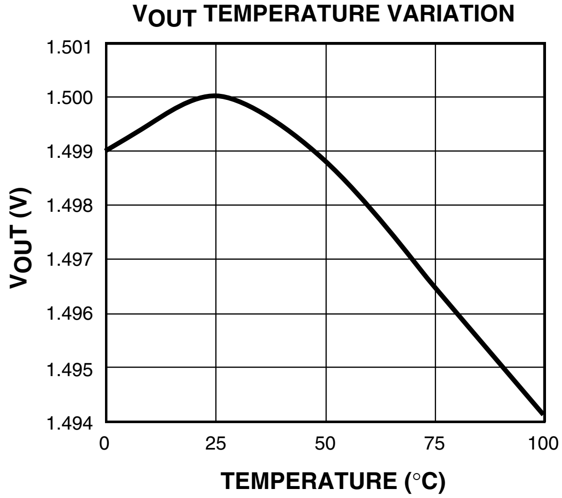
LOAD TRANSIENT, 12-52A



CLOSED LOOP RESPONSE



V_{OUT} TEMPERATURE VARIATION



Application Circuit

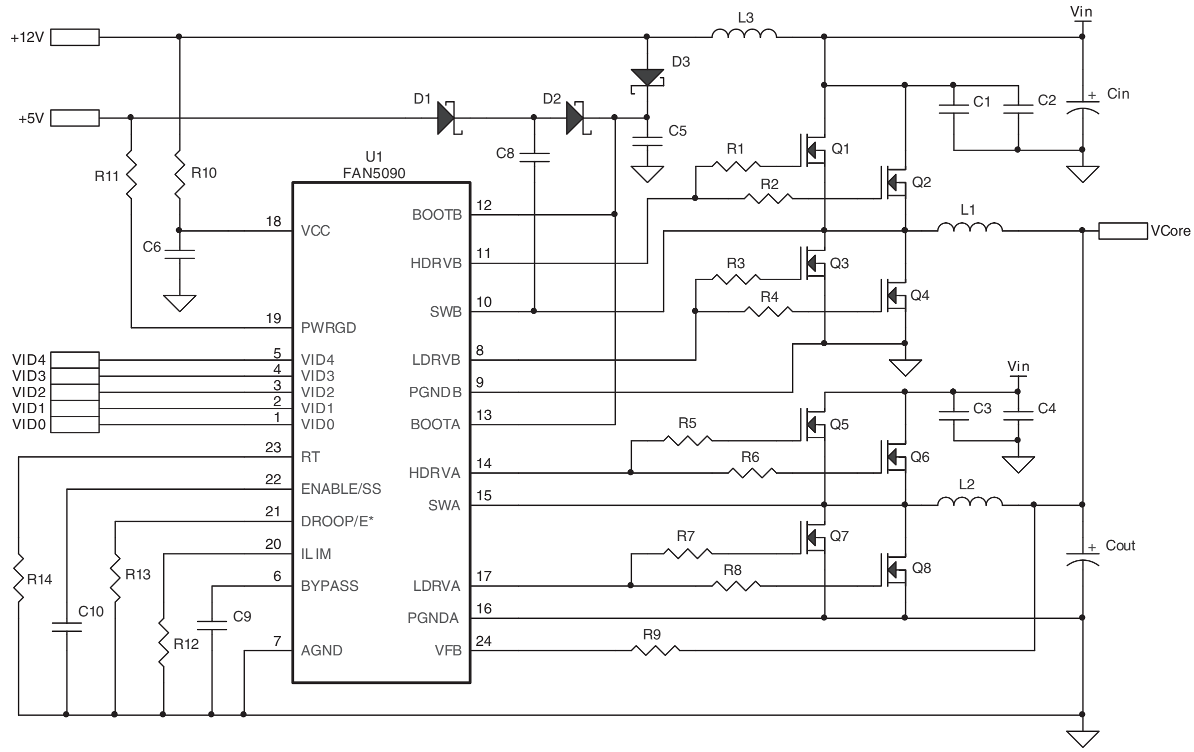


Figure 2. Application Circuit for 70A VRM 9.x Desktop Application

Table 2. FAN5090 Application Bill of Materials for Figure 2

Reference	QTY	Description	Manufacturer / Number
U1	1	FAN5090	Fairchild FAN5090
Q1-Q8	8	MOSFET, Nch, 30V, 50A, 9mΩ	Fairchild FDD6296
D1, 2, 3	3	SCHOTTKY, 40V, 500mA	Fairchild MBR0540
L1, 2	2	850nH, 30A, 0.9mΩ	Inter-Technical SCTA5022A-R86K
L3	1	630nH, 15A, 1.7mΩ	Inter-Technical AK1418160052-R63M
R1, 2, 5, 6	4	2.2Ω, 5%	
R3, 4, 7, 8, 9	5	4.7Ω, 5%	
R10	1	10Ω, 5%	
R11	1	10K, 5%	
R12	1	68.1K, 1%	
R13	1	15.0K, 1%	
R14	1	56.2K, 1%	
C1-6	6	1.0µf, 25V, 10%, X7R	
C8-10	3	0.1µf, 16V, 10%, X7R	
Cin	3	1500µf, 16V, 20%,12mΩ	Rubycon 16MBZ1500M
Cout	7	2200µf, 6.3V, 20%, 12mΩ	Rubycon 6.3MBZ2200M

Application Information

Operation

The FAN5090 Controller

The FAN5090 is a programmable synchronous two-phase DC-DC controller IC. When designed with the appropriate external components, the FAN5090 can be configured to deliver more than 50A of output current, for VRM 9.x applications. The FAN5090 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the FAN5090 Block Diagram on page 1. The FAN5090 consists of two interleaved synchronous buck converters, implemented with summing-mode control. Each phase has its own current feedback, and there is a common voltage feedback.

The two buck converters controlled by the FAN5090 are interleaved, that is, they run 180° out-of-phase. This minimizes the RMS input ripple current, minimizing the number of input capacitors required. It also doubles the effective switching frequency, improving transient response.

The FAN5090 implements "summing mode control", which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads and external components. No external compensation is required.

The regulator's control loop contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts inputs from a current sensor and a voltage sensor, with the voltage sensor being common to both phases, and the current sensor separate for each. The voltage sensor amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to each of the two comparators. The current control path for each phase takes the difference between its PGND and SW pins when the low-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; It presents the resulting signal to the same input of its summing amplifier, adding its signal to the voltage amplifier's with a certain gain. These two signals are thus summed together. This sum is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block. The oscillator ramps are 180° out-of-phase with each other, so that the two phases are on alternately.

The digital control block takes the analog comparator input to provide the appropriate pulses to the HDRV and LDRV output pins for each phase. These outputs control the external power MOSFETs.

Response Time

The FAN5090 utilizes leading-edge, not trailing-edge control. Conventional trailing-edge control turns on the high-side MOSFET at a clock signal, and then turns it off when the error amplifier output voltage is equal to the ramp voltage. As a result, the response time of a trailing-edge converter can be as long as the off-time of the high-side driver, nearly an entire switching period. The FAN5090's leading-edge control turns the high-side MOSFET on when the error amplifier output voltage is equal to the ramp voltage, and turns it off at the clock signal. As a result, when a transient occurs, the FAN5090 responds immediately by turning on the high-side MOSFET. Response time is set by the internal propagation delays, typically 100nsec. In worst case, the response time is set by the minimum on-time of the low-side MOSFET, 330nsec.

Oscillator

The FAN5090 oscillator section runs at a frequency determined by a resistor from the RT pin to ground according to the formula

$$R_T(\Omega) = \frac{27.5 \bullet 10^9}{f(Hz)}$$

The oscillator generates two internal sawtooth ramps, each at one-half the oscillator frequency, and running 180° out of phase with each other. These ramps cause the turn-on time of the two phases to be phased apart. The oscillator frequency of the FAN5090 can be programmed from 200kHz to 600kHz with each phase running at 100kHz to 300kHz, respectively. Frequency selection depends on various system performance criteria, with higher frequency resulting in smaller components but lower efficiency.

Quiescent current (Icc) of the FAN5090 is also frequency dependent:

$$Icc = 12.7 + 0.006\,[(f/2) - 100] \quad mA$$

Where f is the oscillator frequency in KHz

Remote Voltage Sense

The FAN5090 has true remote voltage sense capability, eliminating errors due to trace resistance. To utilize remote sense, the VFB and AGND pins should be connected as a Kelvin trace pair to the point of regulation, such as the processor pins. The converter will maintain the voltage in regulation at that point. Care is required in layout of these grounds; see the layout guidelines in this datasheet.

High Current Output Drivers

The FAN5090 contains four high current output drivers that utilize MOSFETs in a push-pull configuration. The drivers for the high-side MOSFETs use the BOOT pin for input power and the SW pin for return. The drivers for the low-side MOSFETs use the VCC pin for input power and the PGND pin for return. Typically, the BOOT pin will use a charge pump as shown in Figure 2. Note that the BOOT and VCC pins are separated from the chip's internal power and ground, BYPASS and AGND, for switching noise immunity.

Adaptive Delay Gate Drive

The FAN5090 embodies an advanced design that ensures minimum MOSFET transition times while eliminating shoot-through current. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure that they are never on simultaneously. When the high-side MOSFET turns off, the voltage on its source begins to fall. When the voltage there reaches approximately 2.2V, the low-side MOSFETs gate drive is applied. When the low-side MOSFET turns off, the voltage at the LDRV pin is sensed. When it drops below approximately 1.2V, the high-side MOSFET's gate drive is applied with 50ns delay.

Maximum Duty Cycle

In order to ensure that the current-sensing and charge-pumping work, the FAN5090 guarantees that the low-side MOSFET will be on a certain portion of each period. For low frequencies, this occurs as a maximum duty cycle of approximately 90%. Thus at 250KHz, with a period of 4μsec, the low-side will be on at least 4μsec • 10% = 400nsec. At higher frequencies, this time might fall so low as to be ineffective. The FAN5090 provides a minimum low-side on-time of approximately 330nsec, regardless of duty cycle.

Current Sensing

The FAN5090 has two independent current sensors, one for each phase. Current sensing is accomplished by measuring the source-to-drain voltage of the low-side MOSFET during its on-time. Each phase has its own power ground pin, to permit the phases to be placed in different locations without affecting measurement accuracy. For best results, it is important to connect the PGND and SW pins for each phase as a Kelvin trace pair directly to the source and drain, respectively, of the appropriate low-side MOSFET. Care is required in the layout of these grounds; see the layout guidelines in this datasheet.

Current Sharing

The two independent current sensors of the FAN5090 operate with their independent current control loops to guarantee that the two phases each deliver half of the total output current. Mismatch between the two phases occurs only if there is a mismatch between the R_{DSon} of the low-side MOSFETs.

Short Circuit Current Characteristics (ILIM pin)

The FAN5090 short circuit current characteristic includes a function that protects the DC-DC converter from damage in the event of a short circuit. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S(\Omega) = I_{SC} \bullet R_{DS,on} \bullet R_T \bullet 3.33$$

with I_{SC} the desired output current limit, R_T the oscillator resistor and R_{DSon} one phase's low-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFETs' R_{DSon}.

Important Note! The oscillator frequency must be selected before selecting the current limit resistor, because the value of RT is used in the calculation of R_S.

When an overcurrent is detected, the high-side MOSFETs are turned off, and the low-side MOSFETs are turned on, and they remain in this state until the measured current through the low-side MOSFET has returned to zero amps. After reaching zero, the FAN5090 soft-starts, ensuring that it can also safely turn on into a faulted load.

A limitation on the current sense circuit is that $I_{SC} \bullet R_{DS,on}$ must be less that 375mV. To ensure correct operation, use $I_{SC} \bullet R_{DS,on} \leq 300$mV; between 300mV and 375mV. There will be some non-linearity in the short-circuit current that is not accounted for in the equation.

As an example, consider the typical characteristics of the circuit using two FDD6696 low-side MOSFETs (8mΩ @ 25°C, 10.4mΩ @ 95°C, each), R_T = 56.2K, and R_S = 75K:

The converter maintains a normal load regulation characteristic until the voltage across the MOSFETs exceeds the internal short circuit threshold of 75K / (3.33 x 56.2K x 5.2mΩ) = 77A. At this point, the internal comparator trips and signals the controller to leave on the low-side MOSFETs and keep off the high-side MOSFETs. The inductor current decreases, and power is not applied again until inductor current reaches 0A and the converter attempts a new soft-start cycle.

Internal Voltage Reference

The reference included in the FAN5090 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4, and scales the reference voltage from 1.100V to 1.850V in 25mV steps.

BYPASS Reference

The internal logic of the FAN5090 runs on 5V. To permit the IC to run with 12V only, it produces 5V internally with a linear regulator, whose output is present on the BYPASS pin. This pin should be bypassed with a 100nF capacitor for noise suppression. The BYPASS pin should not have any external load attached to it.

Dynamic Voltage Adjustment

The FAN5090 can have its output voltage dynamically adjusted to accommodate low power modes. The designer must ensure that the transitions on the VID lines all occur simultaneously (within less than 500nsec) to avoid false codes generating undesired output voltages. The Power Good flag tracks the VID codes, but has a 500µsec delay transitioning from high to low; long enough to ensure that there will not be any glitches during dynamic voltage adjustment.

Power Good (PWRGD)

The FAN5090 Power Good function is designed in accordance with the Pentium IV DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than -12% of its nominal setpoint. The Power Good flag provides no control functions to the FAN5090.

Output Enable/Soft Start (ENABLE/SS)

The FAN5090 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have an attached capacitor (typically 100nF) to soft-start the switching. A softstart capacitor may be chosen by the formula:

$$t_D = \frac{C_{SS}}{10\mu A} \bullet \frac{(1.7 + 0.9074 \bullet V_{OUT})}{2.5}$$

where: t_D is the delay time before the output starts to ramp

$$t_R = \frac{C_{SS}}{10\mu A} \bullet \frac{V_{OUT} \bullet 0.9}{V_{IN}}$$

t_R is the ramp time of the output
C_{SS} = softstart cap
V_{OUT} = nominal output voltage

However, C must be ≥ 100nF.

Programmable Active Droop™

The FAN5090 features Programmable Active Droop™: As the output current increases, the output voltage drops proportionately an amount programmed by an external resistor. This feature allows maximum headroom for transient response of the converter. The current is sensed losslessly by measuring the voltage across the low-side MOSFET during its on time. Consult the section on current sensing for details. The droop is adjusted by the droop resistor changing the gain of the current loop. Note that this method makes the droop dependent on the temperature and initial tolerance of the MOSFET, and the droop must be calculated taking account of these tolerances. Given a maximum output current, the amount of droop can be programmed with a resistor to ground on the droop pin, according to the formula:

$$R_{Droop}(\Omega) = \frac{V_{Droop} \bullet R_T}{I_{max} \bullet R_{DS,on}}$$

with V_{Droop} the desired droop voltage, R_T the oscillator resistor, I_{max} the output current at which the droop is desired, and R_{DSon} the on-state resistance of one phase's low-side MOSFET.

Important Note! The oscillator frequency must be selected before selecting the droop resistor, because the value of R_T is used in the calculation of R_{Droop}.

Over-Voltage Protection

The FAN5090 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds 2.2V, an over-voltage condition is assumed and the FAN5090 latches on the external low-side MOSFET and latches off the high-side MOSFET. The DC-DC converter returns to normal operation only after V_{CC} has been recycled.

Over Temperature Protection

If the FAN5090 die temperature exceeds approximately 150°C, the IC shuts itself off. It remains off until the temperature has dropped approximately 25°C, before it resumes normal operation.

E* Mode

Further enhancements in light-load efficiency can be obtained by operating the FAN5090 in E* mode. When the DROOP pin is pulled to the 5V BYPASS voltage, the "A" phase of the FAN5090 is completely turned off, reducing the consumed gate charge power by half. E* mode can be implemented using the circuit shown in figure 3.

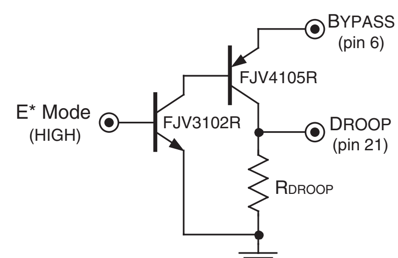


Figure 3. Implementing E* Mode Control

Note: The HDRV charge pump should be connected to "Phase B" of the FAN5093 circuit.

Component Selection

MOSFET Selection

This application requires N-channel Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Drain-Source On-Resistance,
- $R_{DS,ON} < 10m\Omega$ (lower is better);
- Power package with low Thermal Resistance;
- Drain-Source voltage rating > 15V;
- Low gate charge, especially for higher frequency operation.

For the low-side MOSFET, the on-resistance ($R_{DS,ON}$) is the primary parameter for selection. Because of the small duty cycle of the high-side, the on-resistance determines the power dissipation in the low-side MOSFET and therefore significantly affects the efficiency of the DC-DC converter. For high current applications, it may be necessary to use two MOSFETs in parallel for the low-side for each phase.

For the high-side MOSFET, the gate charge is as important as the on-resistance, especially with a 12V input and with higher switching frequencies. This is because the speed of the transition greatly affects the power dissipation. It may be a good trade-off to select a MOSFET with a somewhat higher $R_{DS,on}$, if by so doing a much smaller gate charge is available. For high current applications, it may be necessary to use two MOSFETs in parallel for the high-side for each phase.

At the FAN5090's highest operating frequencies, it may be necessary to limit the total gate charge of both the high-side and low-side MOSFETs together, to avert excess power dissipation in the IC.

Gate Resistors

Use of a gate resistor on some MOSFETs may be required. The gate resistor prevents high-frequency oscillations caused by the trace inductance ringing with the MOSFET gate capacitance. The gate resistors should be located physically as close to the MOSFET gate as possible.

The gate resistor also limits the power dissipation inside the IC, which could otherwise be a limiting factor on the switching frequency. It may thus carry significant power, especially at higher frequencies. As an example: The FDB7045L has a maximum gate charge of 70nC at 5V, and an input capacitance of 5.4nF. The total energy used in powering the gate during one cycle is the energy needed to get it up to 5V, plus the energy to get it up to 12V:

$$E = QV + \frac{1}{2}C \bullet \Delta V^2 = 70nC \bullet 5V + \frac{1}{2}5.4nF \bullet (12V - 5V)^2$$
$$= 482nJ$$

This power is dissipated every cycle, and is divided between the internal resistance of the FAN5090 gate driver and the gate resistor. Thus,

$$P_{Rgate} = \frac{E \bullet f \bullet R_{gate}}{(R_{gate} + R_{internal})} = 482nJ \bullet 300KHz \bullet \frac{4.7\Omega}{4.7\Omega + 0.5\Omega} = 131mW$$

and each gate resistor thus requires a 1/4W resistor to ensure worst case power dissipation.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. A smaller inductor produces greater ripple while producing better transient response. In any case, the minimum inductance is determined by the allowable ripple. The first order equation (close approximation) for minimum inductance for a two-phase converter is:

$$L_{min} = \frac{V_{in} - 2 \bullet V_{out}}{f} \bullet \frac{V_{out}}{V_{in}} \bullet \frac{ESR}{V_{ripple}}$$

where:
Vin = Input Power Supply
Vout = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
Vripple = Maximum peak to peak output ripple voltage budget.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance. For most converters, the transient response and the output ripple voltage determines the number of capacitors. Selection is typically dominated by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

For higher frequency applications, particularly those running the FAN5090 oscillator at >1MHz, Oscon or ceramic capacitors may be considered. They have much smaller ESR than comparable electrolytics, but also much smaller capacitance.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system main supply and the converter input as shown in Figure 2. This inductor serves to isolate the main supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up.

It is necessary to have some low ESR capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Because of the interleaving, the number of such capacitors required is greatly reduced from that required for a single-phase buck converter. Figure 2 shows 3 x 1500µF, but the exact number required will vary with the output voltage and current, according to the formula

$$I_{rms} = \frac{I_{out}}{2}\sqrt{2D - 4D^2}$$

for the two phase FAN5090, where D is the duty cycle (Vout / Vin). Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the FAN5090 is critical. Place the MOSFETs so that the trace length of the HDRV and LDRV pins of the FAN5090 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the FAN5090. That is, traces that connect to pins LDRV, HDRV, SW, BOOT, and PGND should be kept far away from the traces that connect to pins 1 through 7, and pins 18-24.
- Place the decoupling capacitors as close to the FAN5090 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each power and ground pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky of a given phase as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. Placing a 1.0µF decoupling cap directly on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the FAN5090 along with the PCAD layout Gerber file and silk screen can be obtained through your local Fairchild representative.

FAN5090 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the FAN5090. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please contact your local Fairchild representative for an evaluation board.

Additional Information

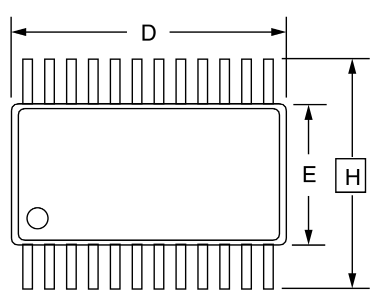
For additional information contact your local Fairchild representative.

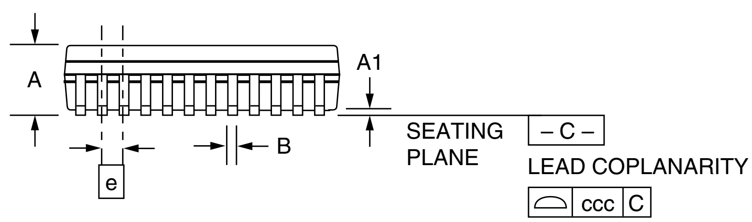
Mechanical Dimensions – 24 Lead TSSOP

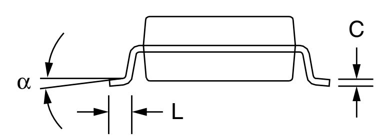
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.047	—	1.20	
A1	.002	.006	0.05	0.15	
B	.007	.012	0.19	0.30	
C	.004	.008	0.09	0.20	
D	.303	.316	7.70	7.90	2
E	.169	.177	4.30	4.50	2
e	.026 BSC		0.65 BSC		
H	.252 BSC		6.40 BSC		
L	.018	.030	0.45	0.75	3
N	24		24		5
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Description	Package
FAN5090MTC	VRM 9.x DC-DC Controller	24 pin TSSOP
FAN5090MTCX	VRM 9.x DC-DC Controller	24 pin TSSOP in Tape and Reel

9/16/03 0.0m 005
Stock#DS30005090