

August 1991 Revised December 1999

#### 74AC05

# **Hex Inverter with Open Drain Outputs**

#### **General Description**

The AC05 contains six inverters.

#### **Features**

- Outputs sink 24 mA
- Open drain for wired NOR function
- Radiation tolerant FACT<sup>™</sup> process

# **Ordering Code:**

Order Number	Package Number	Package Description
74AC05SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body

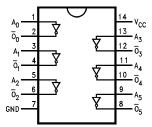
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### **Logic Symbol**

# A<sub>0</sub> 1 $\overline{0}_0$ A<sub>1</sub> $\overline{0}_1$ A<sub>2</sub> $\overline{0}_2$ A<sub>3</sub> $\overline{0}_3$ A<sub>4</sub> $\overline{0}_4$ A<sub>5</sub> $\overline{0}_5$

IEEE/IEC

## **Connection Diagram**



## **Pin Descriptions**

Pin Names	Description		
A <sub>n</sub>	Inputs		
$\overline{O}_n$	Outputs		

FACT™ is a trademark of Fairchild Semiconductor Corporation.

#### Absolute Maximum Ratings(Note 1)

 $V_1 = -0.5V$  -20 mA  $V_1 = V_{CC} + 0.5V$  +20 mA

DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> + 0.5V

DC Output Diode Current (I<sub>OK</sub>)

 $V_{O} = -0.5V$  -20 mA  $V_{O} = V_{CC} + 0.5V$  +20 mA

DC Output Voltage ( $V_O$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source

or Sink Current ( $I_O$ )  $\pm$  50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm$  50 mA

Storage Temperature (T  $_{\rm STG}$ )  $-65^{\circ}{\rm C}$  to +150  $^{\circ}{\rm C}$ 

# Recommended Operating Conditions

Minimum Input Edge Rate  $(\Delta V/\Delta t)$ 

 $V_{\mbox{\scriptsize IN}}$  from 30% to 70% of  $V_{\mbox{\scriptsize CC}}$ 

 $V_{CC} @ 3.3V, 4.5V, 5.5V$  125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

#### **DC Electrical Characteristics**

Symbol	Parameter			$+25^{\circ}$ C $T_A = -40^{\circ}$ C to $+85^{\circ}$ C		Units	Conditions	
Syllibol				aranteed Limits	Ullis			
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	1.65	1.65			
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		0.32	0.44		$I_{OL} = 12 \text{ mA}$	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)	
I <sub>IN</sub> (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$ , GND	
I <sub>OHD</sub>	Off-State Current	5.5		+0.5	+10.0	μΑ	$V_{IN} = V_{CC}$	
I <sub>OLD</sub>	Minimum Dynamic	5.5	E E	50	75	mA	V - 1 65V Mov	
	Output Current (Note 3)	5.5		30	/5	IIIA	V <sub>OLD</sub> = 1.65V Max	
I <sub>CC</sub> (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	20.0	μΑ	$V_{IN} = V_{CC}$ or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time

Note 4:  $I_{\text{IN}}$  and  $I_{\text{CC}} @ 3.0 \text{V}$  are guaranteed to be less than or equal to the respective limit @ 5.5 V  $V_{\text{CC}}$ .

# **AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	$T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$		T <sub>A</sub> = -40°C to +85°C		Units
		(Note 5)	Min	Max	Min	Min	
t <sub>PLZ</sub>	Propagation Delay	3.3	2.0	14.5	2.0	14.5	
	(Note 6)	5.0	2.0	14.0	2.0	14.0	ns
t <sub>PZL</sub>	Propagation Delay	3.3	2.0	6.5	2.0	6.5	ns
		5.0	2.0	5.0	2.0	5.0	115

Note 5: Voltage Range 3.3 is  $3.3V \pm 0.3V$ Voltage Range 5.0 is  $5.0V \pm 0.5V$ 

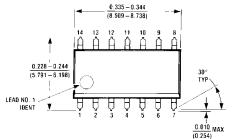
Note 6: AC Load is  $V_{CC} \times 2$ ,  $R_L = 1 \text{ k}\Omega$ 

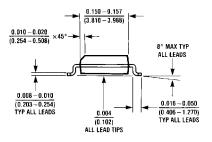
 $C_{L} = 50 \text{ pF}$ 

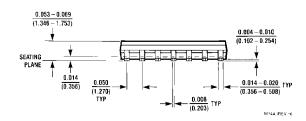
# Capacitance

Symbol	Symbol Parameter		Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	30.0	pF	V <sub>CC</sub> = 5.0V

# Physical Dimensions inches (millimeters) unless otherwise noted







14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com