



DS1977 32KB EEPROM iButton

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General Description

The DS1977 is a 32Kbyte EEPROM in a rugged, iButton enclosure. Access to the memory can be password-protected with different passwords for read-only and full access. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. Every DS1977 is factory-lasered with a guaranteed unique 64-bit registration number that allows for absolute trace-ability. The durable stainless steel iButton package is highly resistant to environmental hazards such as dirt and shock. Accessories permit the DS1977 iButton to be mounted on almost any object, including containers, pallets and bags.

Applications

- Maintenance and Inspection of equipment
- Medical Information / Health
- Data Shuttle for Fleet Management and Vending applications

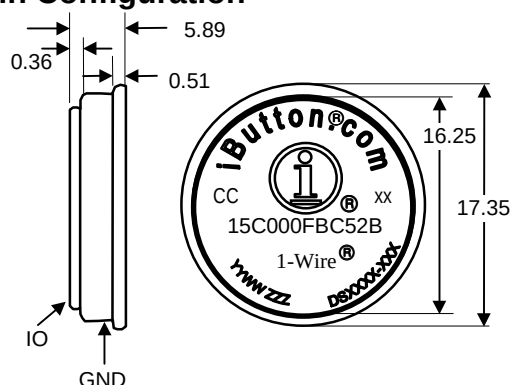
Ordering Information

Part	Temp Range	Pin-Pkg
DS1977-F5	-40 to 85°C	F5 iButton

Features

- 32KB EEPROM memory
- Durable, stainless-steel iButton package
- Built-in multi-drop controller ensures compatibility with other Dallas Semiconductor 1-Wire net products
- Unique factory lasered 64-bit registration number assures error free device selection and absolute part identity
- Supports Overdrive mode
- Operating range: 2.8V to 5.25V, -40 to +85°C

Pin Configuration



F5 iButton

ROM ID field

Like all 1-Wire devices, the DS1977 has a 64-bit lasered ROM identification field. The Family code of the DS1977 in the 64-bit ROM is to be assigned.

Figure 1. 64-BIT LASERED ROM

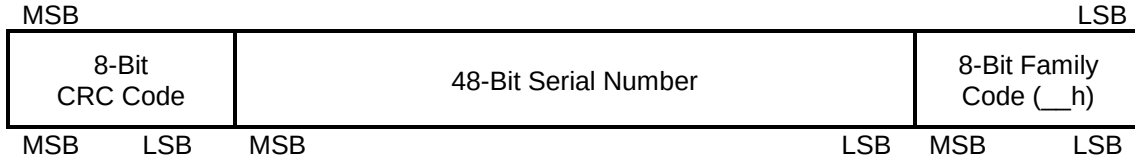


Figure 2. Command Hierarchy

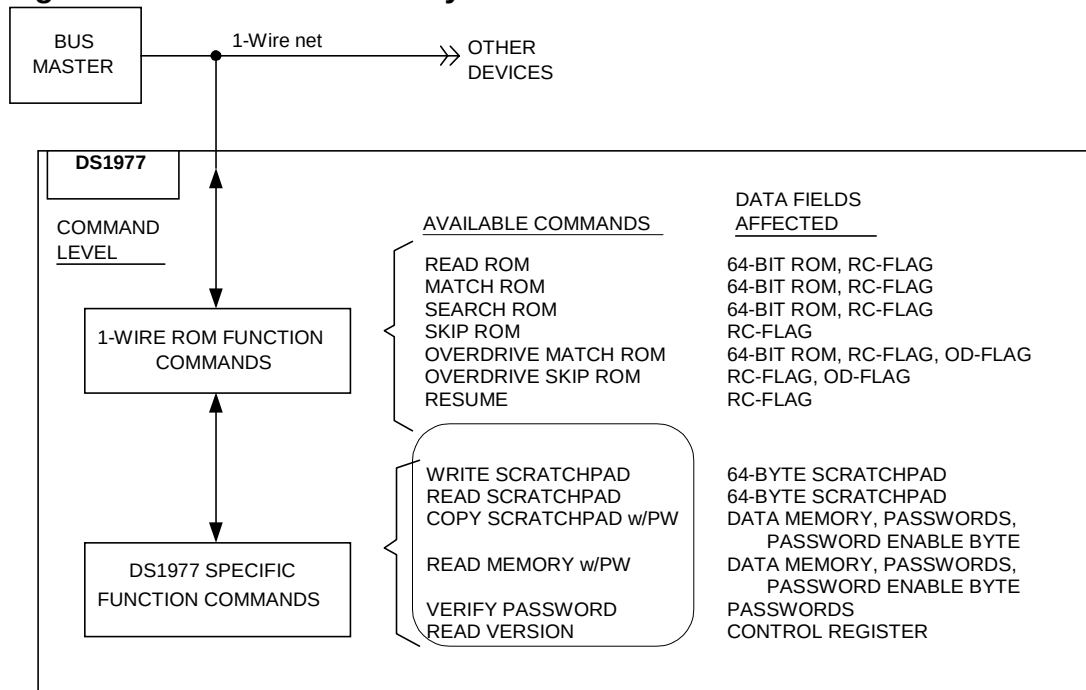


Figure 3. Device Memory Map

ADDRESS RANGE	ACCESS TYPE	DESCRIPTION
0000h to 003Fh	R/W	User Data Memory Page 0
0040h to 007Fh	R/W	User Data Memory Page 1
0080h to 7F7Fh	R/W	User Data Memory Pages 2 to 509
7F80h to 7FBFh	R/W	User Data Memory Page 510
7FC0h to 7FC7h	W	Read Access Password (A)
7FC8h to 7FCFh	W	Read/Write Access Password (B)
7FD0h	R/W	Password Control Register
7FD1h to 7FFFh	----	(reserved)

Read Access Password, Addresses 7FC0h to 7FC7h

The Read Access Password provides access to the function Read Memory. No password applies when reading from or writing to the scratchpad. If passwords are enabled (EPW = AAh, see Password Control Register), the 64-bit data pattern that the 1-Wire master has to transmit with the command flow is compared to the passwords stored in the DS1977 iButton. If the password matches, access is granted.

Read/Write Access Password, Addresses 7FC8h to 7FCFh

The Read/Write Access Password provides access to the functions Read Memory and Copy Scratchpad. No password applies when reading from or writing to the scratchpad. If passwords are enabled (EPW = AAh, see Password Control Register), the 64-bit data pattern that the 1-Wire master has to transmit with the command flow is compared to the passwords stored in the DS1977 iButton. If the password matches, access is granted.

Setting up a password is done essentially in the same way as writing data to the user data memory, only the address is different. Before changing passwords, disable passwords. When setting up a password, make sure that all 8 bytes of the password are defined. Otherwise the new password may be unknown. Since they are located in the same memory page, both passwords can be redefined at the same time. Always verify the scratchpad before sending the copy scratchpad command. Before enabling passwords, check whether the new password has been successfully written to the EEPROM chip. See "Verify Password" command for details. After a new password is successfully copied from the scratchpad to its memory location, erase the scratchpad by filling it with new data. Otherwise a copy of the password will remain accessible through the scratchpad until the iButton is disconnected from the 1-Wire line.

Password Control Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
7FD0h	EPW							

Bit Description	Bit(s)	Definition
EPW: Enable Passwords	b0 to b7	This byte specifies whether the device will test the validity of passwords. If the EPW bits form a pattern of 10101010 (AAh), the device will execute these commands only if the correct password is transmitted. If the EPW pattern is different from AAh, any data pattern will be accepted as a valid password. Before enabling passwords, passwords for read access as well as read/write access need to be written to the password registers. The power-on default pattern of EPW is different from AAh.

Version Register (DS1977)

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
N/A	VER2	VER1	VER0	0	0	0	0	0

Bit Description	Bit(s)	Definition
VER: Chip Revision Indicator	b5 to b7	These hard-wired bits are used to distinguish different revisions or chips that use the same 1-Wire family code as the DS1977. The initial version of the DS1977 chip will have all revision bits set to 0.

Figure 4. ADDRESS REGISTERS

TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	PF	E5	E4	E3	E2	E1	E0

Address Registers and Transfer Status

Because of the serial data transfer, the DS1977 iButton employs three address registers, called TA1, TA2 and E/S (Figure ??). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the 1-Wire master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with write commands. Therefore, the 1-Wire master only has read access to this register. The lower six bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 6 of the E/S register, called PF, is set if the number of data bits sent by the 1-Wire master is not an integer multiple of 8 or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad will clear the PF bit. Note that the lowest six bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address (TA1) for a Write command is 103Ch for example, then the scratchpad will store incoming data beginning at the byte offset 3Ch and will be full after only four bytes. The corresponding ending offset in this example is 3Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 64-byte capacity of the scratchpad is available, resulting also in the ending offset of 3Fh. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial Flag support the 1-Wire master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA is valid only if the PF flag reads 0. If PF is 0 and AA is 1, a copy has taken place. The AA bit is cleared when the device receives a write scratchpad command.

Writing With Verification

To write data to the DS1977 iButton, the scratchpad has to be used as intermediate storage. First the 1-Wire master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see Write Scratchpad command) the 1-Wire master will receive an inverted CRC16 of the command, address and data at the end of the write scratchpad command sequence. Knowing this CRC value, the 1-Wire master can compare it to the value it has calculated itself to decide if the communication was successful and proceed to the Copy Scratchpad command. If the 1-Wire master could not receive the CRC16, it has to send the Read Scratchpad command to read back the scratchpad to verify data integrity. As preamble to the scratchpad data, the DS1977 iButton repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The 1-Wire master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the 1-Wire master can continue reading and verifying every data byte. After the 1-Wire master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S. The 1-Wire master may obtain the contents of these registers by reading the scratchpad or derive it from the target address and the amount of data to be written. As soon as the DS1977 iButton has received these bytes correctly and the 1-Wire master has provided an acceptable password, the DS1977 will copy the scratchpad data to the requested location beginning at the target address.

Memory and Control Functions

The DS1977 supports the following functions:

- Write Scratchpad (iButton version only)
- Read Scratchpad (iButton version only)
- Copy Scratchpad with Password (iButton version only)
- Read Memory with Password (iButton version only)
- Verify Password (iButton version only)

The following pages provide a short discussion of these functions. **For the detailed flow charts refer to Figure ??.** The TA1, TA2, E/S logic is described in section *Address Registers and Transfer Status*.

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the 1-Wire master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T5:T0). The ending offset (E5: E0) will be the byte offset at which the 1-Wire master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete its content will be ignored and the partial byte flag PF will be set. When writing to a password address, internal circuitry of the chip will force the 3 least significant address bits to 0. Only full 8-byte passwords are accepted. The ending offset will be 07 or 0F, depending on the password(s) to be changed.

When executing the Write Scratchpad command the CRC generator inside the DS1977 iButton (see Figure ??) calculates a CRC over the entire data stream, starting at the command code and ending at the last data byte sent by the 1-Wire master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0FH) of the Write Scratchpad command, the Target Addresses TA1 and TA2 as supplied by the 1-Wire master and all the data bytes. The 1-Wire master may end the Write Scratchpad command at any time. However, if the ending offset is 3Fh, the 1-Wire master may send 16 read time slots and will receive the CRC generated by the DS1977 iButton.

The memory address range of the DS1977 iButton is 0000h to 7FFFh (see Figure ??). There is no user-access to the address range 7FD1h to 7FFFh. If the 1-Wire master sends a target address higher than this, the internal circuitry of the chip will set the most significant address bit to zero as it is shifted into the internal address register. The Read Scratchpad command will reveal the target address as it will be used by the DS1977 iButton. The 1-Wire master will identify such address modifications by comparing the target address read back to the target address transmitted. If the 1-Wire master does not read the scratchpad, a subsequent copy scratchpad command will not work since the most significant bits of the target address the 1-Wire master sends will not match the value the DS1977 iButton expects.

Read Scratchpad Command [AAh]

This command is used to verify scratchpad data and target address. After issuing the read scratchpad command, the 1-Wire master begins reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T5: T0). The 1-Wire master may read data until the end of the scratchpad. If the master generates additional times slots, it will read a CRC16 of the command code, target address, E/S byte and scratchpad data starting at the byte offset, which is determined by the target address.

Copy Scratchpad with Password [99h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the 1-Wire master must provide a 3-byte authorization pattern, which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). Next the master must send a valid write access password, or, if passwords are not enabled, 8 dummy bytes. Now the master must provide power by bypassing the 1-Wire pull-up resistor with an electronic switch, generating a "strong pull-up". If authorization pattern and password are accepted, the AA (Authorization Accepted) flag will be set and the copy will begin. Copy takes 10ms maximum during which the voltage on the 1-Wire bus must not fall below 2.8V. After the copy is completed, the master turns off the strong pull-up and begins reading from the 1-Wire. A pattern of alternating 1's and 0's will indicate that the copy command was executed successfully. If the copy command was disturbed due to lack of power or for other reasons, the master will read a constant stream of FFh bytes until it sends a 1-Wire reset pulse.

The data to be copied is determined by the three address registers (TA1, TA2, E/S). The scratchpad data from the beginning offset through the ending offset will be copied to memory, starting at the target address. Anywhere from 1 to 64 bytes may be copied to memory with this command. When updating a password, instead of the password written to the scratchpad a scrambled password is written to the memory location of the respective password.

After the DS1977 has received the password, the 1-Wire master must activate the strong pull-up.

Read Memory with Password [69h]

The read memory command may be used to read the entire memory, except for the passwords. After issuing the command, the master must provide the 2-byte target address. Next the master must send a valid read access password, or, if passwords are not enabled, 8 dummy bytes. Now the master must provide power by bypassing the 1-Wire pull-up resistor with an electronic switch, generating a "strong pull-up". If the password was accepted, EEPROM data beginning at the specified target address and ending at the page boundary will be loaded into the scratchpad starting at the beginning offset. This transfer takes 5 ms maximum during which the voltage on the 1-Wire bus must not fall below 2.8V. After the transfer is completed, the master turns off the strong pull-up and begins reading from the 1-Wire. When the end of the memory page (end of scratchpad) is reached, the master will receive a CRC16 of the command, target address and page data. If the master wants to read more data and the end of the memory is not yet reached, it again has to activate the strong pull-up. This will transfer a full 64-byte page of memory data to

the scratchpad from where the master can read it by issuing read time slots. This loop of strong pull-up and reading 64 bytes can be repeated until the end of the memory is reached, at which point the master will read logic 1's.

After the DS1977 has received the password, the 1-Wire master must activate the strong pull-up.

Verify Password [C3h]

This command allows the user to verify whether the process of updating a password was successful, eliminating the risk of a weak programming of the memory cells that actually store the password. First disable the use of passwords. Then using Write Scratchpad, Read Scratchpad and Copy Scratchpad, write the new password to its respective memory location. Now use Verify Password to double-check whether the password reads correctly from the EEPROM memory. The Verify Password command does not reveal the password, neither in the clear nor in its scrambled form, as it is stored in memory. Instead, the user will learn whether the password transmitted with this command, after having passed the scrambler, matches the password read from the memory. If the match is successful, it is safe to again enable passwords.

Read Version Command [CCh]

This command allows the 1-Wire master to read the chip revision code of the DS1977. After issuing the command code, the master sends two 00h-bytes to access the version register. With the next 16 time slots the master receives two copies of the content of the version register. Additional read-time slots will read logic 1's. Only the upper 3 bits of the version register are valid. The lower 5 bits will all read 0.

ROM Functions

The DS1977 supports the following ROM functions:

- Read ROM
- Match ROM
- Search ROM
- Skip ROM
- Resume
- Overdrive Skip ROM
- Overdrive Match ROM

These functions are implemented in the same way as with other 1-Wire devices.

For the detailed flow charts refer to Figure ??.

Figure 5-1. Memory Function Flow Chart, Part 1

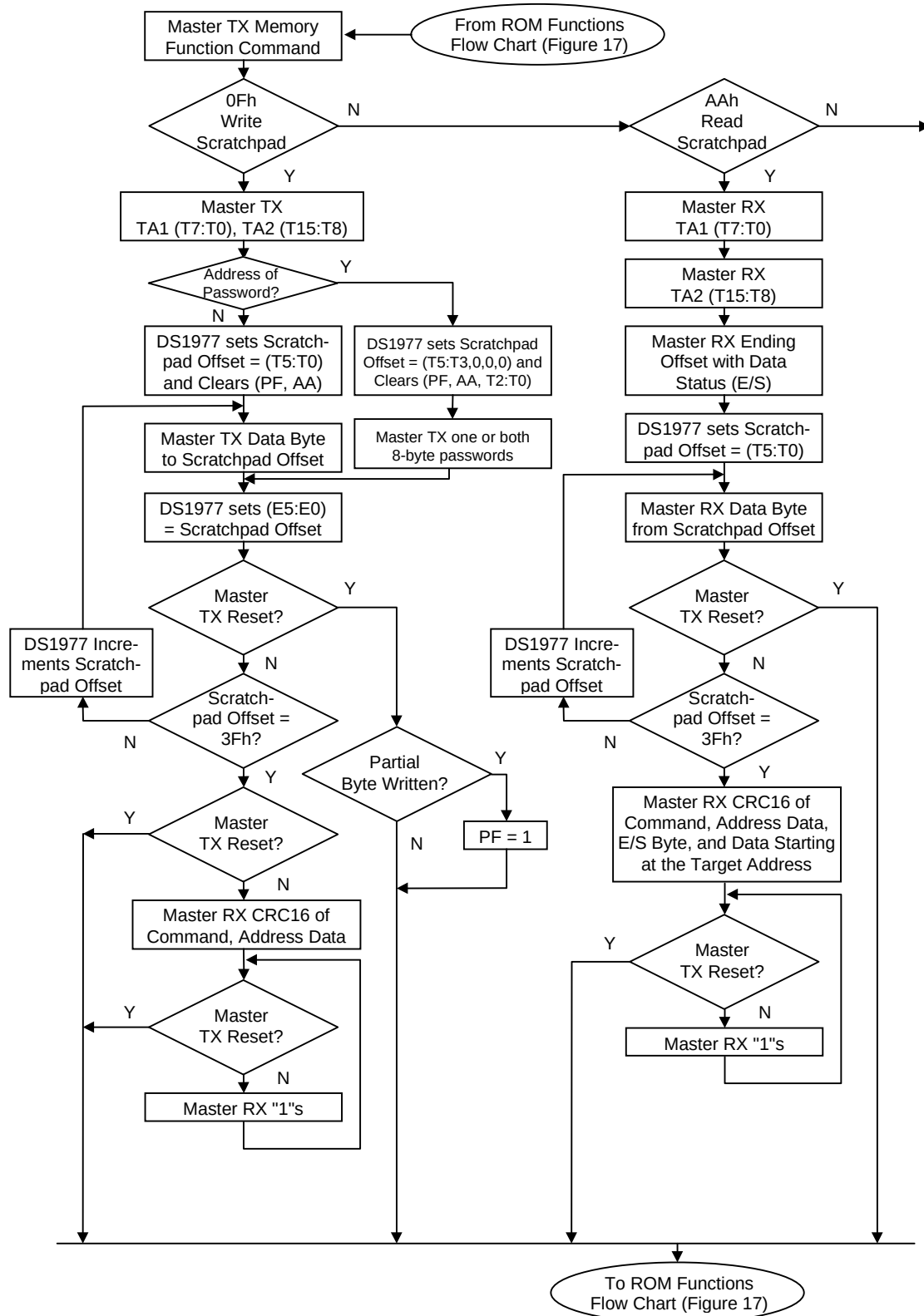


Figure 5-2. Memory Function Flow Chart, Part 2

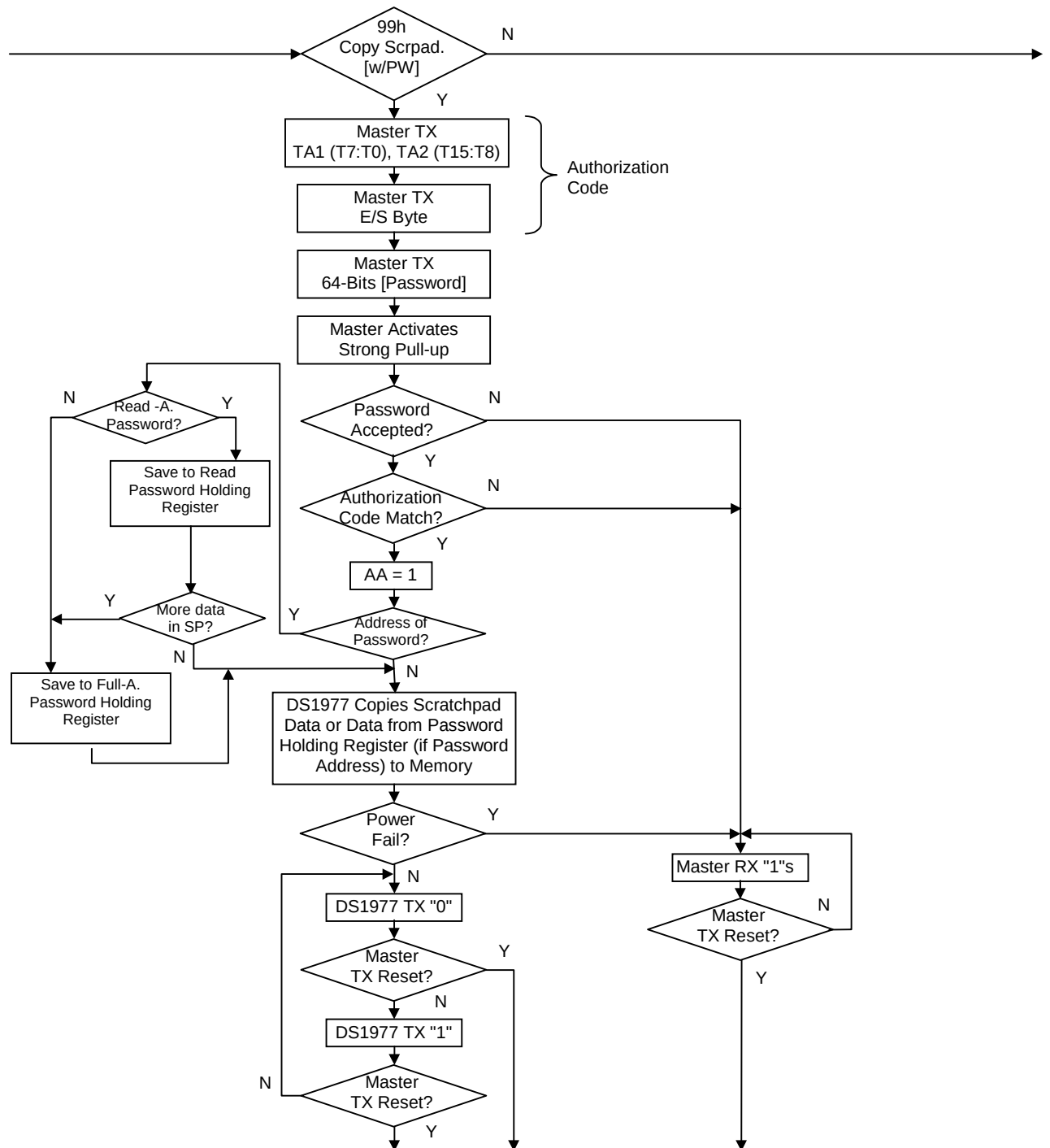


Figure 5-3. Memory Function Flow Chart, Part 3

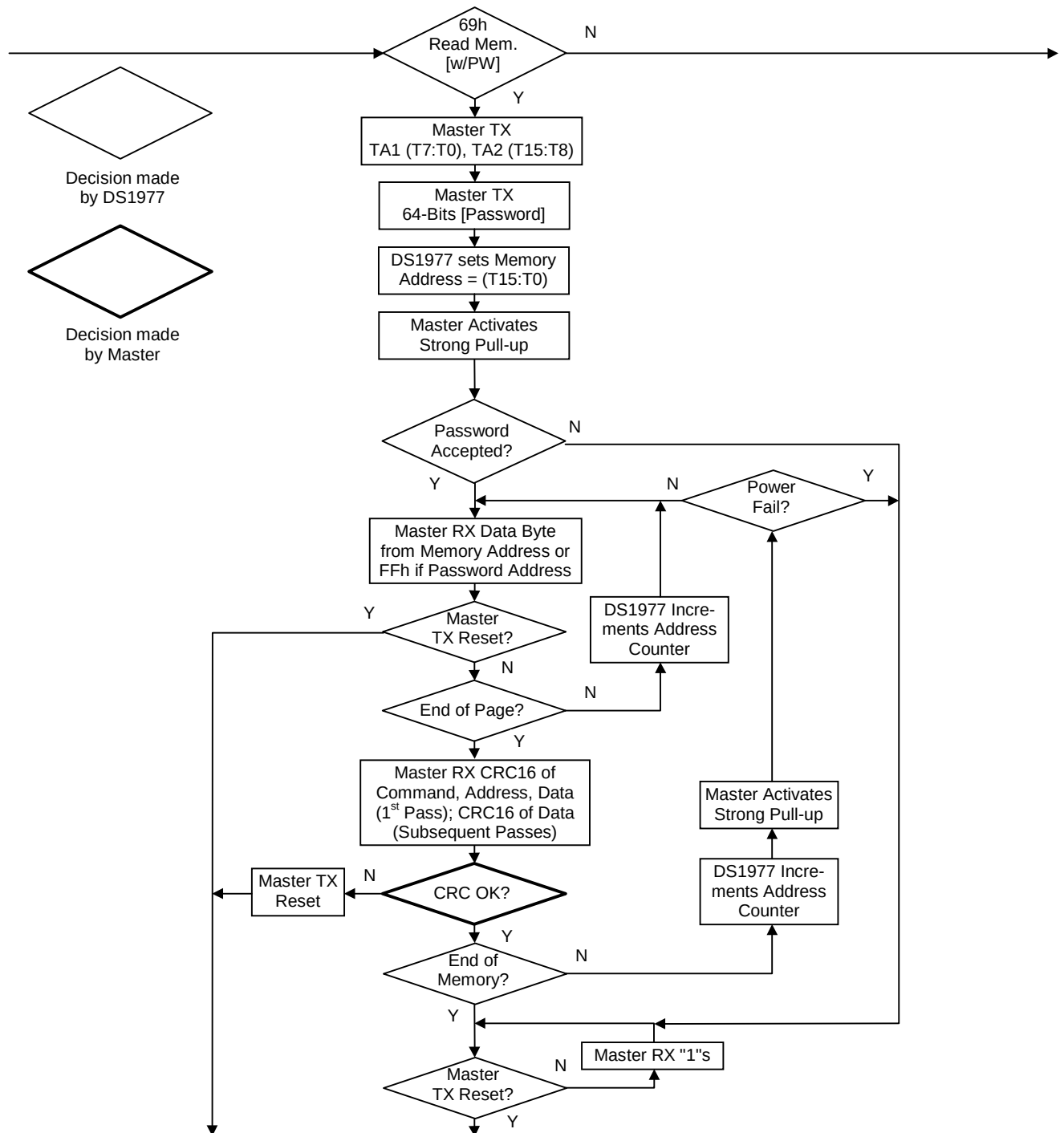
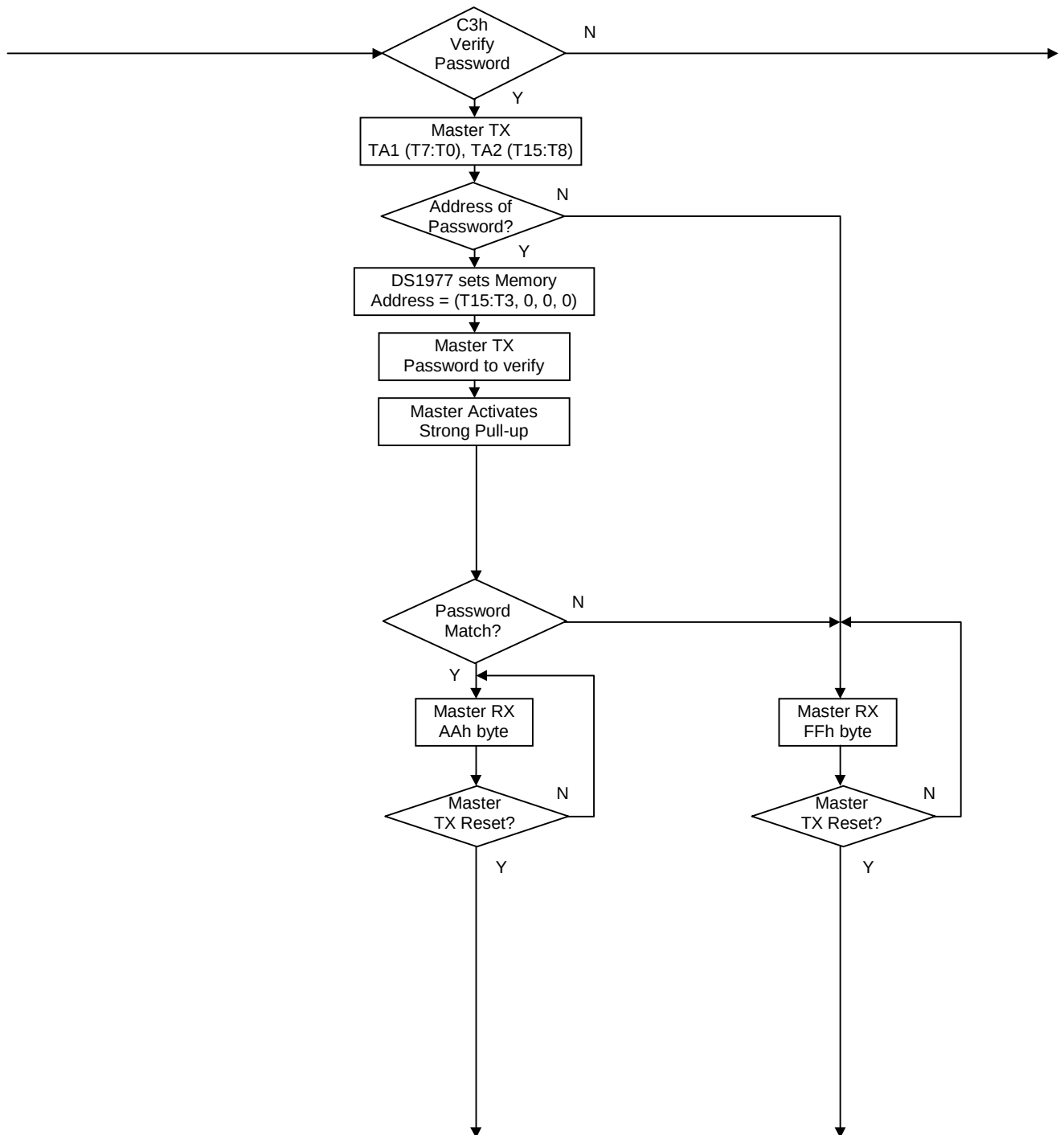


Figure 5-4. Memory Function Flow Chart, Part 4



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graph TD
    Start([All data is LSB first]) --> BusMasterTXResetPulse[Bus Master TX Reset Pulse]
    BusMasterTXResetPulse --> ODResetPulse{OD Reset Pulse?}
    ODResetPulse -- N --> OD0[OD=0]
    OD0 --> DS1977TXPresencePulse[DS1977 TX Presence Pulse]
    ODResetPulse -- Y --> DS1977TXPresencePulse
    DS1977TXPresencePulse --> BusMasterTXROMFunctionCommand[Bus Master TX ROM Function Command]
    BusMasterTXROMFunctionCommand --> R33h{33h Read ROM Command?}
    R33h -- Y --> RC0_33h[RC=0]
    RC0_33h --> DS1977TXFamilyCode[DS1977 TX Family Code 1 Byte]
    DS1977TXFamilyCode --> DS1977TXSerialNumber[DS1977 TX Serial Number 6 Bytes]
    DS1977TXSerialNumber --> DS1977TXCRCByte[DS1977 TX CRC Byte]
    DS1977TXCRCByte --> ToMemoryFunctionFlowChart([To Memory Function Flow Chart])
    R33h -- N --> R55h{55h Match ROM Command?}
    R55h -- Y --> RC0_55h[RC=0]
    RC0_55h --> BusMasterTXBit0_55h[Bus Master TX Bit 0]
    BusMasterTXBit0_55h --> Bit0Match_55h{Bit 0 Match?}
    Bit0Match_55h -- Y --> BusMasterTXBit1_55h[Bus Master TX Bit 1]
    Bit0Match_55h -- N --> Bit0Match_F0h{Bit 0 Match?}
    BusMasterTXBit1_55h --> Bit1Match_55h{Bit 1 Match?}
    Bit1Match_55h -- Y --> BusMasterTXBit63_55h[Bus Master TX Bit 63]
    Bit1Match_55h -- N --> Bit1Match_F0h{Bit 1 Match?}
    BusMasterTXBit63_55h --> Bit63Match_55h{Bit 63 Match?}
    Bit63Match_55h -- Y --> RC1_55h[RC=1]
    Bit63Match_55h -- N --> BusMasterTXReset{Bus Master TX Reset}
    BusMasterTXReset -- Y --> BusMasterTXResetPulse
    BusMasterTXReset -- N --> ToMemoryFunctionFlowChart
    Bit0Match_F0h -- Y --> DS1977TXBit0_F0h[DS1977 TX Bit 0  
DS1977 TX Bit 0  
Bus Master TX Bit 0]
    Bit0Match_F0h -- N --> Bit0Match_CCh{Bit 0 Match?}
    DS1977TXBit0_F0h --> Bit1Match_F0h{Bit 1 Match?}
    Bit1Match_F0h -- Y --> DS1977TXBit63_F0h[DS1977 TX Bit 63  
DS1977 TX Bit 63  
Bus Master TX Bit 63]
    Bit1Match_F0h -- N --> Bit1Match_CCh{Bit 1 Match?}
    DS1977TXBit63_F0h --> Bit63Match_F0h{Bit 63 Match?}
    Bit63Match_F0h -- Y --> RC1_F0h[RC=1]
    Bit63Match_F0h -- N --> BusMasterTXReset
    Bit0Match_CCh -- Y --> RC0_CCh[RC=0]
    RC0_CCh --> ToMemoryFunctionFlowChart
    Bit0Match_CCh -- N --> RFB([RFB])
    
```

The flowchart illustrates the DS1977 TX ROM Function Command sequence. It begins with a 'Bus Master TX Reset Pulse' and an 'OD Reset Pulse?' decision. If the OD Reset Pulse is not received (N), OD is set to 0. If received (Y), the process proceeds to the 'DS1977 TX Presence Pulse'. Following this, the 'Bus Master TX ROM Function Command' is issued. The process then checks for the '33h Read ROM Command?'. If received (Y), RC is set to 0, and the DS1977 TX Family Code (1 Byte), Serial Number (6 Bytes), and CRC Byte are transmitted. If not received (N), the process checks for the '55h Match ROM Command?'. If received (Y), RC is set to 0, and the Bus Master TX Bit 0 is transmitted. A 'Bit 0 Match?' decision follows. If matched (Y), the Bus Master TX Bit 1 is transmitted, followed by a 'Bit 1 Match?' decision. If matched (Y), the Bus Master TX Bit 63 is transmitted, followed by a 'Bit 63 Match?' decision. If matched (Y), RC is set to 1. If not matched (N), a 'Bus Master TX Reset' is performed. If the '55h Match ROM Command?' is not received (N), the process checks for the 'F0h Search ROM Command?'. If received (Y), RC is set to 0, and the DS1977 TX Bit 0, Bit 1, and Bit 63 are transmitted. 'Bit 0 Match?', 'Bit 1 Match?', and 'Bit 63 Match?' decisions follow, with 'Y' leading to RC=1 and 'N' leading to a 'Bus Master TX Reset'. If the 'F0h Search ROM Command?' is not received (N), the process checks for the 'CCh Skip ROM Command?'. If received (Y), RC is set to 0, and the process proceeds to the 'To Memory Function Flow Chart'. If not received (N), the process proceeds to 'RFB'.

Figure 6-2. ROM Function Flow Chart, Part 2

All data is LSB first

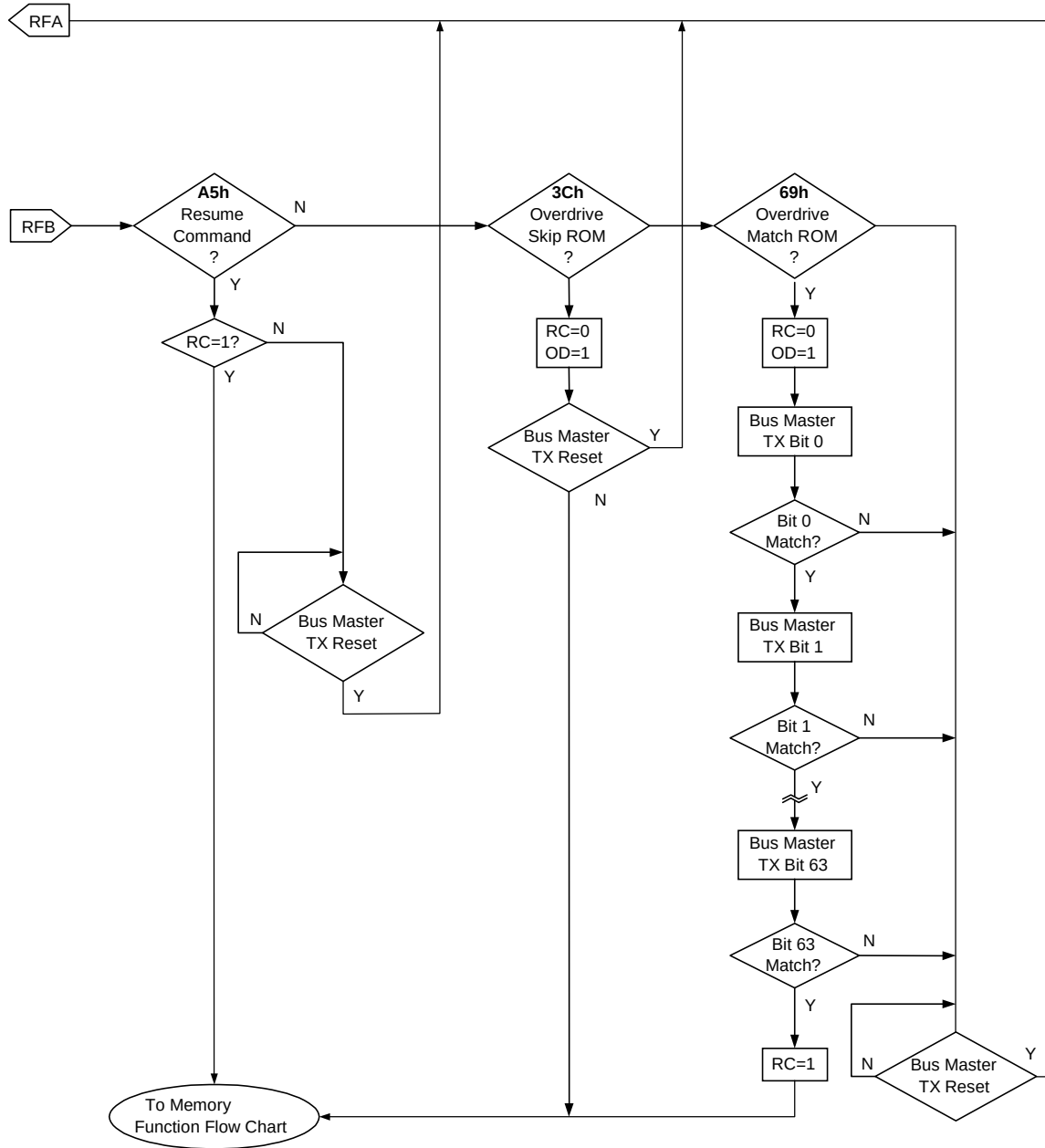


Figure 7. Reset/Presence Detect Cycle

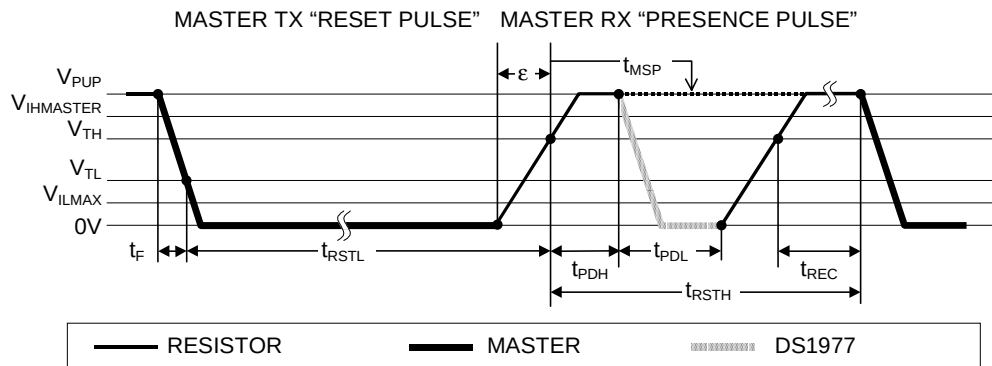


Figure 8. Write-1 Time Slot

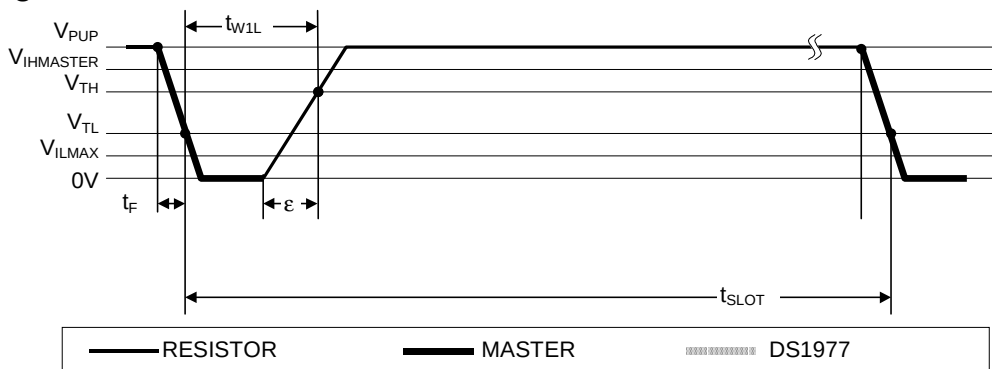


Figure 9. Write-0 Time Slot

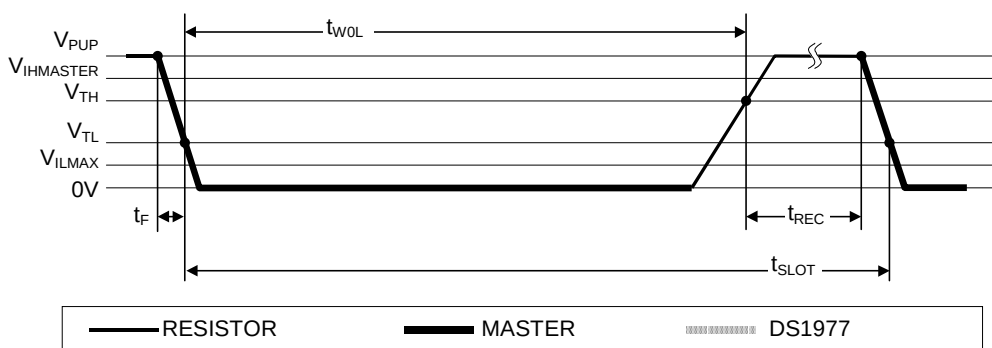
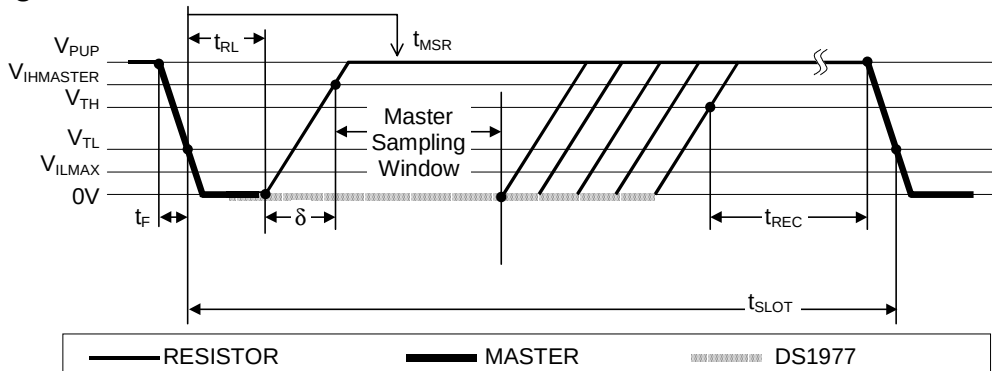


Figure 10. Read-data Time Slot



ABSOLUTE MAXIMUM RATINGS

IO Voltage to GND	-0.3V, +5.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

($V_{PUP} = 2.8V$ to $5.25V$, $V_{CC} \leq V_{PUP}$, parasitic supply capacitor see note 15, $T_A = -40^\circ C$ to $+85^\circ C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Supply Current	I _{CC}	V _{PUP} = V _{CC} = 5.0V, IO at 0V		0.05	5	μA
Ground Current (system requirement)	I _{GND}				20	mA
IO pin general data						
1-Wire Pull-up Resistance (Note 2) (system requirement)	R _{PUP}			2.2		kΩ
Input Load Current	I _L	IO pin at V _{PUP}	1	10		μA
High-to-Low Switching Threshold (Notes 3, 4)	V _{TL}		0.5	3.2		V
Input Low Voltage (Note 5) (system requirement)	V _{IL}			0.30		V
Low-to-High Switching Threshold (Notes 3, 6)	V _{TH}		0.7	3.4		V
Switching Hysteresis (Note 7)	V _{HY}		0.15	N/A		V
Output low voltage at 4mA (Note 8)	V _{OL}			0.4		V
Recovery Time (system requirement)	t _{REC}	Standard Speed, R _{PUP} =2.2kΩ	5			μs
		Overdrive Speed, R _{PUP} =2.2kΩ	2			μs
		Overdrive Speed, immediately prior to reset pulse; R _{PUP} =2.2kΩ	5			μs
Rising-Edge Hold-off Time (Note 9)	t _{REH}	Standard Speed	0.5	5.0		μs
		Overdrive Speed	0.5	2.0		μs
Timeslot Duration (system requirement)	t _{SLOT}	Standard Speed	65			μs
		Overdrive Speed	8			μs
IO pin, 1-Wire Reset, Presence detect cycle						
Reset Low Time (system requirement)	t _{RSTL}	Standard Speed	480	640		μs
		Overdrive Speed	48	80		μs
Presence Detect High Time	t _{PDH}	Standard Speed	15	60		μs
		Overdrive Speed	2	6		μs
Presence Detect Fall Time (Note 10)	t _{FPD}	Standard Speed, V _{PUP} > 4.5V.	1.5	5		μs
		Standard Speed	1.5	8		μs
		Overdrive Speed	0.15	1		μs
Presence Detect Low Time	t _{PDL}	Standard Speed	60	240		μs
		Overdrive Speed	8	24		μs
Presence Detect Sample Time (system requirement)	t _{MSP}	Standard Speed, V _{PUP} > 4.5V.	65	75		μs
		Standard Speed	68	75		μs
		Overdrive Speed	9	10		μs
IO pin, 1-Wire Write						
Write-0 Low Time (system requirement)	t _{W0L}	Standard Speed	60	120		μs
		Overdrive Speed	6	16		μs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write-1 Low Time (Note 11) (system requirement)	t _{W1L}	Standard Speed	5		15 - ε	μs
		Overdrive Speed	1		2 - ε	μs
IO pin, 1-Wire Read						
Read Low Time (Note 12) (system requirement)	t _{RL}	Standard Speed	5		15 - δ	μs
		Overdrive Speed	1		2 - δ	μs
Read-0 Low (data from slave)	t _{SPD}	Standard Speed, V _{PUP} > 4.5V.	20		54	μs
		Standard Speed	15		60	μs
		Overdrive Speed	2		6	μs
Read Sample Time (Note 12) (system requirement)	t _{MSR}	Standard Speed, V _{PUP} > 4.5V.	t _{RL} + δ		20	μs
		Standard Speed	t _{RL} + δ		15	μs
		Overdrive Speed	t _{RL} + δ		2	μs
VCC Output						
IO to VCC Voltage Drop (Note 13)	ΔV _{IOCC}	7 mA load current, V _{IO} = 2.8V			0.1	V
Load current	I _{LOAD}	V _{CC} = 2.7 to 5.25V			7	mA

Note 1: This is a requirement that the 1-Wire master has to meet.

Note 2: Maximum allowable pull-up resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pull-up such as that found in the DS2480B may be required.

Note 3: V_{TL} , V_{TH} are a function of the internal supply voltage.

Note 4: Voltage below which, during a falling edge on IO, a logic '0' is detected.

Note 5: The voltage on IO needs to be less or equal to V_{ILMAX} whenever the master drives the line low.

Note 6: Voltage above which, during a rising edge on IO, a logic '1' is detected.

Note 7: After V_{TH} is crossed during a rising edge on IO, the voltage on IO has to drop by V_{HY} to be detected as logic '0'.

Note 8: The I-V characteristic is linear for voltages less than 1V.

Note 9: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached before.

Note 10: Interval during the negative edge on IO at the beginning of a Presence Detect pulse between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP} .

Note 11: ϵ represents the time required for the pull-up circuitry to pull the voltage on IO up from V_{IL} to V_{TH} .

Note 12: δ represents the time required for the pull-up circuitry to pull the voltage on IO up from V_{IL} to the input high threshold of the bus master.

Note 13: At 7mA load, V_{CC} must not be less than **2.7V**, regardless of V_{IO} . If this condition cannot be met, increase the minimum V_{PUP} to 3.0V or higher.

Note 16: The strong pull-up must be on when the t_{DCSA} interval elapses. The t_{DCSA} value must be determined in design as the maximum time required to turn the bypass NCH transistor fully on.