Preliminary Data Sheet
Subject to Change without Notice
January 21, 2004

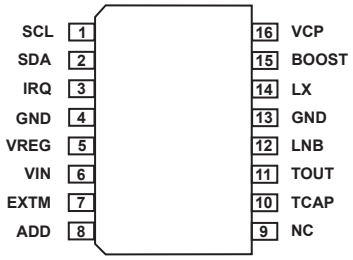
A8285/A8287

Data Sheet
27448.003c

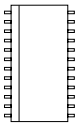
LNB Supply and Control Voltage Regulator

A8285SlB
SOIC

Scale 1:1



A8287SlB
SOIC



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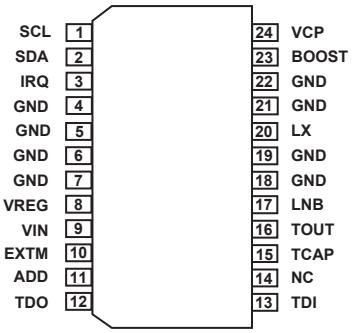


ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{IN} ..... **16 V**
Output Current, I_{OUT} ..... **Internally Limited***
Output Voltage
LNB, BOOST ..... **–0.3 V to 28 V**
TOUT ..... **–0.3 V to 22 V**
Logic Input
EXTM ..... **–0.3 V to 5 V**
Other ..... **–0.3 V to 7 V**
Logic Output ..... **–0.3 V to 7 V**
Package Power Dissipation ……. See power dissipation information in the Application Information section
Operating Temperature
Ambient, T_A ..... **–20°C to +85°C**
Junction, T_J ..... **–20°C to +150°C**
Storage, T_S ..... **–55°C to +150°C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, *do not exceed* the specified current rating or a junction temperature of +150°C.

Intended for analog and digital satellite receivers, the LNB (low noise block) converter regulator is a monolithic linear and switching voltage regulator, specifically designed to provide power and interface signals to an LNB downconverter, via coaxial cable.

The device uses a 2-wire bidirectional serial interface, compatible with the I²C (Inter-C bus) standard, that operates up to 400 kHz.

The A8285 is supplied in a 16-lead plastic power SOIC with copper batwing tabs (suffix *LB*). The A8287 is supplied in a 24-lead plastic power SOIC with copper batwing tabs (part number suffix *LB*).

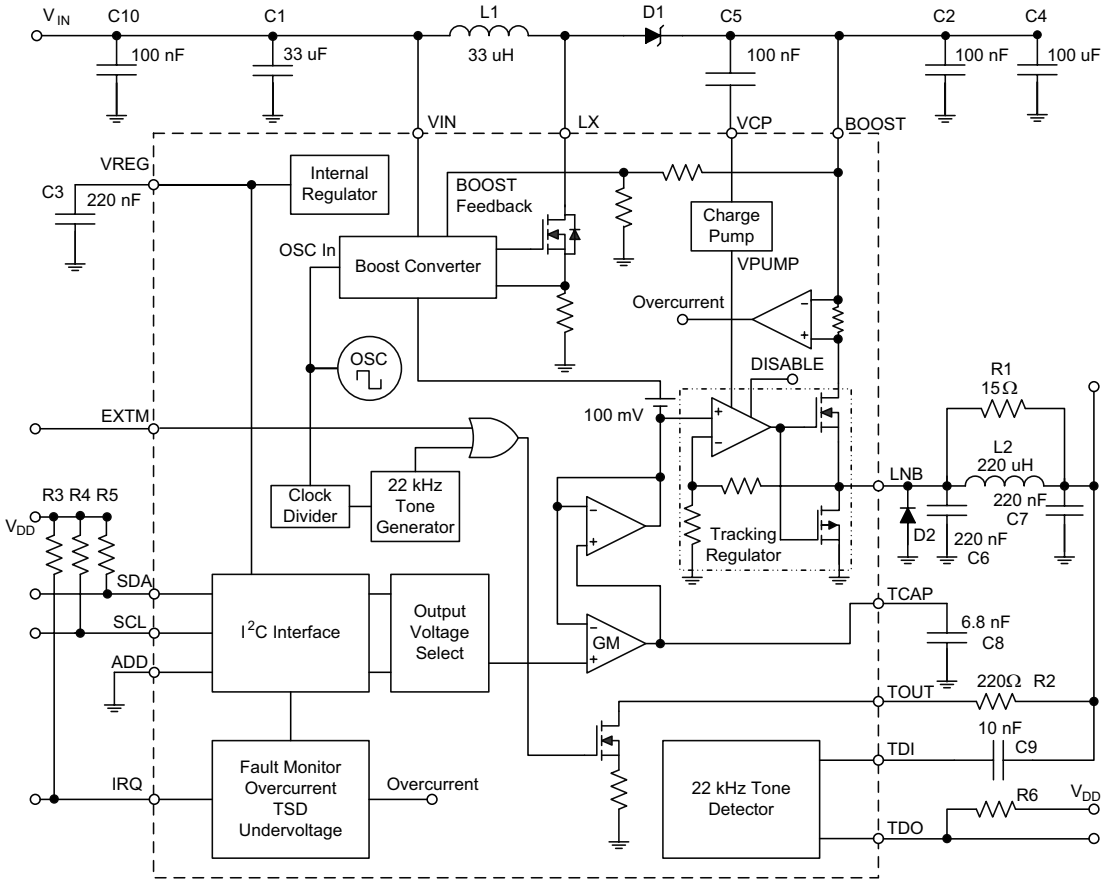
FEATURES

- LNB selection and standby function
- Provides up to 500 mA load current
- Two-wire serial I²C interface
- Built-in tone oscillator, factory-trimmed to 22 kHz; facilitates DiSEqC™ 2.0 encoding
- Auxiliary modulation input
- 22 kHz tone detector facilitates DiSEqC™ decoding (A8287 only)
- Tracking switch-mode power converter for lowest dissipation
- LNB overcurrent protection and diagnostics
- Internal overtemperature protection
- LNB voltages (16 possible levels) compatible with all common standards

Use the following complete part numbers when ordering:

Part Number	Package	Description
A8287SLB	24-pin, batwing SOIC	All features
A8285SLB	16-pin, batwing SOIC	Tone detect not provided

Functional Block Diagram



Tone detector and leads TDI and TDO are not provided in 16-pin package (A8285).

ID	Characteristics	Suggested Manufacturer
C1	33 µF, 25 V, esr < 200 mΩ, I_{ripple} > 350 mA	Nichicon, part number UHC1E330MET
C2, C5,C10	100 nF, 50 V, X5R or X7R	
C4	100 µF, 35 V, esr < 75 mΩ, I_{ripple} > 800 mA	Nichicon, part number UHC1V101MPT
C3,C6,C7	220 nF, 50 V, X5R or X7R	
C8	6.8 nF, 50 V; Y5V, X5R, or X7R	
C9	10 nF (maximum), 50 V; Y5V, X5R, or X7R	
R1	15 Ω, 1%, ⅛ W	
R2	220 Ω, 1%, ½ W	
R3-R6	Value determined by V_{DD}, bus capacitance. etc.	
L1	33 µH, I_{DC} > 1.3 A	TDK, part number TSL0808-330K1R4; Coilcraft, part number DR0810-333
L2	220 µH, I_{DC} > 0.5 A	TDK, part number TSL0808-221KR54; Coilcraft, part number DR0810-224
D1	1 A, 35 V or 40 V, Schottky diode	Various, part number 1N5819; Sanken, part number AW04
D2	1 A, 100 V, 1N4002	

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{IN} = 10 to 16 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Set-point Accuracy, load and line regulation	V_{O1}	Relative to target voltage selected, with: I_{LOAD} = 0 to 500 mA	-4.5	0	4.5	%
Supply Current	I_{CC}	ENB = Low, LNB output disabled	–	–	7	mA
	I_{CCEN}	ENB = High, LNB output enabled, I_{LOAD} = 0mA	–	–	15	mA
Boost Switch-On Resistance	$R_{DSBOOST}$	T_J = 25 °C, I_{LOAD} = 500mA	–	400	500	mΩ
Switching Frequency	fo	–	320	352	384	kHz
Switch Current Limit	–	V_{IN} = 12 V	2.0	3	4.0	A
Linear Regulator Voltage Drop	ΔV_{REG}	V_{BOOST} – V_{LNB}, no tone signal, I_{LOAD} = 500 mA	400	600	800	mV
Slew Rate Current on TCAP	I_{CAP}	Charging	–12.5	–10	–7.5	µA
		Discharging	7.5	10	12.5	µA
Output Voltage Slew Period	t_{slew}	V_{LNB} = 13 to 18 V, TCAP = 6.8 nF, I_{LOAD} = 500 mA	–	500	–	µs
Output Reverse Current	I_{OR}	ENB = Low, V_{LNB} = 28 V with C4 fully charged	–	1	5	mA
Ripple and Noise on LNB Output	V_{RN}	See notes 1 and 2	–	–	50	mV_{pp}
Protection Circuitry						
Overcurrent Limit	I_{LIM}	High limit Low limit	550 400	700 500	850 600	mA mA
Overcurrent Disable Time	t_{DIS}	–	1.2	–	1.7	ms
V_{IN} Undervoltage Threshold	UV_{OFF}	Guaranteed turn-off	8.65	9.15	9.65	V
V_{IN} Turn-On Threshold	UV_{ON}	Guaranteed turn-on	8.75	9.25	9.75	V
Power-Not-Good Flag Set	PNG_{set}	–	77	85	93	$\%V_{LNB}$
Power-Not-Good Flag Reset	PNG_{reset}	–	82	90	98	$\%V_{LNB}$
Thermal Shutdown Threshold	T_J	See note 1	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J	See note 1	–	20	–	°C

Continued on next page

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ELECTRICAL CHARACTERISTICS (*continued*) at T_A = +25°C, V_{IN} = 10 to 16 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Tone Characteristics						
Tone Frequency	f_{TONE}	–	20	22	24	kHz
Tone Pull-Down Current	I_{TONE}	–	30	40	50	mA
Tone Turn-On and Turn-Off Delays	t_{DEL}	Using EXTM pin	–	–	1	µs
External Tone Logic Input	V_{IH}	–	2	–	–	V
	V_{IL}	–	–	–	0.8	V
Input Leakage	I_{IL}	–	–1	–	1	µA
Tone Detector Input Amplitude	V_{TDI}	f_{IN} = 22 kHz	260	–	1000	mV
Tone Detector Frequency Capture	f_{TDI}	600 mV_{pp} sinewave	17.6	–	26.4	kHz
Tone Detector Input Impedance	Z_{TDI}	See note 1	–	8.6	–	kΩ
Tone Detector Output Voltage	V_{OL}	Tone present, I_{LOAD} = 3 mA	–	–	0.4	V
Tone Detector Output Leakage	I_{OL}	Tone absent, V_O = 7 V	–	–	10	µA
I²C Interface						
Logic Input (SDA,SCL) Low Level	V_{IL}	–	–	–	0.8	V
Logic Input (SDA,SCL) High Level	V_{IH}	–	2	–	–	V
Input Hysteresis	V_{HYS}	–	–	150	–	mV
Logic Input Current	I_{IN}	V_{IN} = 0 V to 7 V	–10	<±1.0	10	µA
Output Voltage (SDA, IRQ)	V_{OL}	I_{LOAD} = 3 mA	–	–	0.4	V
Output Leakage (SDA, IRQ)	I_{OL}	V_O = 0 V to 7 V	–	–	10	µA
SCL Clock Frequency	f_{CLK}	–	0	–	400	kHz
Output Fall Time	t_{OF}	V_{IH} to V_{IL}	–	–	250	ns
Bus Free Time Between Stop and Start	t_{BUF}	See I²C Interface Timing Diagram	1.3	–	–	µs
Hold Time for Start Condition	$t_{HD:STA}$	See I²C Interface Timing Diagram	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	See I²C Interface Timing Diagram	0.6	–	–	µs
SCL Low Time	t_{LOW}	See I²C Interface Timing Diagram	1.3	–	–	µs
SCL High Time	t_{HIGH}	See I²C Interface Timing Diagram	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	See note1; I²C Interface Timing Diagram	100	–	–	ns
Data Hold Time	$t_{HD:DAT}$	See I²C Interface Timing Diagram	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	See I²C Interface Timing Diagram	0.6	–	–	µs

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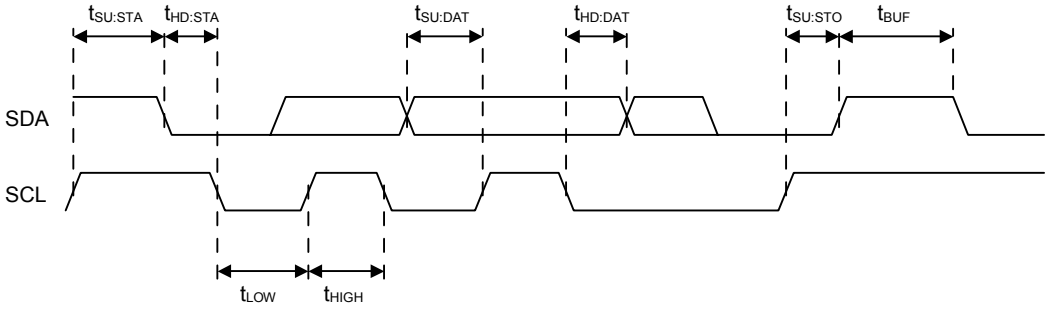
ELECTRICAL CHARACTERISTICS (*continued*) at T_A = +25°C, V_{IN} = 10 to 16 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
I2C Address Setting						
ADD Voltage for Address 0001,000	Address1	–	0	–	0.7	V
ADD Voltage for Address 0001,001	Address2	–	1.3	–	1.7	V
ADD Voltage for Address 0001,010	Address3	–	2.3	–	2.7	V
ADD Voltage for Address 0001,011	Address4	–	3.3	–	5	V

[1] Guaranteed by design.
[2] Use recommended components and adhere to layout guidelines.

I²C Interface Timing Diagram



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Functional Description

Boost Converter/Linear Regulator. A current-mode boost converter provides the tracking regulator a supply voltage that tracks the requested LNB output voltage. The converter operates at 16 times the internal tone frequency, 352 kHz nominal.

The tracking regulator provides minimum power dissipation across the range of output voltages, assuming the input voltage is less than the output voltage, by adjusting the BOOST pin voltage 600 mV nominal above the LNB output voltage selected. Under conditions where the input voltage is greater than the output voltage, the tracking regulator must drop the differential voltage. When operating in this condition, care must be taken to ensure that the safe operating temperature range of the A8285/A8287 is not exceeded. For additional information, see *Power Dissipation* in the Application Information section.

Note: To conserve power at light loads, the boost converter operates in a pulse-skipping mode.

Overcurrent Protection. The A8285/A8287 is protected against both overcurrent and short circuit conditions by limiting the output current to I_{LIM}. In the event of an overcurrent, the current limit can be applied indefinitely. Alternatively, if the ODT feature is enabled, and the fault current appears for longer than the disable time t_{DIS}, then the device is turned off. The device can be enabled again via the I²C interface. If the overcurrent is removed before the disable time has elapsed, the device remains functioning. These settings are made in the Control register and the Status register.

Charge Pump. Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

Slew Rate Control. During either start-up or when the output voltage on the BOOST pin is being changed, the output voltage rise and fall times can be programmed by an external capacitor located on the TCAP pin. Note that during start-up, the BOOST pin is precharged to the input voltage minus a diode drop. As a result, the slew rate control occurs from this point.

The value for TCAP can be calculated using the following formula:

$$TCAP = (I_{CAP} \times 8) / (\Delta V/s)$$

where ΔV/s is required slew rate. The smallest value for TCAP is 2.2 nF.

Modulation is unaffected by the choice of TCAP. If limiting LNB output voltage rise and fall times is not required, the TCAP terminal must have a value of at least a 2.2 nF to minimize output noise.

External Tone Modulation. To improve design flexibility and to allow implementation of proposed LNB remote control standards, the logic modulation input pin EXTM is provided. The logic signal supplied to this pin creates a 650 mV ±250 mV tone signal on the TOUT pin by controlling a 40 mA current pull-down device through the DiSEqC™ filter. The shape of the tone waveform depends on the filter components used and the LNB/cable capacitance.

Tone Detection. A 22 kHz tone envelope detector is provided in the A8287 solution. The detector extracts the tone signal and provides it as an open-collector signal on the TDO pin. The maximum tone out error is ±1 tone cycle, and the maximum tone out delay with respect to the input is ±1 tone cycle.

Control Register. The main functions of the A8285/A8287 are controlled via the I²C interface by writing to the control register. The power-up states for the control functions are all zero. Control functions include the following:

• **Internal Tone Modulation Enable (ENT)**. When the ENT bit is set to 1, the internal tone generator controls a 40 mA pull-down device, thus creating the tone signal after the DiSEqC™ filter in a way identical to the EXTM scheme. The internal oscillator is factory-trimmed to provide a tone of 22 ±2 kHz. No further adjustment is required. Burst coding of the 22 kHz tone is accomplished due to the fast response of the serial command and rapid tone response. This allows implementation of the DiSEqC™ 2.0 protocols.

• **Select Output Voltage Amplitude** (VSEL0, VSEL1, VSEL2, VSEL3). The LNB output voltage can be programmed to a particular voltage according to the Output Voltage Amplitude Selection table shown on the following page.

• **Enable (ENB)**. When set to 1, the LNB output is enabled. When reset to 0, the LNB output is disabled.

• **Overcurrent Limit (I_{LIM})**. Selects the output overcurrent limit. When set to 0, the limit is 500 mA. When set to 1, the limit is 700 mA.

• **Overcurrent Disable Time (ODT)**. When set to 1, in the event of an overcurrent occuring for a duration exceeding the disable time, the device is turned off. When set to 0,

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this feature is disabled and the device is not turned off during an overcurrent.

Status Register. The status of the A8285/A8287 read register can be interrogated by the system master controller via the I²C interface. Status functions include the following:

• **Power Not Good (PNG)**. When the LNB output is enabled, and the LNB output is below 85% of the programmed LNB voltage, the PNG bit is set.

• **Disable (DIS).** Provides the status of the LNB output. When set, this indicates that the output is disabled, either intentionally or by a fault.

• **Thermal Shutdown (TSD)**. When the junction temperature exceeds the maximum threshold, the thermal shutdown bit is set, which disables the LNB output. DIS also is set.

• **Overcurrent (OCP)**. This disables LNB output when an overcurrent appears on the LNB output for a period greater than the ODT (ODT must be enabled for this feature to take effect). In addition, the DIS bit is set. Note: If an overcurrent occurs and ODT is disabled, the A8285/A8287 will operate in current limit indefininitely and the OCP bit will not be set.

Output Voltage Amplitude Selection Table

VSEL3	VSEL2	VSEL1	VSEL0	LNB (V)
0	0	0	0	12.709
0	0	0	1	13.042
0	0	1	0	13.375
0	0	1	1	13.709
0	1	0	0	14.042
0	1	0	1	14.375
0	1	1	0	14.709
0	1	1	1	15.042
1	0	0	0	18.042
1	0	0	1	18.375
1	0	1	0	18.709
1	0	1	1	19.042
1	1	0	0	19.375
1	1	0	1	19.709
1	1	1	0	20.042
1	1	1	1	20.375

• **Undervoltage Lockout (VUV)**. When the input voltage (V_{IN}) drops below the undervoltage threshold, the undervoltage bit VUV is set, disabling the output.

When V_{IN} is initially applied to the A8285/A8285, the VUV bit is set, indicating that an undervoltage condition has occurred.

IRQ Flag. The IRQ flag is activated when any fault condition occurs, including: thermal shutdown, overcurrent, undervoltage, or the occurrence of a power-up sequence. Note that the IRQ flag is not activated when either (a) the channel is disabled (DIS), as it may have been disabled intentionally by the master controller, or (b) if PNG is active, as the A8285/A8287 may be starting up. Fault conditions are stored in the status registers. Also note that the IRQ flag will not activate when an overcurrent occurs and ODT is disabled. In this condition, the device operates within I_{LIM}.

When the IRQ flag is activated during either of the above fault conditions, and the system master controller addresses the A8285/A8287 with the read/write bit set to 1, then the IRQ flag is reset once the A8285/A8287 acknowledges the address. When the master controller reads the data and is acknowledged, the status registers are updated. If the fault is removed, the A8285/A8287 is again ready for operation (being re-enabled via a write command). Otherwise, the controller can keep polling the A8285/A8287 until the fault is removed.

When V_{IN}, is initially applied to the A8285/A8285, the I²C interface will not function until the internal logic supply V_{REG} has reached its operating level. Once V_{REG} is within tolerance, the VUV bit in the status register is set and the IRQ is activated to inform the master controller of this condition. (The IRQ is effectively acting as a power-up flag.) The IRQ is reset when the A8285/A8287 acknowledges the address. Once the master has read the status registers, the VUV bit is reset. The device is then ready for operation.

I²C Interface. This is a serial interface that uses two bus lines, SCL and SDA, to access the internal Control and Status registers of the A8285/A8287. Data is exchanged between a microcontroller (master) and the A8285/A8287 (slave). The clock input to SCL is generated by the master, while SDA functions as either an input or an open drain output, depending on the direction of the data.

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Application Information

Timing Considerations

The control sequence of the communication through the I²C interface is composed of several steps in sequence:

1. **Start Condition**. Defined by a negative edge on the SDA line, while SCL is high.
2. **Address Cycle**. 7 bits of address, plus 1 bit to indicate read (1) or write (0), and an acknowledge bit. The first five bits of the address are fixed as: *00010*. The four optional addresses, defined by the remaining two bits, are selected by the ADD input. The address is transmitted MSB first.
3. **Data Cycles**. 8 bits of data followed by an acknowledge bit. Multiple data bytes can be read. Data is transmitted MSB first.
4. **Stop Condition**. Defined by a positive edge on the SDA line, while SCL is high.

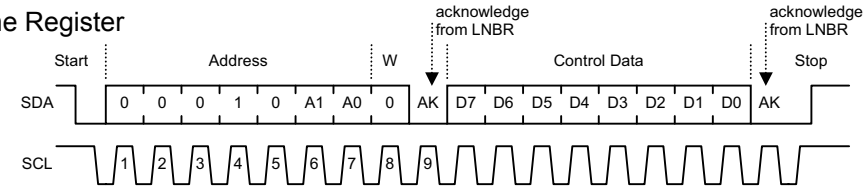
Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A8285/A8287 always responds by resetting the data transfer sequence.

The Read/Write bit is used to determine the data transfer direction. If the Read/Write bit is high, the master reads one or more bytes from the A8285/A8287. If the Read/Write bit is low, the master writes one byte to the A8285/A8287. Note that multiple writes are not permitted. All write operations must be preceded with the address.

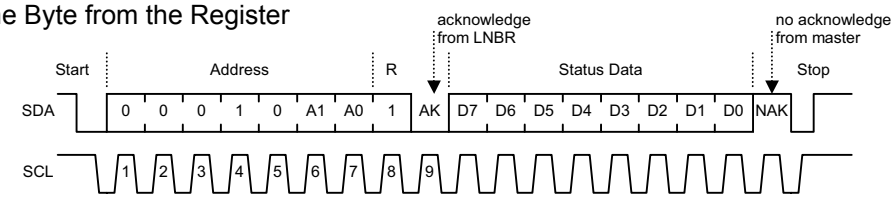
The Acknowledge bit has two functions. It is used by the master to determine if the slave device is responding to its address and data, and it is used by the slave when the master is reading data back from the slave. When the A8285/A8287 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A8285/A8287 also pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received. In both cases, the master device must release the

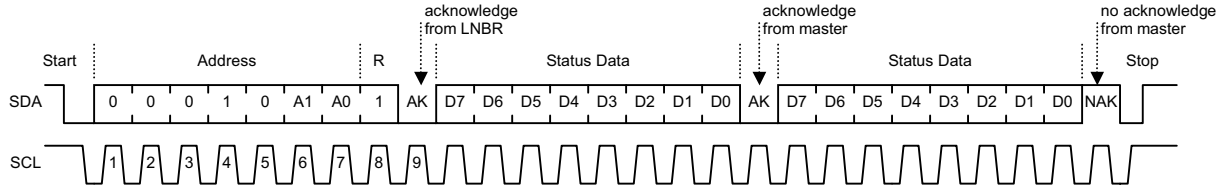
Writing to the Register



Reading One Byte from the Register



Reading Multiple Bytes from the Register



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SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

During a data read, the A8285/A8287 acknowledges the address in the same way as in the data write sequence, and then retains control of the SDA line and send the data to the master. On completion of the eight data bits, the A8285/A8287 releases the SDA line before the ninth clock cycle, in order to allow the master to acknowledge the data. If the master holds the SDA line low during this Acknowledge bit, the A8285/A8287 responds by sending another data byte to the master. Data bytes continue to be sent to the master until the master releases the SDA line during the Acknowledge bit. When this is detected, the A8285/A8287 stops sending data and waits for a stop signal.

Interrupt Request. The A8285/A8287 also provides an interrupt request pin IRQ, which is an open-drain, active-low output. This output may be connected to a common IRQ line with a suitable external pull-up and can be used with other I²C devices to request attention from the master controller. The IRQ output becomes active when either the A8285/A8287 first recognizes a fault condition, or at power-on when the main supply V_{IN} and the internal logic supply V_{REG} reach the correct operating conditions. It is only reset to inactive when the I²C master addresses the A8285/A8287 with the Read/Write bit set (causing a read). Fault conditions are indicated by the TSD, VUV, and OCP bits in the status register (see description of OCP for conditions of use). The DIS and PNG bits do not cause an interrupt. When the master recognizes an interrupt, it addresses all slaves connected to the interrupt line in sequence, and then reads the status register to determine which device is requesting attention. The A8285/A8287 latches all conditions in the status register until the completion of the data read.

The action at the resampling point is further defined in the description for each of the status bits. The bits in the status register are defined such that the all-zero condition indicates that the A8285/A8287 is fully active with no fault conditions.

When V_{IN} is initially applied, the I²C interface does not respond to any requests until the internal logic supply V_{REG} has reached its operating level. Once V_{REG} has reached this point, the IRQ output goes active, and the VUV bit is set. After the A8285/A8287 acknowledges the address, the IRQ flag is reset. Once the master reads the status registers, the registers are updated with the VUV reset.

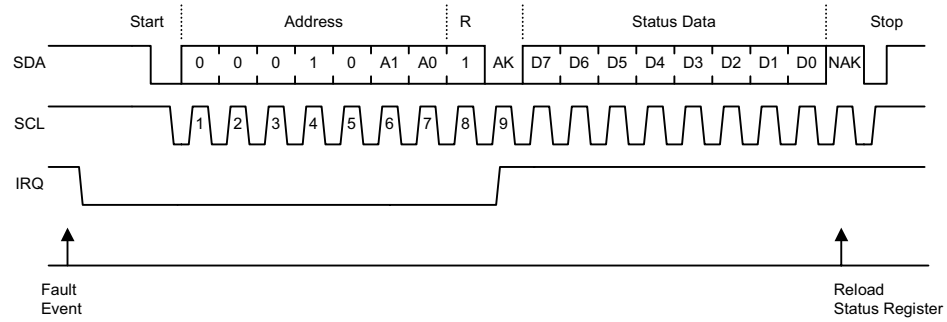
Control Register (I²C Write Register). All main functions of the A8285/A8287 are controlled through the I²C interface via the 8-bit Control register. This register allows selection of the output voltage and current limit, enabling and disabling the LNB output, and switching the 22 kHz tone on and off. The power-up state is 0 for all of the control functions.

Bit 0 (VSEL0), Bit 1 (VSEL1), and Bit 2 (VSEL2). These provide incremental control over the voltage on the LNB output. The available voltages provide the necessary levels for all the common standards plus the ability to add line compensation in increments of 333 mV. The voltage levels are defined in the Output Voltage Amplitude Selection table.

Bit 3 (VSEL3). Switches between the low-level and high-level output voltages on the LNB output. A value of 0 selects the low level voltage and a value of 1 selects the high level. The low-level center voltage is 12.709 V nominal, and the high level is 18.042 V nominal. These may be increased, in increments of 333 mV, by using the VSEL2, VSEL1, and VSEL0 control register bits.

Bit 4 (ODT). When set to 1, enables the ODT feature (disables the A8285/A8287 if the overcurrent disable time is exceeded during an overcurrent condition on the output). When set to 0, the ODT feature is disabled.

Reading the Register After an Interrupt



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Bit 5 (ENB). When set to 1, enables the LNB output. When set to 0, the LNB output is disabled.

Bit 6 (I_{LIM}). Selects the I_{LIM} level. When set to 0, the lower limit (typically 500 mA) is selected. When set to 1, the higher limit (typically 700 mA), is selected.

Bit 7 (ENT). When set to 1, enables modulation of the LNB output with the the internal 22 kHz tone. Since the I²C interface is compatible with the 400 kHz transfer speed, this bit may be used to encode DiSEqC™ 2.0 tone bursts for communication with the LNB or switcher at the far end of the coaxial cable.

Status Register (I²C Read Register). The main fault conditions: overcurrent, undervoltage, and overtemperature, are all indicated by setting the relevant bit in the Status register. In all fault cases, once the bit is set it is not reset until the A8285/A8287 is read by the I²C master. The current status of the LNB output is also indicated by DIS. DIS and PNG are the only bits that may be reset without an I²C read sequence. The normal sequence of the master in a fault condition is to detect the fault by reading the Status register, then rereading the Status register until the status bit is reset, indicating the fault condition has been reset. The fault may be detected by: continuously polling, responding to an interrupt request (IRQ), or detecting a fault condition externally and performing a diagnostic poll of all slave devices. Note that the fully operational condition of the Status register is all 0s. This simplifies checking of the status byte.

Control (I²C Write) Register Table

Bit	Name	Function
0	VSEL0	See Output Voltage Amplitude Selection Table
1	VSEL1	
2	VSEL2	
3	VSEL3	0: LNBx = Low range 1: LNBx = High range
4	ODT	0: Overcurrent disable time off 1: Overcurrent disable time on
5	ENB	0: Disable LNB Output 1: Enable LNB Output
6	ILIM	0: Overcurrent Limit = 500mA 1: Overcurrent Limit = 700mA
7	ENT	0: Disable Tone 1: Enable 22KHz internal tone

Bit 0 (TSD). A 1 indicates that the A8285/A8287 has detected an overtemperature condition and has disabled the LNB output. DIS is set and the A8285/A8287 does not re-enable the output until so instructed by writing the relevant bit into the Control register. The status of the overtemperature condition is sampled on the rising edge of the ninth clock pulse in the data read sequence. If the condition is no longer present, then the TSD bit is reset, allowing the master to re-enable the LNB output if required. If the condition is still present, then the TSD bit remains at 1.

Bit 1 (OCP) Overcurrent. If the A8285/A8287 detects an overcurrent condition for greater than the detection time, and if ODT is enabled, the LNB output is then disabled. Also, the OCP bit is set to indicate that an overcurrent has occurred, and the DIS bit is set. The Status register is updated on the rising edge of the ninth clock pulse. The OCP bit is reset in all cases, allowing the master to re-enable the LNB output. If the overcurrent timer is not enabled, the A8285/A8287 operates in current limit indefinitely, and the OCP bit is not set.

Bit 2 and 3. Reserved.

Bit 4 (PNG) Power Not Good. Set to 1 when the LNB output is enabled and the LNB output volts are below 85% of the programmed LNB voltage. The PNG is reset when the LNB volts are within 90% of the programmed LNB voltage.

Bit 5 (DIS) LNB output disabled. DIS is used to indicate the current condition of the LNB output. At power-on, or if a fault condition occurs, the disable bit is set. Having this bit change to 1 does not cause the IRQ to activate because the LNB output may be disabled intentionally by the I²C master. This bit also is reset at the end of a write sequence, if the LNB output is enabled.

Bit 6. Reserved.

Bit 7 (VUV) Undervoltage lockout. Set to 1 to indicate that the A8285/A8287 has detected that the input supply V_{IN} is, or has been, below the minimum level and that an undervoltage lockout has occurred, which has disabled the LNB output. Bit 5 also is set, and the A8285/A8287 does not re-enable the output until so instructed (by having the relevant bit written into the Control register). The status of the undervoltage condition is sampled on the rising edge of the ninth clock pulse in the data read sequence. If the condition is no longer present, the VUV bit is reset, allowing the master to re-enable the LNB output if required. If the condition is still present, the VUV bit remains set to 1.

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Power Dissipation

To ensure that the device operates within the safe operating temperature range, several checks should be performed. An approximate operating junction temperature can be determined by estimating the power losses and the thermal impedance characteristics of the printed circuit board solution. To do so, perform the following procedure:

1. Estimate the maximum ambient temperature (T_A).

2. Define the maximum running junction temperature (T_J)of A8285/A8287. Note that the absolute maximum junction temperature should never exceed 150ºC.

3. Determine worst case power dissipation:

(a) Estimate the duty cycle D:

$$D = 1 - [V_{IN} / (V_{OUT} + V_D + \Delta V_{REG})]$$

where:

V_D is the voltage drop of the boost diode, and

ΔV_{REG} can be taken from the specification table.

(b) Estimate the peak current in boost stage I_{PK}:

$$I_{PK} = V_{OUT} \times [\, I_{LOAD} / (0.89 \times V_{IN})]$$

(c) Estimate boost R_{DS} ($R_{DSBOOST}$) at maximum running junction temperature. $R_{DSBOOST}$ is a function of junction temperature and it rises by 2.7 mΩ/ºC with respect to the specified figure, $R_{DSBOOST(25ºC)}$, when T_j equals 25ºC.

$$\text{Actual } R_{DSBOOST} = R_{DSBOOST(25ºC)} + [(T_j - 25) \times 2.7\ m\Omega]$$

(d) Determine losses in each block P_{TOT}; based on the relative value of V_{IN}, perform either (i) or (ii):

(i) When $V_{IN} < V_{OUT} + V_D + \Delta V_{REG}$. Note that worst case dissipation occurs at minimum input voltage.

$$P_{TOT} = Pd\_Rds + Pd\_sw + Pd\_control + Pd\_lin$$

where

$$Pd\_Rds = I^2_{PK} \times R_{DSBOOST} \times D$$

$$Pd\_control = 15\ mA \times V_{IN}$$

$$Pd\_lin = \Delta V_{REG} \times I_{LOAD}$$

and Pd_sw (switching losses estimate); worst case = 70 mW.

(ii) When $V_{IN} > V_{OUT} + V_D + \Delta V_{REG}$. Note that worst case dissipation in this case occurs at maximum input voltage.

$$P_{TOT} = Pd\_control + Pd\_lin$$

where:

$$Pd\_control = 15\ mA \times V_{IN}$$

$$Pd\_lin = (V_{IN} - V_D - V_{OUT}) \times I_{LOAD}$$

Step 4. Determine the thermal impedance required in the solution:

$$R_{\Theta JA} = (T_J - T_A) / P_{TOT}$$

The $R_{\Theta JA}$ for one or two layer PCBs can be estimated from the $R_{\Theta JA}$ vs. Area charts on the following page.

Note: For maximum effectiveness, the PCB area underneath the IC should be filled copper and connected to pins 4 and 13 for A8285, and pins 6, 7, 18, and 19 for A8287. Where a PCB with two or more layers is used, apply thermal vias, placing them adjacent to each of the above pins, and underneath the IC.

Status (I²C Read) Register Table

Bit	Name	Function
0	TSD	Thermal Shutdown
1	OCP	Overcurrent
2		Reserved
3		Reserved
4	PNG	Power Not Good
5	DIS	LNB output disabled
6		Reserved
7	VUV	V_{IN} Undervoltage

Example.

Given:

V_{IN} = 12 V

V_{OUT} = 18 V

I_{LOAD} = 500 mA

Two-layer PCB.

Maximum ambient temperature = 70 ºC,

Maximum allowed junction temperature= 110 ºC

Assume:

$$V_D = 0.4 \text{ V and select } \Delta V_{REG} = 0.7 \text{ V}$$

$$D = 1 - (12 / (18 + 0.4 + 0.7) = 0.37$$

$$I_{PK} = 18 \times 0.5 / (0.89 \times 12) = 843 \text{ mA}$$

$$R_{DSBOOST} = 0.5 + (110 - 25) \times 2.7 \text{ m}\Omega = 730 \text{ m}\Omega$$

Worst case losses can now be estimated:

$$Pd\_Rds = 0.843^2 \times 0.73 \times 0.37 = 192 \text{ mW}$$

$$Pd\_sw = 70 \text{ mW}$$

$$Pd\_control = 15 \text{ mA} \times V_{IN} = 180 \text{ mW}$$

$$Pd\_lin = 0.7 \times 0.5 = 350 \text{ mW}$$

and therefore

$$P_{TOT} = 0.192 + 0.07 + 0.18 + 0.35 = 0.792 \text{ W}$$

The thermal resistance required is:

$$(110 - 70) / 0.792 = 50.5 ºC/W$$

Note: For the case of the A8287, the area of copper required on each layer is approximately 1.2 in².

Layout Considerations

Recommended placement of critical components and tracking for the A8287 is shown in the PCB Layout digagram on the following page. It is recommended that the ground plane be separated into two areas, referred to as *switcher* and *control,* on each layer using a ground plane. With respect to the input connections, VIN and 0V, the two ground plane areas are isolated as shown by the dotted line and the ground plane areas are connected together at pins 6, 7, 18, and 19. This configuration minimizes the effects of the noise produced by the switcher on the noise-sensitive sections of the circuit.

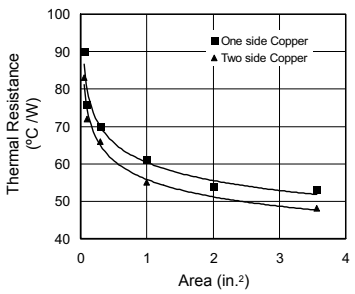
Power-related tracking from INPUT to L1, LNB (pin 17) to L2 then OUTPUT, LX (pin 20) to D1 and L1, VBOOST (pin 23) to C4 and D1 should be as short and wide as possible. Power components such as the boost diode D1, inductor L1, and input/output capacitors C1, C9, and C4, should be located as close as possible to the IC. The DiSEqC inductor L2 should be located as far away from the boost inductor L1 to prevent potential magnetic crosstalk.

The filter capacitor (VREG), charge pump capacitor (VCP), ac coupling tone detect capacitor (TDI), tone pull-down resistor (TOUT), and LNB output capacitor/protection diode (LNB) should be located directly next to the appropriate pin.

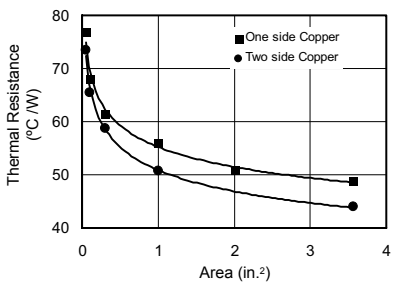
Where a PCB with two or more layers is used, it is recommended that four thermal vias be deployed as shown in the PCB Layout diagram. Note that adding additional vias does not enhance the thermal characteristics.

$R_{ØJA}$ vs. Area Charts

A8285, 16-Pin SOIC



A8287, 24-Pin SOIC



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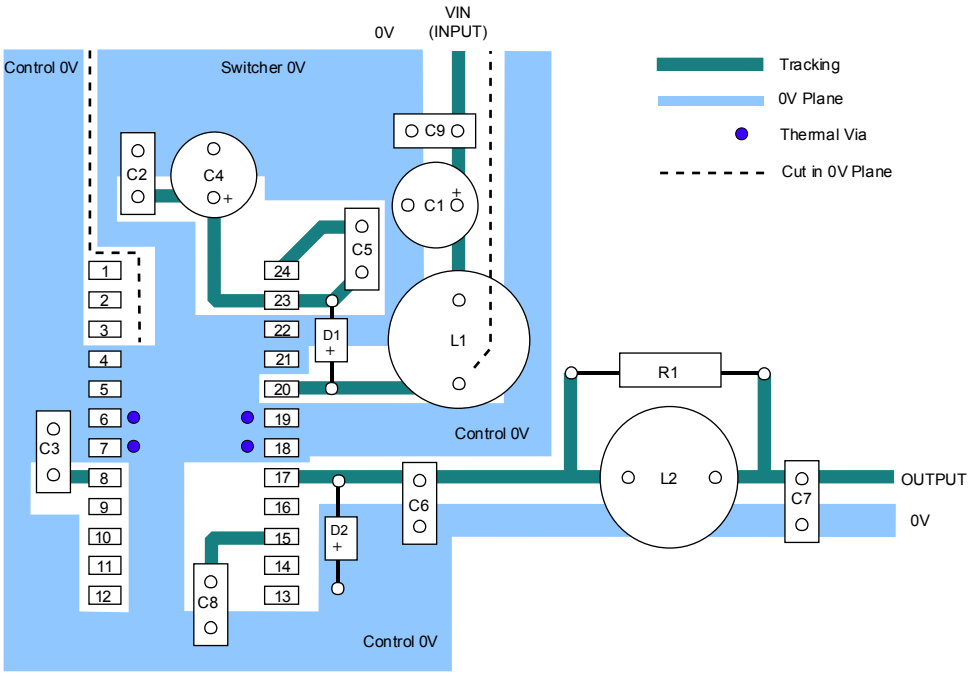
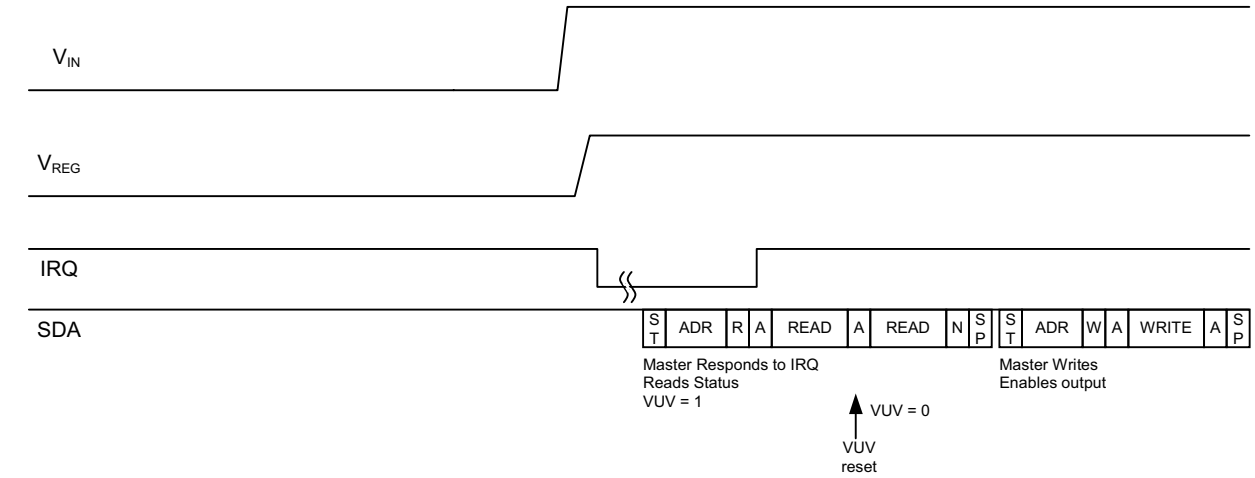
PCB Layout Diagram



Note that to add additional connections, e.g. SCL, SDA, IRQ, VIN, EXTM, ADD, TDO, and TDI, some modifications to the control ground plane will be necessary.

Refer to Functional Block diagram for circuit connections.

Power-on Reset I²C Sequence



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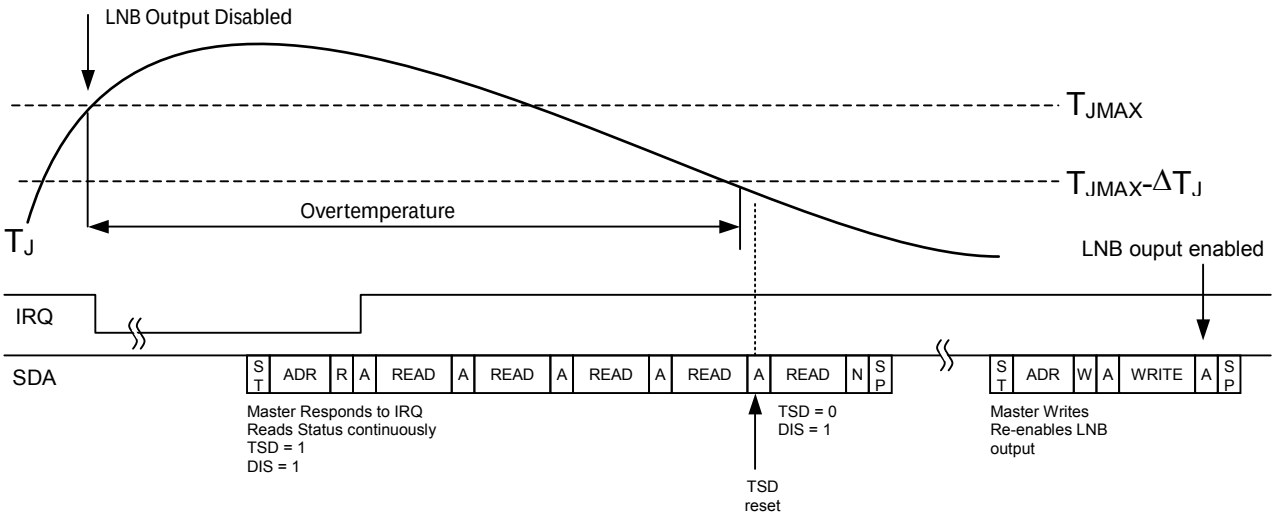
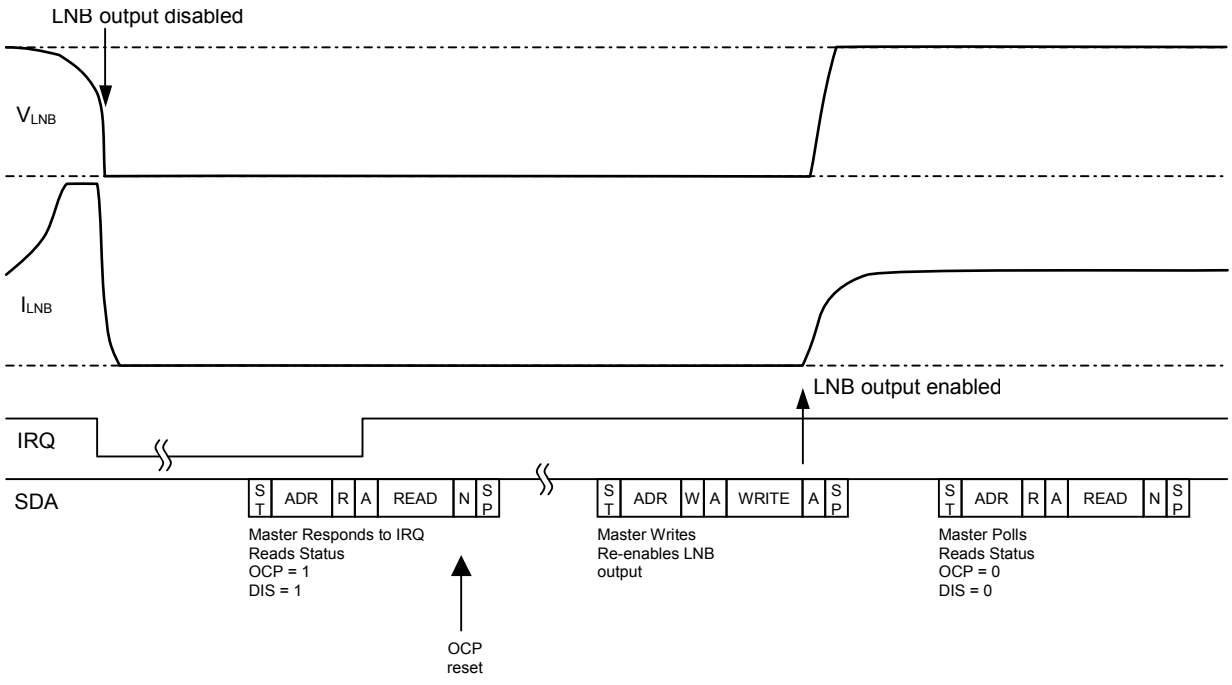
Overtemperature and Overcurrent I²C Sequences

Response to Overtemperature fault condition using multiple byte read



Response to Overcurrent fault condition using single byte read



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Terminal List Table

Pin Name	Pin Description	A8287SLB SOIC-24	A8285SLB SOIC-16
SCL	I2C Clock Input	1	1
SDA	I2C Data Input/Output	2	2
IRQ	Interrupt Request	3	3
GND	Ground	4,5,6,7	4
VREG	Analog Supply	8	5
VIN	Supply Input Voltage	9	6
EXTM	External Modulation Input	10	7
ADD	Address Select	11	8
TDO	Tone Detect Out	12	-
TDI	Tone Detect Input	13	-
NC	No Connection	14	9
TCAP	Capacitor for setting the rise and fall time of the LNB output	15	10
TOUT	Tone Generation	16	11
LNB	Output voltage to LNB	17	12
GND	Ground	18,19	13
LX	Inductor drive point	20	14
GND	Ground	21,22	-
BOOST	Tracking supply voltage to linear regulator	23	15
VCP	Gate supply voltage	24	16

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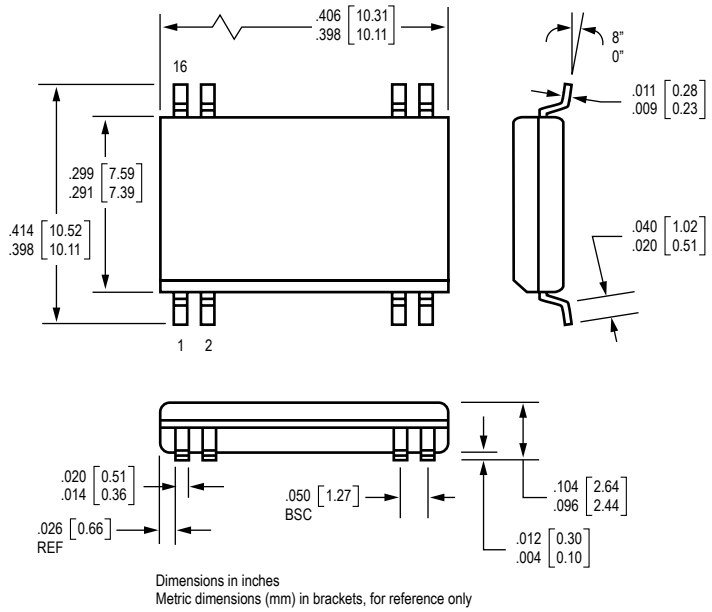
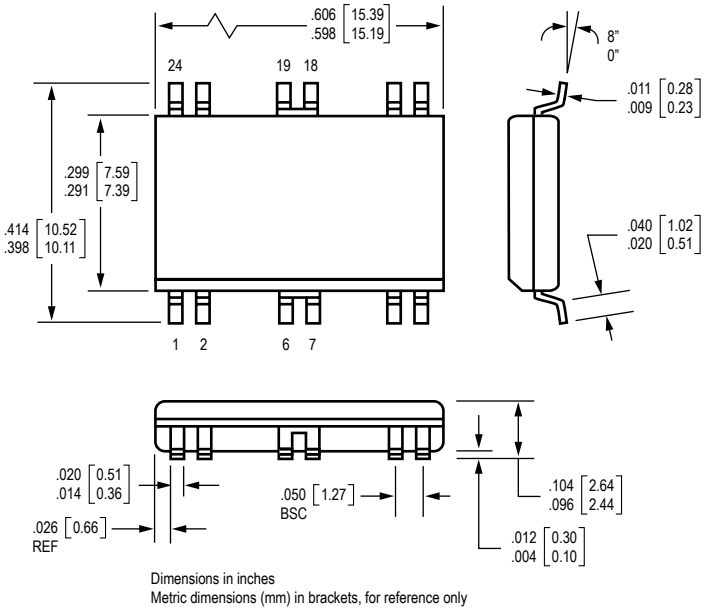
A8285SLB 16-Pin Batwing SOIC



Dimensions in inches
Metric dimensions (mm) in brackets, for reference only

Leads 4 and 13 are connected inside the device package.

A8287SLB 24-Pin Batwing SOIC



Dimensions in inches
Metric dimensions (mm) in brackets, for reference only

Leads 6, 7, 18 and 19 are connected intside the device package.

NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 49 devices or add "TR" to part number for tape and reel.

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A8285/A8287
LNB Supply and Control Voltage Regulator

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