Blackfin® Embedded Processor

ADSP-BF531/ADSP-BF532/ADSP-BF533

FEATURES

Up to 600 MHz high performance Blackfin processor
- **Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit Shifter**
- **RISC-like register and instruction model for ease of programming and compiler-friendly support**
- **Advanced debug, trace, and performance monitoring**

0.8 V to 1.2 V core V_{DD} with on-chip voltage regulation

3.3 V and 2.5 V tolerant I/O

160-ball mini-BGA, 169-ball lead free PBGA, and 176-lead LQFP packages

MEMORY

Up to 148K bytes of on-chip memory:
- **16K bytes of instruction SRAM/Cache**
- **64K bytes of instruction SRAM**
- **32K bytes of data SRAM/Cache**
- **32K bytes of data SRAM**
- **4K bytes of scratchpad SRAM**

Two dual-channel memory DMA controllers

Memory Management Unit providing memory protection

External Memory Controller with glueless support for SDRAM, SRAM, FLASH, and ROM

Flexible memory booting options from SPI and external memory

PERIPHERALS

Parallel Peripheral Interface (PPI)/GPIO, supporting ITU-R 656 video data formats

Two dual-channel, full duplex synchronous serial ports, supporting eight stereo I^2S channels

12-channel DMA controller

SPI compatible port

Three Timer/Counters with PWM support

UART with support for IrDA®

Event Handler

Real-Time Clock

Watchdog Timer

Debug/JTAG interface

On-chip PLL capable of 1x to 63x frequency multiplication

Core Timer

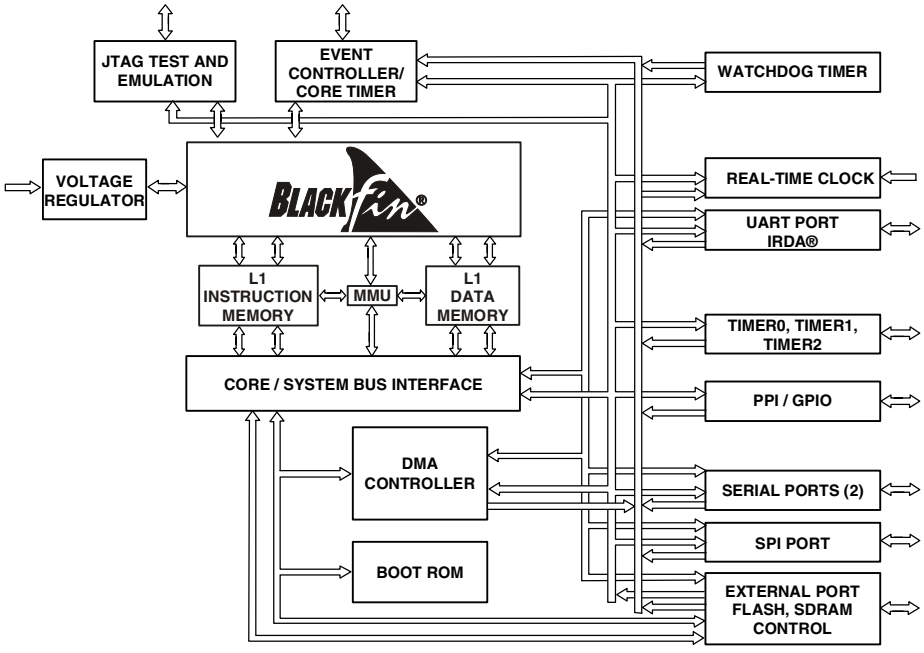

Figure 1. Functional Block Diagram

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

GENERAL DESCRIPTION

The ADSP-BF531/2/3 processors are members of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF531/2/3 processors are completely code and pin compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in Table 1.

Table 1. Processor Comparison

	ADSP-BF531	ADSP-BF532	ADSP-BF533
Maximum Performance	400 MHz 800 MMACs	400 MHz 800 MMACs	600 MHz 1200 MMACs
Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
Instruction SRAM	16K bytes	32K bytes	64K bytes
Data SRAM/Cache	16K bytes	32K bytes	32K bytes
Data SRAM			32K bytes
Scratchpad	4K bytes	4K bytes	4K bytes

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature Dynamic Power Management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/2/3 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a Parallel Peripheral Interface.

ADSP-BF531/2/3 PROCESSOR PERIPHERALS

The ADSP-BF531/2/3 processor contains a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in Figure 1 on Page 1). The general-purpose peripherals include functions such as UART, Timers with PWM (Pulse-Width Modulation) and pulse measurement capability, general-purpose flag I/O pins, a Real-Time Clock, and a Watchdog Timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the ADSP-BF531/2/3 processor contains high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, Real-Time Clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF531/2/3 processor includes an on-chip voltage regulator in support of the ADSP-BF531/2/3 processor Dynamic Power Management capability. The voltage regulator provides a range of core voltage levels from a single 2.25 V to 3.6 V input. The voltage regulator can be bypassed at the user's discretion.

BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives,

saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). By also using the second ALU, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit Index, Modify, Length, and Base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: User mode, Supervisor mode, and Emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while Supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/2/3 processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3 on Page 5, Figure 4 on Page 5, and Figure 5 on Page 6.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF531/2/3 processor has three blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

The External Bus interface can be used with both asynchronous devices such as SRAM, FLASH, EEPROM, ROM, and I/O devices, and synchronous devices such as SDRAMs. The bus width is always 16 bits. A1 is the least significant address of a 16-bit word. 8-bit peripherals should be addressed as if they were 16-bit devices, where only the lower 8 bits of data should be used.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. The SDRAM controller allows one row to be open for each internal SDRAM bank, for up to four internal SDRAM banks, improving overall system performance.

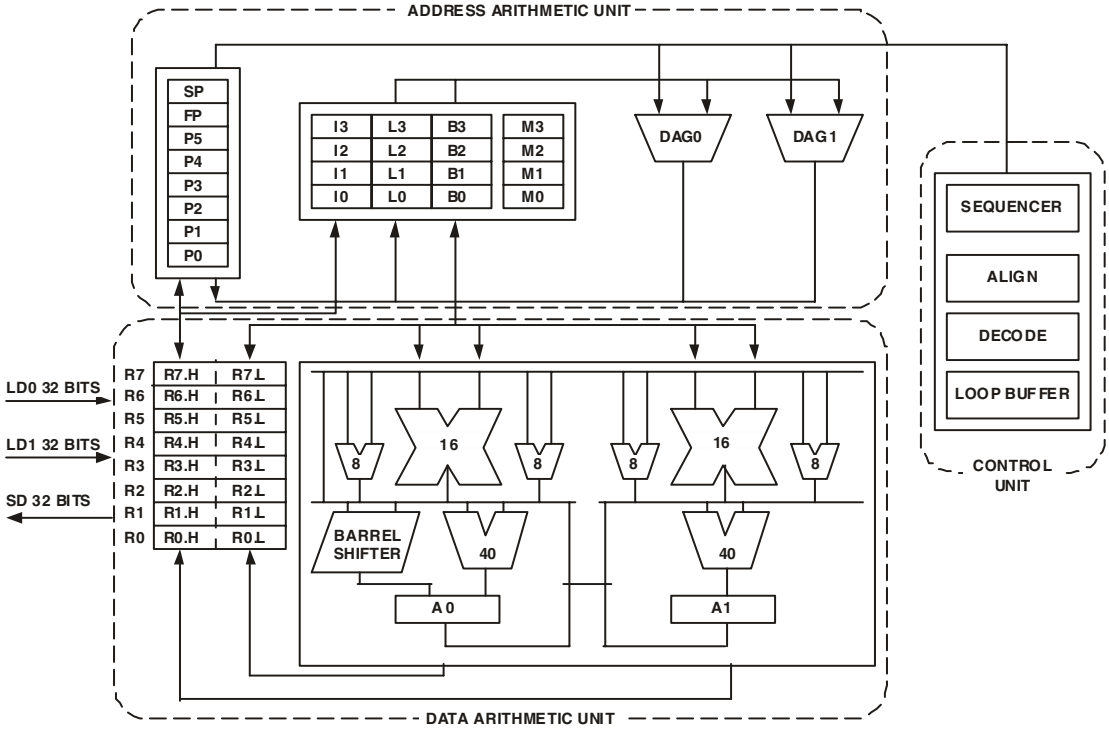


Figure 2. Blackfin Processor Core

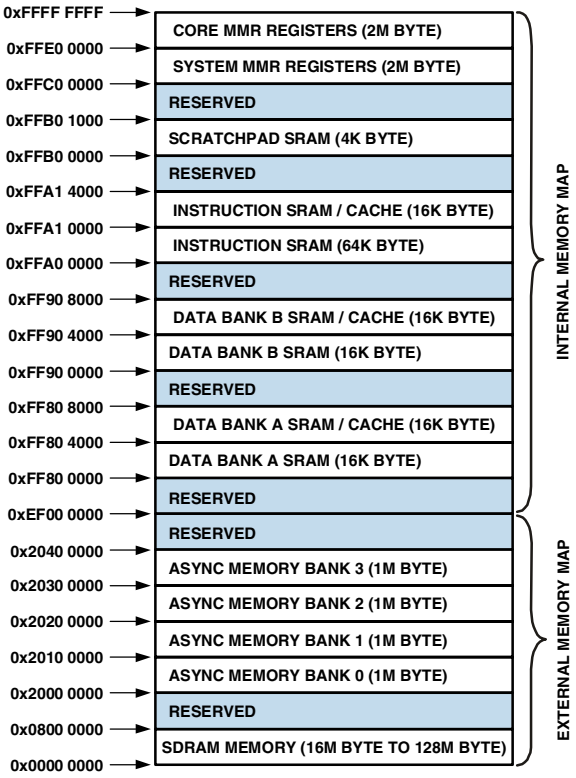


Figure 3. ADSP-BF533 Internal/External Memory Map

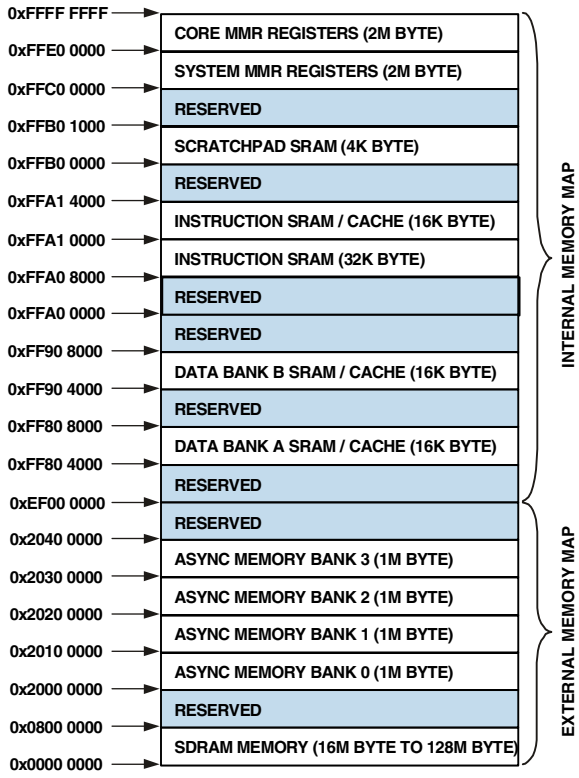


Figure 4. ADSP-BF532 Internal/External Memory Map

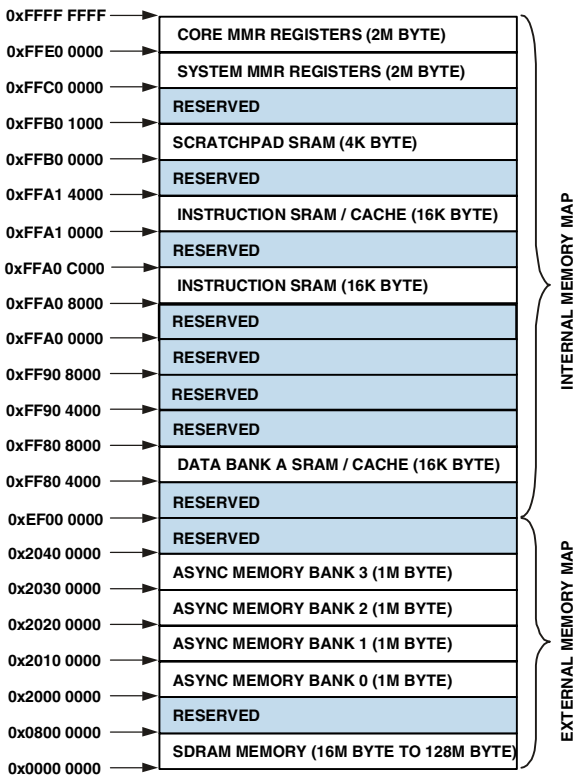


Figure 5. ADSP-BF531 Internal/External Memory Map

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks will only be contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one of which contains the control MMRs for all core functions, and the other of which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF531/2/3 processor contains a small boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF531/2/3 processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 13.

Event Handling

The event controller on the ADSP-BF531/2/3 processor handles all asynchronous and synchronous events to the processor. The ADSP-BF531/2/3 processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Non-Maskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception will be taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/2/3 processor Event Controller consists of two stages, the Core Event Controller (CEC) and the System Interrupt Controller (SIC). The Core Event Controller works with the System Interrupt Controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-BF531/2/3 processor. Table 2 describes the inputs to the CEC, identifies their names in the Event Vector Table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The System Interrupt Controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF531/2/3 processor provides a default mapping, the user can alter the mappings and priorities of

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Non-Maskable Interrupt	NMI
3	Exception	EVX
4	Reserved	
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

interrupt events by writing the appropriate values into the Interrupt Assignment Registers (IAR). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Event Control

The ADSP-BF531/2/3 processor provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide:

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC Interrupt Pending Register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA Error	IVG7
PPI Error	IVG7
SPORT 0 Error	IVG7
SPORT 1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Real-Time Clock	IVG8
DMA Channel 0 (PPI)	IVG8
DMA Channel 1 (SPORT 0 RX)	IVG9
DMA Channel 2 (SPORT 0 TX)	IVG9
DMA Channel 3 (SPORT 1 RX)	IVG9
DMA Channel 4 (SPORT 1 TX)	IVG9
DMA Channel 5 (SPI)	IVG10
DMA Channel 6 (UART RX)	IVG10
DMA Channel 7 (UART TX)	IVG10
Timer 0	IVG11
Timer 1	IVG11
Timer 2	IVG11
PF Interrupt A	IVG12
PF Interrupt B	IVG12
DMA Channels 8 and 9 (Memory DMA Stream 1)	IVG13
DMA Channels 10 and 11 (Memory DMA Stream 0)	IVG13
Software Watchdog Timer	IVG13

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC Interrupt Mask Register (SIC_IMASK)– This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in the register, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC Interrupt Status Register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC Interrupt Wakeup Enable Register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. (For more information, see Dynamic Power Management on Page 11.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/2/3 processor has multiple, independent DMA controllers that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the ADSP-BF531/2/3 processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-BF531/2/3 processor DMA controller supports both 1-dimensional (1D) and 2-dimensional (2D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF531/2/3 processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels provided for transfers between the various memories of the ADSP-BF531/2/3 processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor based methodology or by a standard register based autobuffer mechanism.

REAL-TIME CLOCK

The ADSP-BF531/2/3 processor Real-Time Clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 KHz crystal external to the ADSP-BF531/2/3 processor. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low-power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

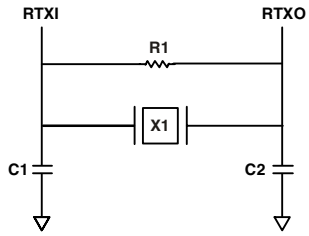
The 32.768 KHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from Sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from Deep Sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.



SUGGESTED COMPONENTS:
ECLIPTEK EC38J (THROUGH-HOLE PACKAGE)
EPSON MC405 12 PF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 PF
C2 = 22 PF
R1 = 10 M OHM

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 PF.

Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/2/3 processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, non-maskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the ADSP-BF531/2/3 processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/2/3 processor. Three timers have an external pin that can be configured either as a Pulse-Width Modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse-widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin, an external clock input to the PPI_CLK pin, or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an auto-baud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTS)

The ADSP-BF531/2/3 processor incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/2/3 processor has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (Serial Clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured Programmable Flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_Baud}$$

Where the 16-bit SPI_Baud register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/2/3 processor provides a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (Programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (Direct Memory Access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/ 1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 to12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

Where the 16-bit UART_Divisor comes from the DLH register (most significant 8 bits) and DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PROGRAMMABLE FLAGS (PFX)

The ADSP-BF531/2/3 processor has 16 bidirectional, general-purpose Programmable Flag (PF15–0) pins. Each programmable flag can be individually controlled by manipulation of the flag control, status and interrupt registers:

- Flag Direction Control Register – Specifies the direction of each individual PFx pin as input or output.
- Flag Control and Status Registers – The ADSP-BF531/2/3 processor employs a "write one to modify" mechanism that allows any combination of individual flags to be modified in a single instruction, without affecting the level of any other flags. Four control registers are provided. One register is written in order to set flag values, one register is written in order to clear flag values, one register is written in order to toggle flag values, and one register is written in order to specify a flag value. Reading the flag status register allows software to interrogate the sense of the flags.
- Flag Interrupt Mask Registers – The two Flag Interrupt Mask Registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two Flag Control Registers that are used to set and clear individual flag values, one Flag Interrupt Mask Register sets bits to enable interrupt function, and the other Flag Interrupt Mask register clears bits to disable interrupt function. PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.
- Flag Interrupt Sensitivity Registers – The two Flag Interrupt Sensitivity Registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processor provides a Parallel Peripheral Interface (PPI) that can connect directly to parallel A/D and D/A converters, ITU-R 601/656 video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to 3 frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate.

In ITU-R 656 modes, the PPI receives and parses a data stream of 8-bit or 10-bit data elements. On-chip decode of embedded preamble control and synchronization information is supported.

Three distinct ITU-R 656 modes are supported:

- Active Video Only - The PPI does not read in any data between the End of Active Video (EAV) and Start of Active Video (SAV) preamble symbols, or any data present during

the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI.

- Vertical Blanking Only - The PPI only transfers Vertical Blanking Interval (VBI) data, as well as horizontal blanking information and control byte sequences on VBI lines.
- Entire Field - The entire incoming bitstream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals.

Though not explicitly supported, ITU-R 656 output functionality can be achieved by setting up the entire frame structure (including active video, blanking, and control information) in memory and streaming the data out the PPI in a frame sync-less mode. The processor's 2D DMA features facilitate this transfer by allowing the static frame buffer (blanking and control codes) to be placed in memory once, and simply updating the active video information on a per-frame basis.

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. The modes are divided into four main categories, each allowing up to 16 bits of data transfer per PPI_CLK cycle:

- Data Receive with Internally Generated Frame Syncs
- Data Receive with Externally Generated Frame Syncs
- Data Transmit with Internally Generated Frame Syncs
- Data Transmit with Externally Generated Frame Syncs

These modes support ADC/DAC connections, as well as video communication with hardware signaling. Many of the modes support more than one level of frame synchronization. If desired, a programmable delay can be inserted between assertion of a frame sync and reception/transmission of data.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/2/3 processor provides five operating modes, each with a different performance/power profile. In addition, Dynamic Power Management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the ADSP-BF531/2/3 processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the Full-On mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the Active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the Full-On mode is entered. DMA access is available to appropriately configured L1 memories.

In the Active mode, it is possible to disable the PLL through the PLL Control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the Full-On or Sleep modes.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled		Disabled	Enabled	On
Deep Sleep	Disabled		Disabled	Disabled	On
Hibernate	Disabled		Disabled	Disabled	Off

Hibernate Operating Mode—Maximum Static Power Savings

The Hibernate mode maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins tri-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current. The internal supply regulator can be woken up either by a Real-Time Clock wakeup or by asserting the $\overline{\text{RESET}}$ pin.

Sleep Operating Mode—High Dynamic Power Savings

The Sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the Sleep mode, assertion of wakeup will cause the processor to sense the value of the BYPASS bit in the PLL Control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the Full On mode. If BYPASS is enabled, the processor will transition to the Active mode.

When in the Sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The Deep Sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such

as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in Deep Sleep mode, an RTC asynchronous interrupt causes the processor to transition to the Active mode. Assertion of $\overline{\text{RESET}}$ while in Deep Sleep mode causes the processor to transition to the Full-On mode.

Power Savings

As shown in Table 5, the ADSP-BF531/2/3 processor supports three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF531/2/3 processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of Dynamic Power Management, without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	VDD Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The Dynamic Power Management feature of the ADSP-BF531/2/3 processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the Power Savings Factor and % Power Savings calculations.

The Power Savings Factor is calculated as:

$$\textit{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

where the variables in the equations are:

- $f_{CCLKNOM}$ is the nominal core clock frequency
- $f_{CCLKRED}$ is the reduced core clock frequency
- $V_{DDINTNOM}$ is the nominal internal supply voltage
- $V_{DDINTRED}$ is the reduced internal supply voltage
- T_{NOM} is the duration running at $f_{CCLKNOM}$
- T_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ \textit{Power Savings} = (1 - \textit{Power Savings Factor}) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate processor core voltage levels 0.85V(-5% / +10%) to 1.2V(-5% / +10%) from an external 2.25 V to 3.6 V supply. Figure 7 shows the typical external components required to complete the power management system.* The regulator controls the internal logic voltage levels and is programmable with the Voltage Regulator Control Register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in hibernation, V_{DDEXT} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

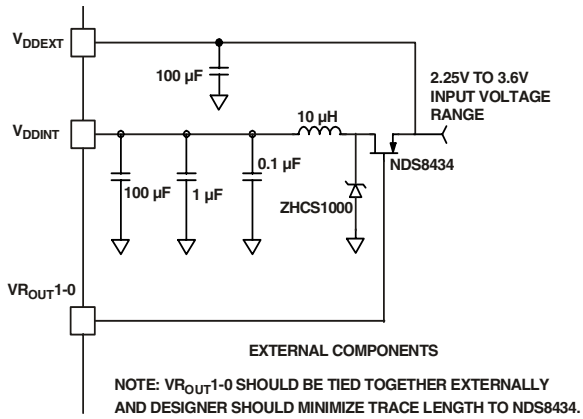


Figure 7. Voltage Regulator Circuit

CLOCK SIGNALS

The ADSP-BF531/2/3 processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

* See EE-228: Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors.

Alternatively, because the ADSP-BF531/2/3 processor includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 8. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

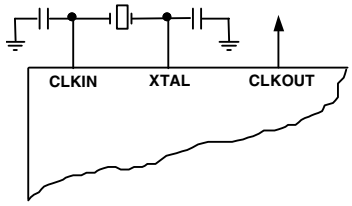


Figure 8. External Crystal Connections

As shown in Figure 9 on Page 13, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 1x to 63x multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10x, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

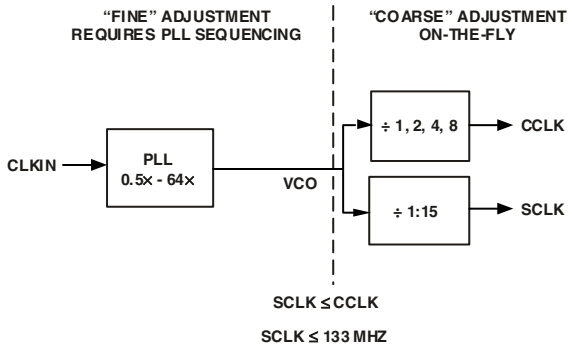


Figure 9. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0011	3:1	400	133
1010	10:1	500	50

The maximum frequency of the system clock is f_{SCLK}. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

BOOTING MODES

The ADSP-BF531/2/3 processor has two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE1 – 0	Description
00	Execute from 16-Bit External Memory (Bypass Boot ROM)
01	Boot from 8-Bit or 16-Bit FLASH
10	Reserved
11	Boot from SPI Serial EEPROM (8-, 16-, or 24-Bit address range)

The BMODE pins of the Reset Configuration Register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external FLASH memory – The FLASH boot routine located in boot ROM memory space is set up using Asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM (8, 16, or 24-bit addressable) – The SPI uses the PF2 output pin to select a single SPI EEPROM device, submits successive read commands at addresses 0x00, 0x0000, and 0x000000 until a valid 8, 16, or 24-bit addressable EEPROM is detected, and begins clocking data into the beginning of L1 instruction memory.

For each of the boot modes, an 10-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, bit 4 of the Reset Configuration Register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16- and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

The ADSP-BF531/2/3 processor is supported with a complete set of CROSSCORE®[†] software and hardware development tools, including Analog Devices emulators and VisualDSP++®[‡] development environment. The same emulator hardware that supports other Blackfin processors also fully emulates the ADSP-BF531/2/3 processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to processor assembly. The processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information).
- Insert breakpoints.

[†] CROSSCORE is a registered trademark of Analog Devices, Inc.
[‡] VisualDSP++ is a registered trademark of Analog Devices, Inc.

- Set conditional breakpoints on registers, memory, and stacks.
- Trace instruction execution.
- Perform linear or statistical profiling of program execution.
- Fill, dump, and graphically plot the contents of memory.
- Perform source level debugging.
- Create custom debugger windows.

The VisualDSP++ IDDE lets programmers define and manage software development. Its dialog boxes and property pages let programmers configure and manage all of the Blackfin development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include Threads, Critical and Unscheduled regions, Semaphores, Events, and Device flags. The VDK also supports Priority-based, Preemptive, Cooperative, and Time-Sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VCSE is Analog Devices technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with the drag of the mouse, examine run time stack and heap usage. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG Test Access Port of the ADSP-BF531/2/3 processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Non-intrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family. Hardware tools include Blackfin processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

DESIGNING AN EMULATOR COMPATIBLE PROCESSOR BOARD

The Analog Devices family of emulators are tools that every system developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices web site (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

PIN DESCRIPTIONS

ADSP-BF531/2/3 processor pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the Memory Interface, Asynchronous Memory Control, and Synchronous Memory Control pins, which are driven high.

If $\overline{BR}$ is active, then the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pullups or pulldowns as noted in the table footnotes.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

Pin Name	I/O	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A[2]
DATA15–0	I/O	Data Bus for Async/Sync Access	A[2]
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A[2]
$\overline{BR}$[3]	I	Bus Request	
$\overline{BG}$	O	Bus Grant	A[2]
$\overline{BGH}$	O	Bus Grant Hang	A[2]
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select	A[2]
ARDY	I	Hardware Ready Control	
$\overline{AOE}$	O	Output Enable	A[2]
$\overline{ARE}$	O	Read Enable	A[2]
$\overline{AWE}$	O	Write Enable	A[2]
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A[2]
$\overline{SCAS}$	O	Column Address Strobe	A[2]
$\overline{SWE}$	O	Write Enable	A[2]
SCKE	O	Clock Enable	A[2]
CLKOUT	O	Clock Output	B[4]
SA10	O	A10 Pin	A[2]
$\overline{SMS}$	O	Bank Select	A[2]
Timers			
TMR0	I/O	Timer 0	C[5]
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C[5]
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C[5]

Table 9. Pin Descriptions (Continued)

Pin Name	I/O	Function	Driver Type[1]
Parallel Peripheral Interface Port/GPIO			
PF0/*SPISS*	I/O	Programmable Flag 0/*SPI Slave Select Input*	C[5]
PF1/*SPISEL1/TMRCLK*	I/O	Programmable Flag 1/*SPI Slave Select Enable 1/External Timer Reference*	C[5]
PF2/*SPISEL2*	I/O	Programmable Flag 2/*SPI Slave Select Enable 2*	C[5]
PF3/*SPISEL3/PPI_FS3*	I/O	Programmable Flag 3/*SPI Slave Select Enable 3/PPI Frame Sync 3*	C[5]
PF4/*SPISEL4/PPI15*	I/O	Programmable Flag 4/*SPI Slave Select Enable 4 / PPI 15*	C[5]
PF5/*SPISEL5/PPI14*	I/O	Programmable Flag 5/*SPI Slave Select Enable 5 / PPI 14*	C[5]
PF6/*SPISEL6/PPI13*	I/O	Programmable Flag 6/*SPI Slave Select Enable 6 / PPI 13*	C[5]
PF7/*SPISEL7/PPI12*	I/O	Programmable Flag 7/*SPI Slave Select Enable 7 / PPI 12*	C[5]
PF8/*PPI11*	I/O	Programmable Flag 8/*PPI 11*	C[5]
PF9/*PPI10*	I/O	Programmable Flag 9/*PPI 10*	C[5]
PF10/*PPI9*	I/O	Programmable Flag 10/*PPI 9*	C[5]
PF11/*PPI8*	I/O	Programmable Flag 11/*PPI 8*	C[5]
PF12/*PPI7*	I/O	Programmable Flag 12/*PPI 7*	C[5]
PF13/*PPI6*	I/O	Programmable Flag 13/*PPI 6*	C[5]
PF14/*PPI5*	I/O	Programmable Flag 14/*PPI 5*	C[5]
PF15/*PPI4*	I/O	Programmable Flag 15/*PPI 4*	C[5]
PPI3–0	I/O	PPI3–0	C[5]
PPI_CLK	I	PPI Clock	C[5]
Serial Ports			
RSCLK0	I/O	SPORT0 Receive Serial Clock	D[6]
RFS0	I/O	SPORT0 Receive Frame Sync	C[5]
DR0PRI	I	SPORT0 Receive Data Primary	
DR0SEC	I	SPORT0 Receive Data Secondary	
TSCLK0	I/O	SPORT0 Transmit Serial Clock	D[6]
TFS0	I/O	SPORT0 Transmit Frame Sync	C[5]
DT0PRI	O	SPORT0 Transmit Data Primary	C[5]
DT0SEC	O	SPORT0 Transmit Data Secondary	C[5]
RSCLK1	I/O	SPORT1 Receive Serial Clock	D[6]
RFS1	I/O	SPORT1 Receive Frame Sync	C[5]
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D[6]
TFS1	I/O	SPORT1 Transmit Frame Sync	C[5]
DT1PRI	O	SPORT1 Transmit Data Primary	C[5]
DT1SEC	O	SPORT1 Transmit Data Secondary	C[5]
SPI Port			
MOSI	I/O	Master Out Slave In	C[5]
MISO[7]	I/O	Master In Slave Out	C[5]
SCK	I/O	SPI Clock	D[6]

Table 9. Pin Descriptions (Continued)

Pin Name	I/O	Function	Driver Type[1]
UART Port			
RX	I	UART Receive	
TX	O	UART Transmit	C[5]
Real Time Clock			
RTXI[8]	I	RTC Crystal Input	
RTXO	O	RTC Crystal Output	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C[5]
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$[9]	I	JTAG Reset	
$\overline{\text{EMU}}$	O	Emulation Output	C[5]
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output	
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
NMI[8]	I	Non-maskable Interrupt	
BMODE1–0	I	Boot Mode Strap	
Voltage Regulator			
VROUT1–0	O	External FET Drive	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Core Power Supply	
V_{DDRTC}	P	Real Time Clock Power Supply	
GND	G	External Ground	

[1] Refer to Figure 26 on Page 39 to Figure 30 on Page 40.
[2] See Figure 25 and Figure 26 on Page 39
[3] This pin should be pulled HIGH when not used.
[4] See Figure 27 and Figure 28 on Page 39
[5] See Figure 29 and Figure 30 on Page 40
[6] See Figure 31 and Figure 32 on Page 40
[7] This pin should always be pulled HIGH through a 4.7K Ohm resistor if booting via the SPI port.
[8] This pin should always be pulled LOW when not used.
[9] This pin should be pulled LOW if the JTAG port will not be used.

SPECIFICATIONS

Component specifications are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Parameter		Minimum	Nominal	Maximum	Unit
V_{DDINT}	Internal Supply Voltage	0.8	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	2.25	2.5 or 3.3	3.6	V
V_{DDRTC}	Real-time Clock Power Supply Voltage	2.25		3.6	V
V_{IH}	High Level Input Voltage[1, 2] @ V_{DDEXT}=maximum	2.0		3.6	V
$V_{IHCLKIN}$	High Level Input Voltage[3] @ V_{DDEXT}=maximum	2.2		3.6	V
V_{IL}	Low Level Input Voltage[2, 4] @ V_{DDEXT}=minimum	–0.3		0.6	V

[1] The ADSP-BF531/2/3 processor is 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[2] Parameter value applies to all input and bidirectional pins except CLKIN.

[3] Parameter value applies to CLKIN pin only.

[4] Parameter value applies to all input and bidirectional pins.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Maximum	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = 3.0V, I_{OH} = –0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = 3.0V, I_{OL} = 2.0 mA		0.4	V
I_{IH}	High Level Input Current[2]	@ V_{DDEXT} = maximum, V_{IN} = V_{DD} maximum		10.0	µA
I_{IHP}	High Level Input Current JTAG[3]	@ V_{DDEXT}=maximum, V_{IN} = V_{DD} maximum		20.0	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT}=maximum, V_{IN} = 0 V		10.0	µA
I_{OZH}	Three-State Leakage Current[4]	@ V_{DDEXT}= maximum, V_{IN} = V_{DD} maximum		10.0	µA
I_{OZL}	Three-State Leakage Current[5]	@ V_{DDEXT}= maximum, V_{IN} = 0 V		10.0	µA
C_{IN}	Input Capacitance[5, 6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		8.0	pF

[1] Applies to output and bidirectional pins.

[2] Applies to input pins except JTAG inputs.

[3] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).

[4] Applies to three-statable pins.

[5] Applies to all signal pins.

[6] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in the table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, $\overline{ABE1–0}$/SDQM1–0, CLKOUT, SCKE, SA10, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, and $\overline{SMS}$.

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage	–0.5 V to 3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
ADSP-BF533 Core Clock (CCLK)	600 MHz
ADSP-BF532/BF531 Core Clock (CCLK)	400 MHz
Peripheral Clock (SCLK)	133 MHz
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-BF531/2/3 processor features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Table 10 through Table 14 describe the timing requirements for the ADSP-BF531/2/3 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock as described in Absolute Maximum Ratings on Page 20, and the Voltage Controlled Oscillator (VCO) operating frequencies described in Table 13. Table 13 describes Phase-Locked Loop operating conditions.

Table 10. Core and System Clock Requirements—ADSP-BF533SKBC600

Parameter		Min	Max	Unit
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.2 V – 5%)	1.67		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.1 V – 5%)	2.10		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.0 V – 5%)	2.35		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.9 V – 5%)	2.66		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.8 V)	4.00		ns
t_{SCLK}	System Clock Period	Maximum of 7.5 or t_{CCLK}		ns

Table 11. Core and System Clock Requirements—ADSP-BF533SBBC500 and ADSP-BF533SBBZ500

Parameter		Min	Max	Unit
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.2 V – 5%)	2.0		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.1 V – 5%)	2.25		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.0 V – 5%)	2.50		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.9 V – 5%)	3.00		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.8 V)	4.00		ns
t_{SCLK}	System Clock Period	Maximum of 7.5 or t_{CCLK}		ns

Table 12. Core and System Clock Requirements—ADSP-BF532/531 All Package Types

Parameter		Min	Max	Unit
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.2 V – 5%)	2.5		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.1 V – 5%)	2.75		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 1.0 V – 5%)	3.00		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.9 V – 5%)	3.25		ns
t_{CCLK}	Core Cycle Period (V_{DDINT} = 0.8 V)	4.0		ns
t_{SCLK}	System Clock Period	Maximum of 7.5 or t_{CCLK}		ns

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max CCLK	MHz

Table 14. Maximum SCLK Conditions

Parameter	Condition	V_{DDEXT} = 3.3 V	V_{DDEXT} = 2.5 V	Unit
MBGA				
f_{SCLK}	V_{DDINT} >= 1.14 V	133	133	MHz
f_{SCLK}	V_{DDINT} < 1.14 V	100	100	MHz
LQFP				
f_{SCLK}	V_{DDINT} >= 1.14 V	133	133[1]	MHz
f_{SCLK}	V_{DDINT} < 1.14 V	83	83[1]	MHz

[1] Set bit 7 (output delay) of PLL_CTL register.

Clock and Reset Timing

Table 15 and Figure 10 describe clock and reset operations. Per Absolute Maximum Ratings on Page 20, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of 600/133 MHz.

Table 15. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[1]	10.0		ns
t_{CKINH}	CLKIN High Pulse[1]	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[2]	11 t_{CKIN}		ns

[1] Applies to bypass mode and non-bypass mode.
[2] Applies after power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles, while $\overline{\text{RESET}}$ is asserted, assuming stable power supplies and CLKIN (not including start-up time of external clock oscillator).

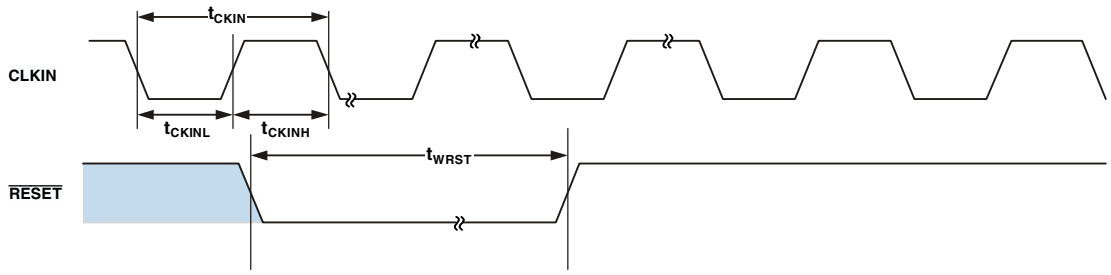


Figure 10. Clock and Reset Timing

Asynchronous Memory Read Cycle Timing

Table 16. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

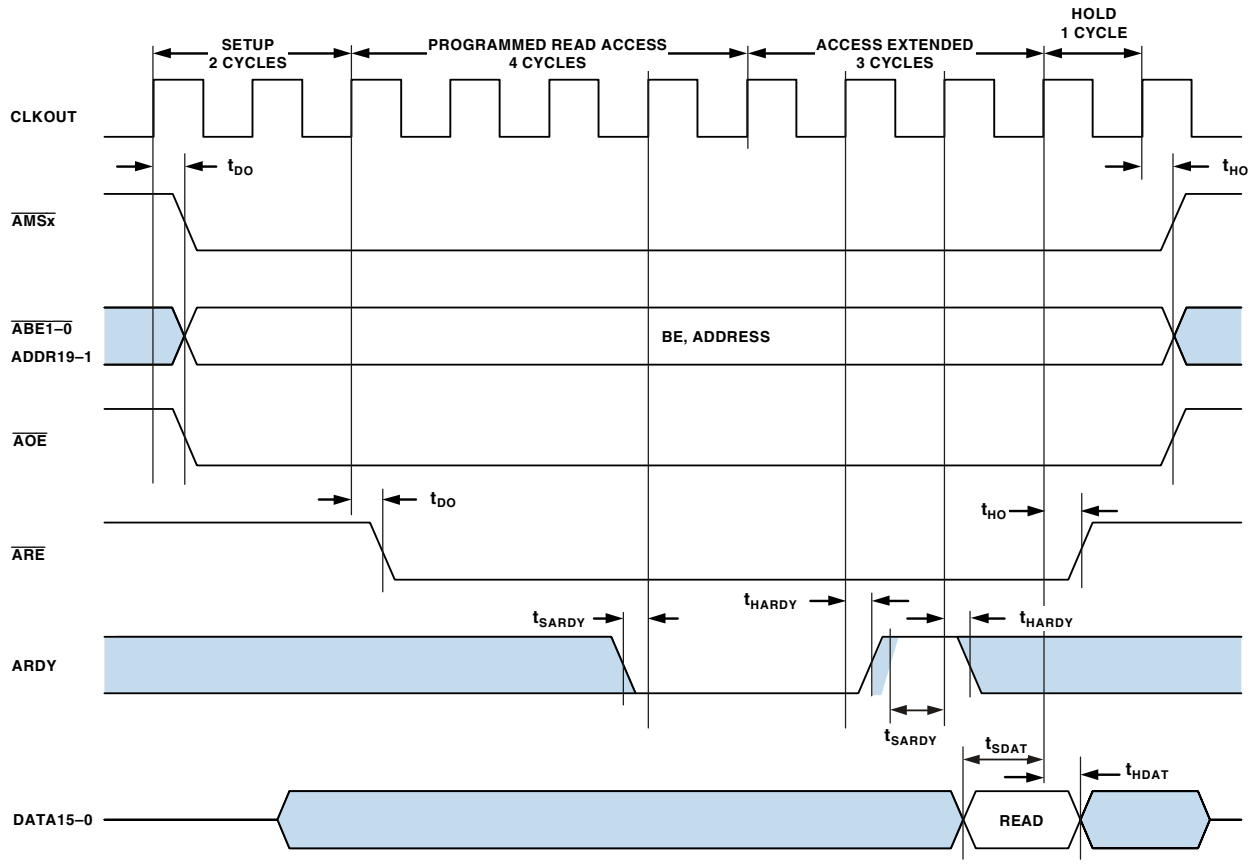


Figure 11. Asynchronous Memory Read Cycle Timing

Asynchronous Memory Write Cycle Timing

Table 17. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

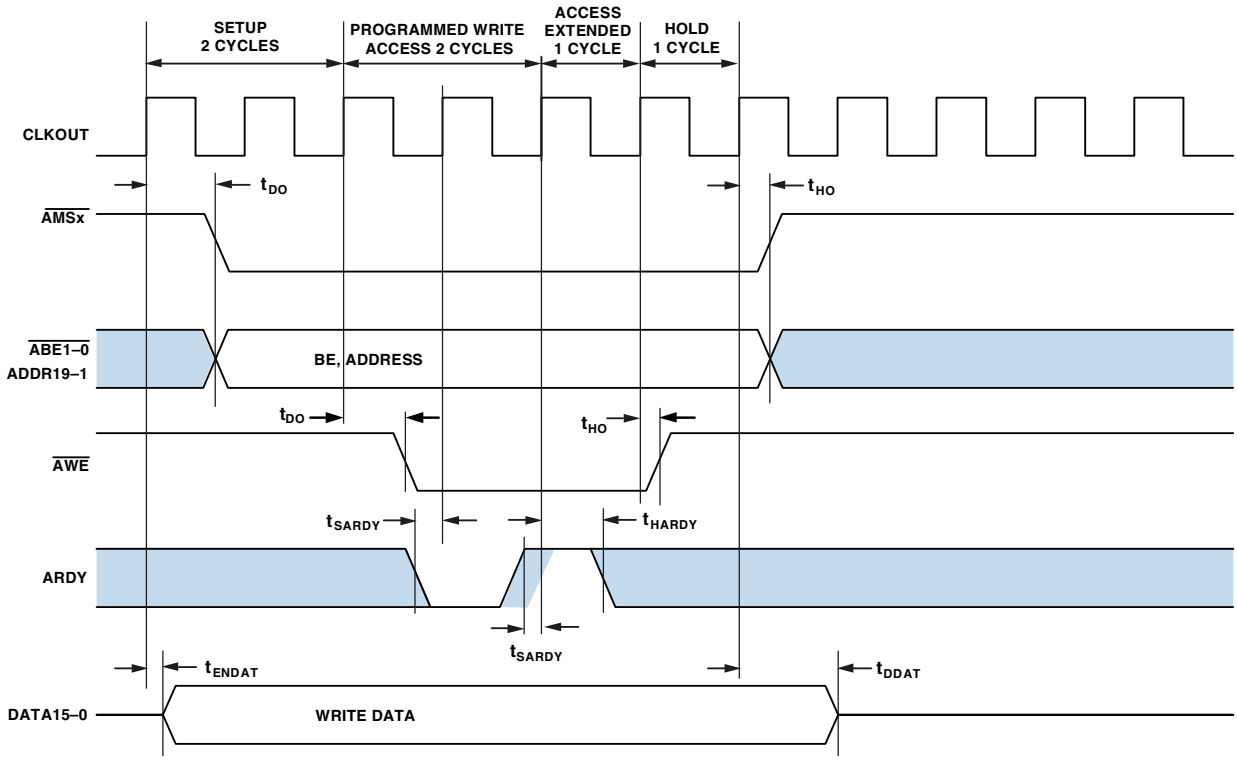


Figure 12. Asynchronous Memory Write Cycle Timing

SDRAM Interface Timing

Table 18. SDRAM Interface Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{SCLK}	CLKOUT Period	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[2]		6.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[1]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns

[1] For V_{DDINT} = 1.2 V.
[2] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

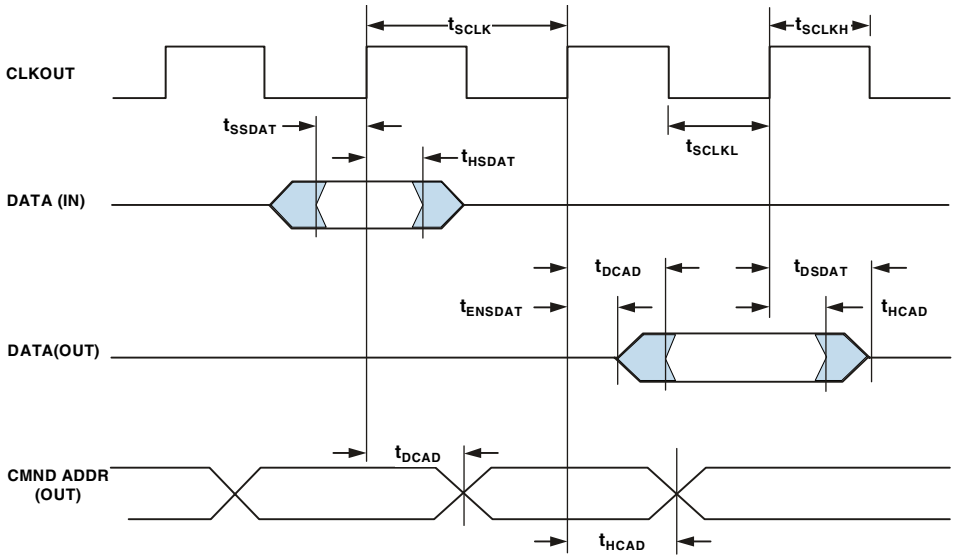


Figure 13. SDRAM Interface Timing

External Port Bus Request and Grant Cycle Timing

Table 19 and Figure 14 describe external port bus request and bus grant operations.

Table 19. External Port Bus Request and Grant Cycle Timing

Parameter[1, 2]		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT High Setup	4.6		ns
t_{BH}	CLKOUT High to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{xMS}$, Address, and $\overline{RD}/\overline{WR}$ disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{xMS}$, Address, and $\overline{RD}/\overline{WR}$ enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ High Setup		3.6	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		3.6	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ High Setup		3.6	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		3.6	ns

[1] These are preliminary timing parameters that are based on worst-case operating conditions.
[2] The pad loads for these timing parameters are 20 pF.

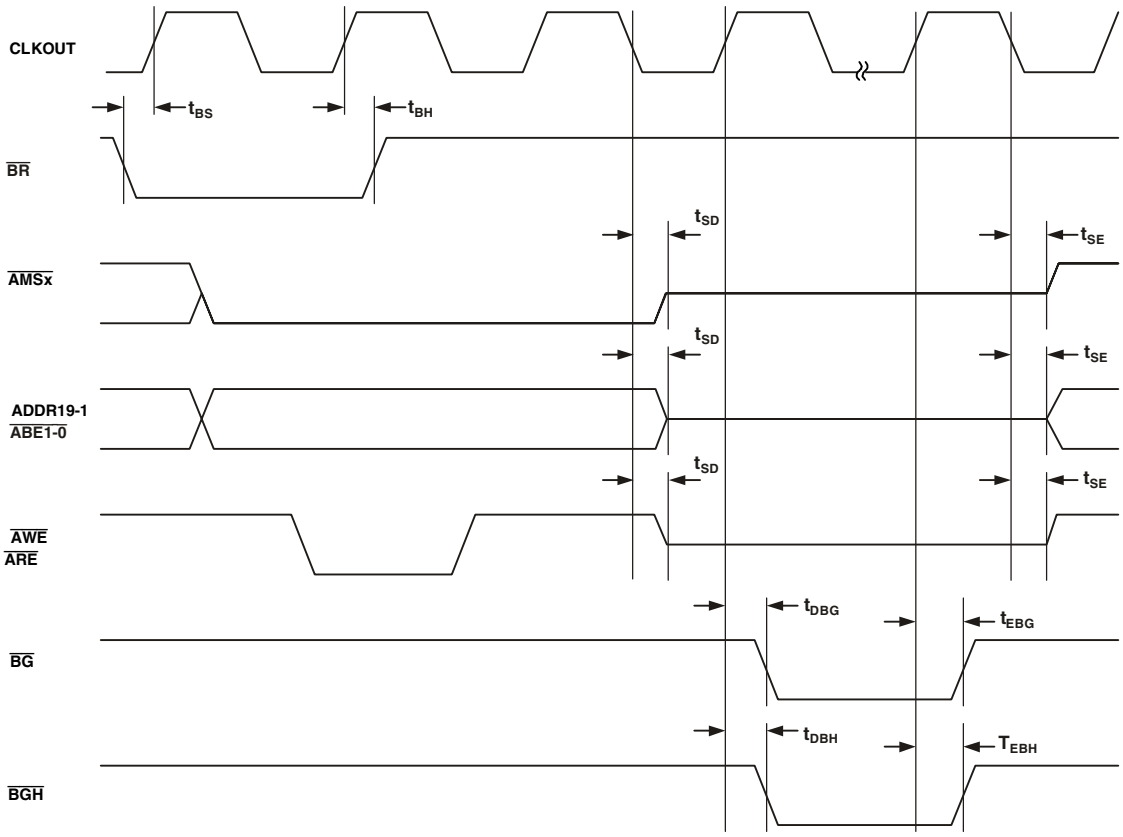


Figure 14. External Port Bus Request and Grant Cycle Timing

Parallel Peripheral Interface Timing

Table 20 and Figure 15 on Page 27 describe Parallel Peripheral Interface operations.

Table 20. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width	6.0		ns
t_{PCLK}	PPI_CLK Period[1]	15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK	3.0		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	3.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	2.0		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	4.0		ns
Switching Characteristics - GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		10.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	0.0		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		10.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	0.0		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

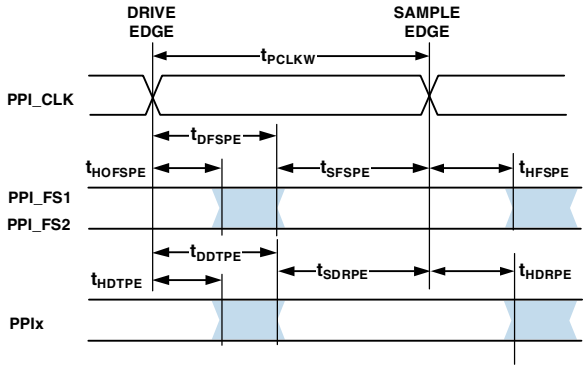


Figure 15. GP Output Mode and Frame Capture Timing

Serial Ports

Table 21 through Table 26 on Page 29 and Figure 16 on Page 30 through Figure 18 on Page 32 describe Serial Port operations.

Table 21. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TSCLK/RSCLK[1]	3.0		ns
t_{HFSE}	TFS/RFS Hold After TSCLK/RSCLK[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLK[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLK[1]	3.0		ns
t_{SCLKEW}	TSCLK/RSCLK Width	4.5		ns
t_{SCLKE}	TSCLK/RSCLK Period	15.0		ns

[1] Referenced to sample edge.

Table 22. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS/RFS Setup Before TSCLK/RSCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TSCLK/RSCLK[1]	–2.0		ns
t_{SDRI}	Receive Data Setup Before RSCLK[1]	6.0		ns
t_{HDRI}	Receive Data Hold After RSCLK[1]	0.0		ns
t_{SCLKEW}	TSCLK/RSCLK Width	4.5		ns
t_{SCLKE}	TSCLK/RSCLK Period	15.0		ns

[1] Referenced to sample edge.

Table 23. Serial Ports—External Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS/RFS Delay After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]		10.0	ns
t_{HOFSE}	TFS/RFS Hold After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLK[1]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLK[1]	0.0		ns

[1] Referenced to drive edge.

Table 24. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS/RFS Delay After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]		3.0	ns
t_{HOFSI}	TFS/RFS Hold After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]	–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLK[1]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLK[1]	–2.0		ns
t_{SCLKIW}	TSCLK/RSCLK Width	4.5		ns

[1] Referenced to drive edge.

Table 25. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLK[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLK[1]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLK[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLK[1]		3.0	ns

[1] Referenced to drive edge.

Table 26. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[1,2]	0		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2] If external RFS/TFS setup to RSCLK/TSCLK > $t_{SCLKE}/2$, then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

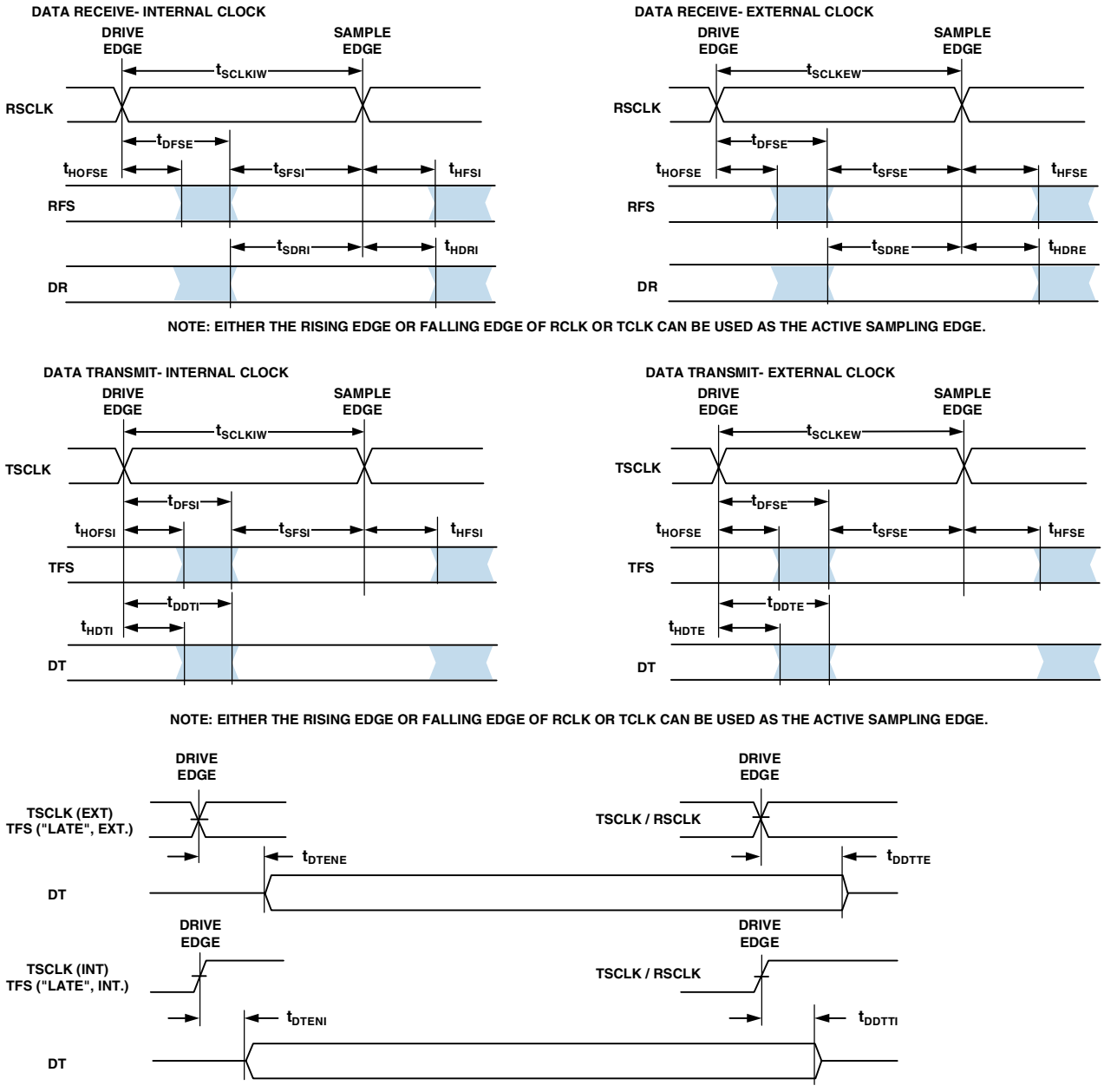
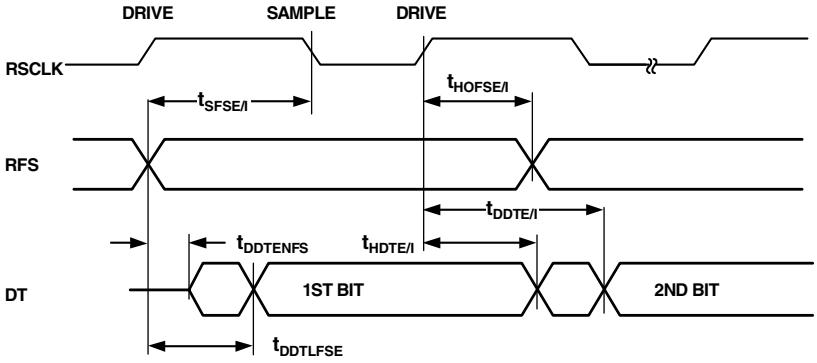


Figure 16. Serial Ports

EXTERNAL RFS WITH MCE = 1, MFD = 0



LATE EXTERNAL TFS

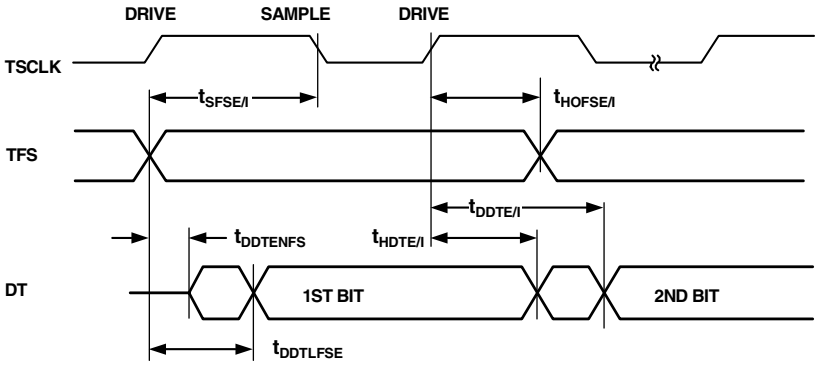
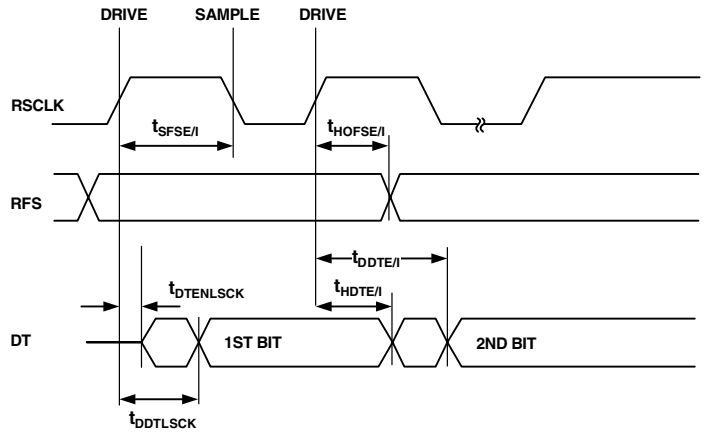


Figure 17. External Late Frame Sync (Frame Sync Setup < $t_{SCLKE}/2$)

EXTERNAL RFS WITH MCE = 1, MFD = 0



LATE EXTERNAL TFS

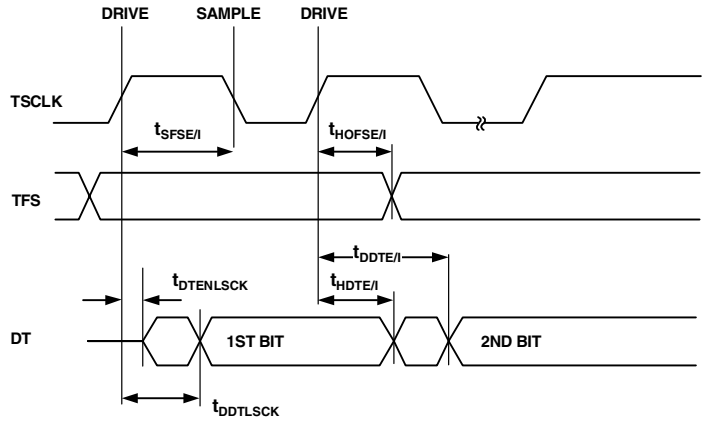


Figure 18. External Late Frame Sync (Frame Sync Setup > $t_{SCLKE}/2$)

Serial Peripheral Interface (SPI) Port —Master Timing

Table 27 and Figure 19 describe SPI port master operations.

Table 27. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK edge (x=0 or 1)	$2t_{SCLK}$ –1.5		ns
t_{SPICHM}	Serial Clock High period	$2t_{SCLK}$ – 1.5		ns
t_{SPICLM}	Serial Clock Low period	$2t_{SCLK}$ – 1.5		ns
t_{SPICLK}	Serial Clock Period	$4t_{SCLK}$ – 1.5		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High (x=0 or 1)	$2t_{SCLK}$ – 1.5		ns
t_{SPITDM}	Sequential Transfer Delay	$2t_{SCLK}$ – 1.5		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	4.0	ns

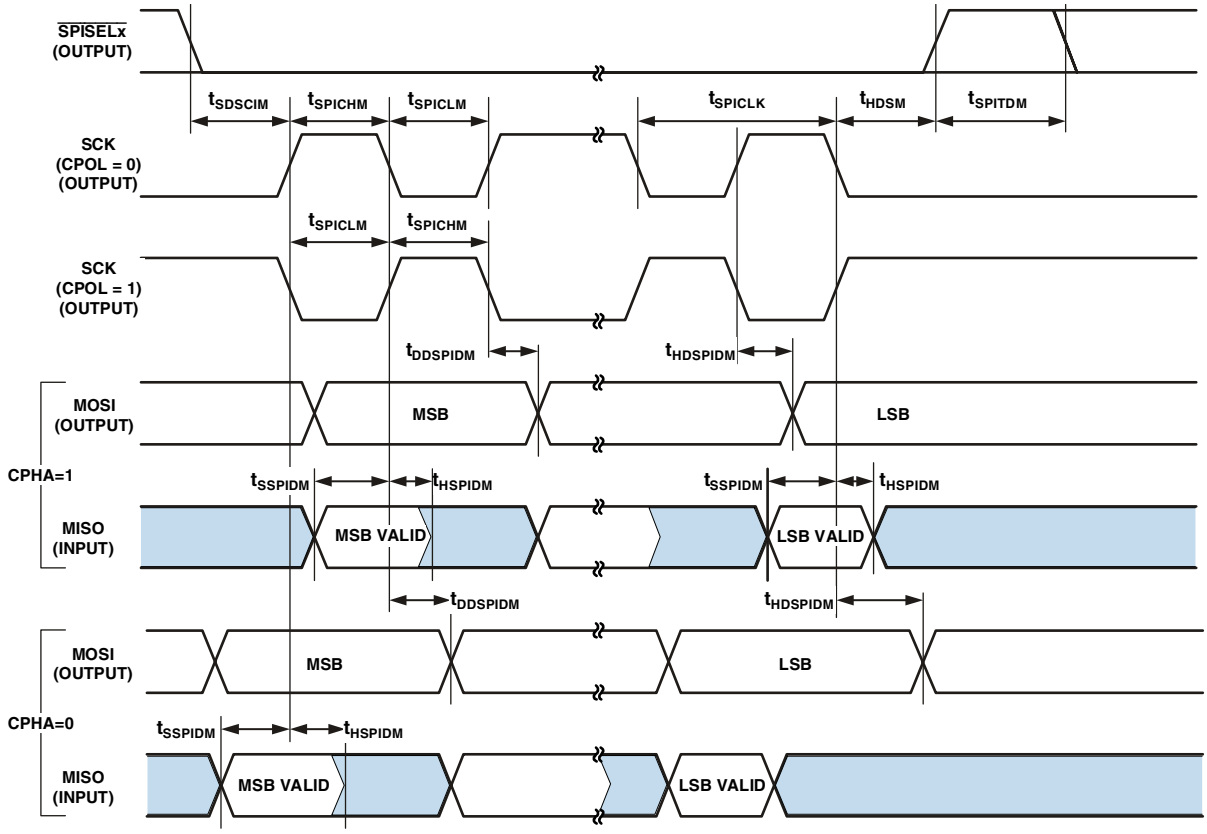


Figure 19. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port —Slave Timing

Table 28 and Figure 20 describe SPI port slave operations.

Table 28. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2t_{SCLK}-1.5$		ns
t_{SPICLS}	Serial Clock low Period	$2t_{SCLK}-1.5$		ns
t_{SPICLK}	Serial Clock Period	$4t_{SCLK}-1.5$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2t_{SCLK}-1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2t_{SCLK}-1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2t_{SCLK}-1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0	10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0	10	ns

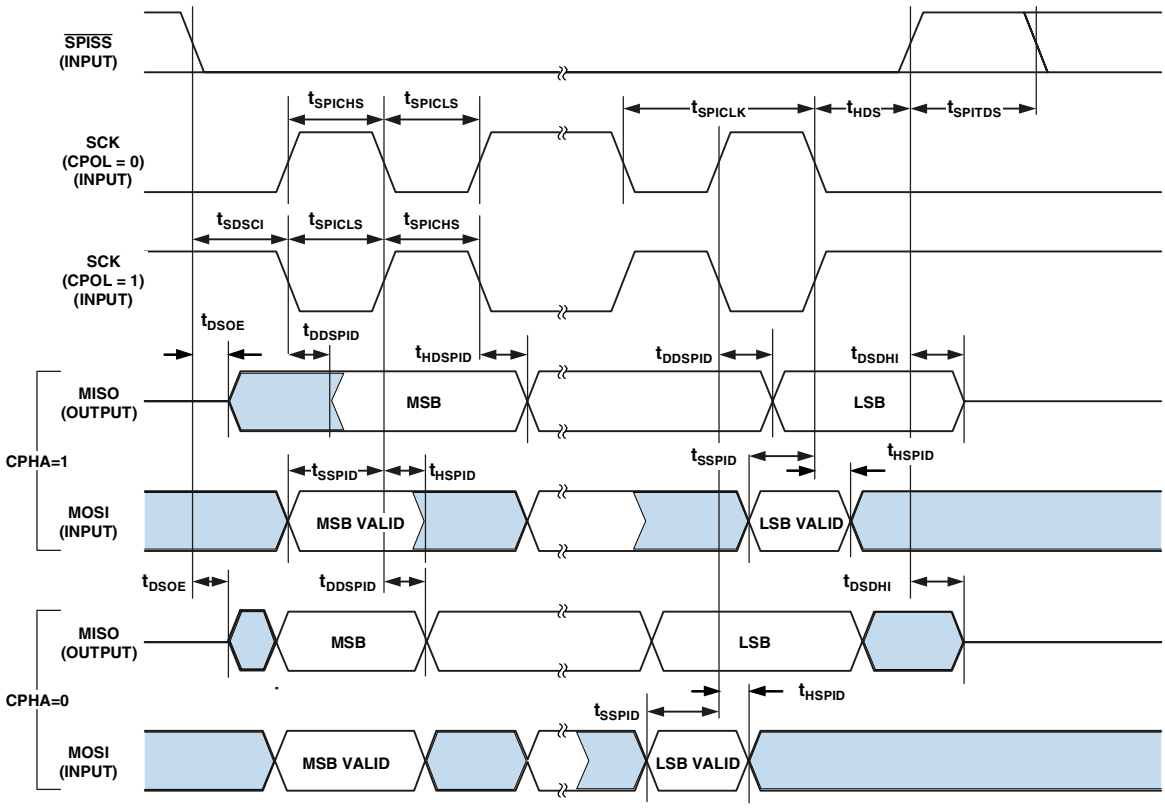


Figure 20. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 21 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 21 there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

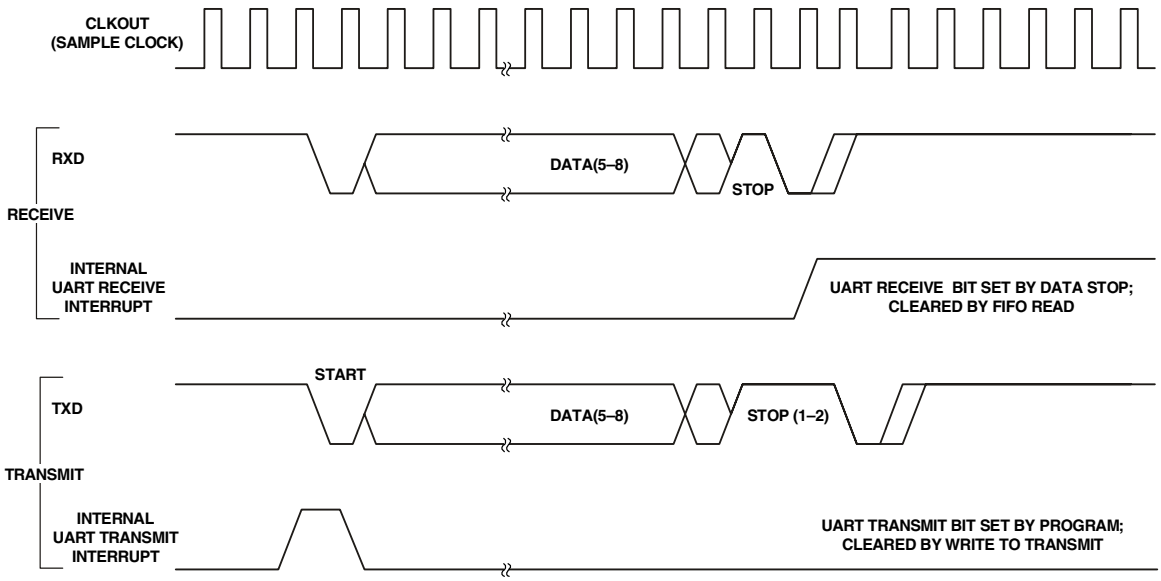


Figure 21. UART Port—Receive and Transmit Timing

Programmable Flags Cycle Timing

Table 29 and Figure 22 describe programmable flag operations.

Table 29. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{WFI}	Flag Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristics				
t_{DFO}	Flag Output Delay from CLKOUT Low		6	ns

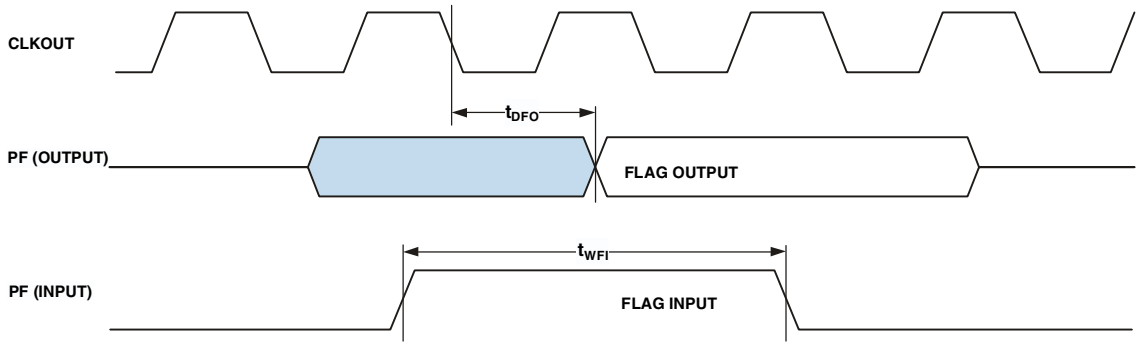


Figure 22. Programmable Flags Cycle Timing

Timer Cycle Timing

Table 30 and Figure 23 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 30. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1] (Measured in SCLK Cycles)	1		SCLK
t_{WH}	Timer Pulse Width Input High[1] (Measured in SCLK Cycles)	1		SCLK
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output[2] (Measured in SCLK Cycles)	1	$(2^{32}–1)$	SCLK

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.
[2] The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}–1)$ cycles.

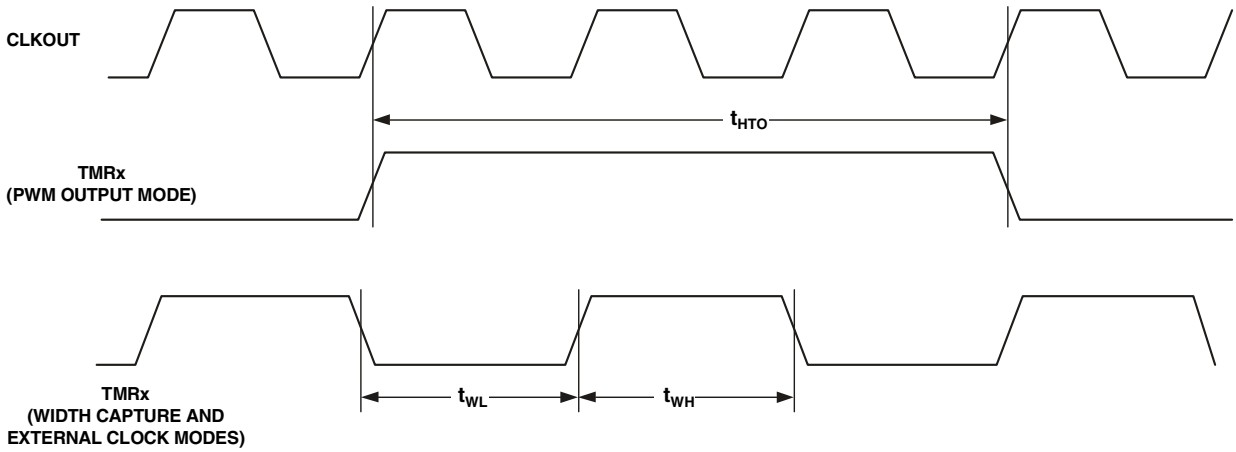


Figure 23. Timer PWM_OUT Cycle Timing

JTAG Test And Emulation Port Timing

Table 31 and Figure 24 describe JTAG port operations.

Table 31. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs=DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{\text{RESET}}$, NMI, BMODE1–0, $\overline{\text{BR}}$, PP3–0.

[2] 50 MHz maximum

[3] System Outputs=DATA15–0, ADDR19–1, $\overline{\text{ABE1–0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, PPI3–0.

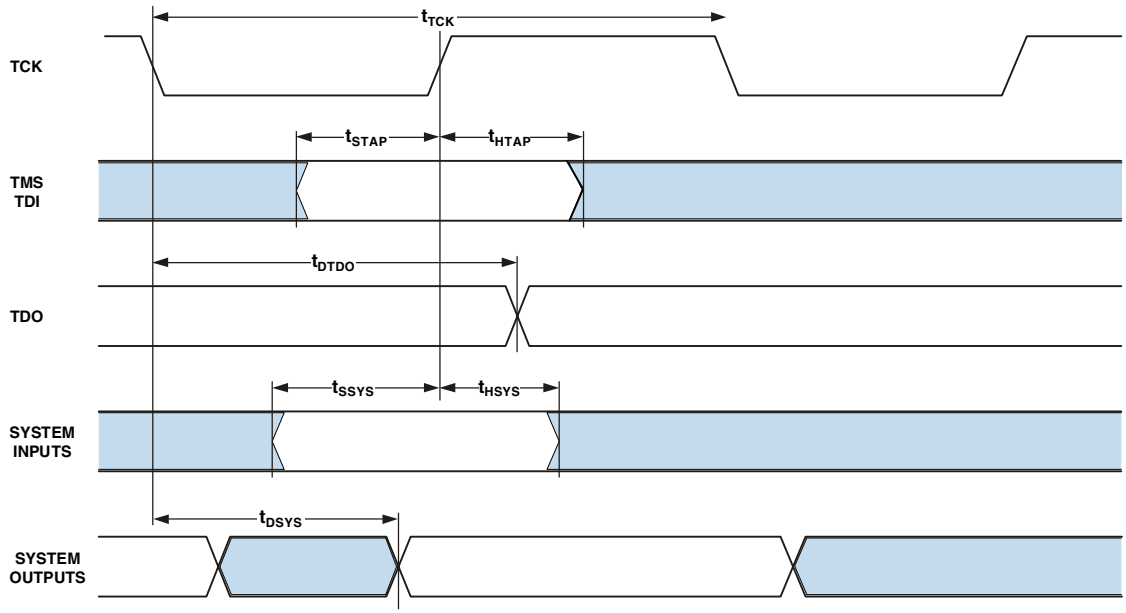


Figure 24. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 25 through Figure 32 show typical current-voltage characteristics for the output drivers of the ADSP-BF531/2/3 processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

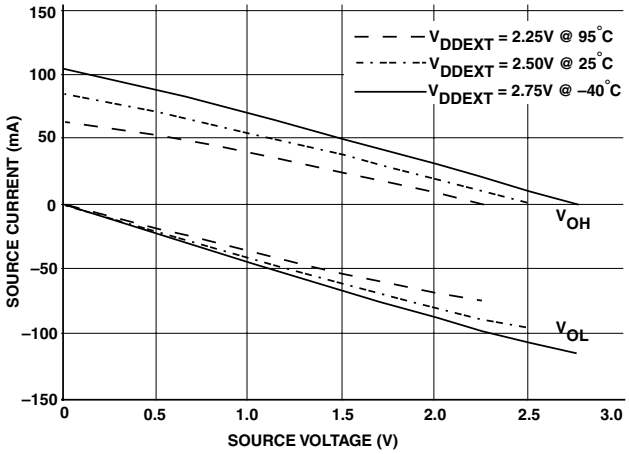


Figure 25. Drive Current A (Low V_{DDEXT})

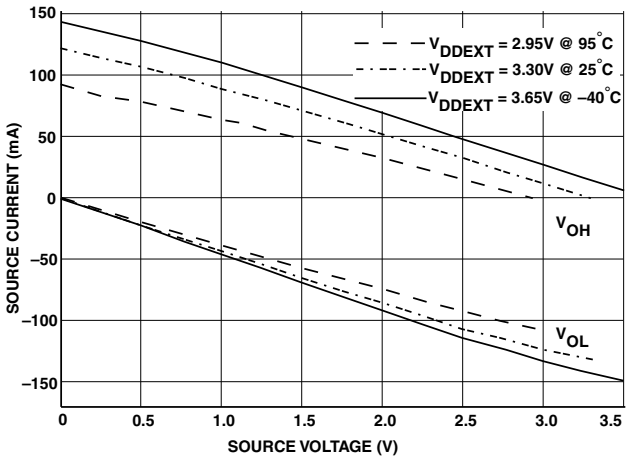


Figure 26. Drive Current A (High V_{DDEXT})

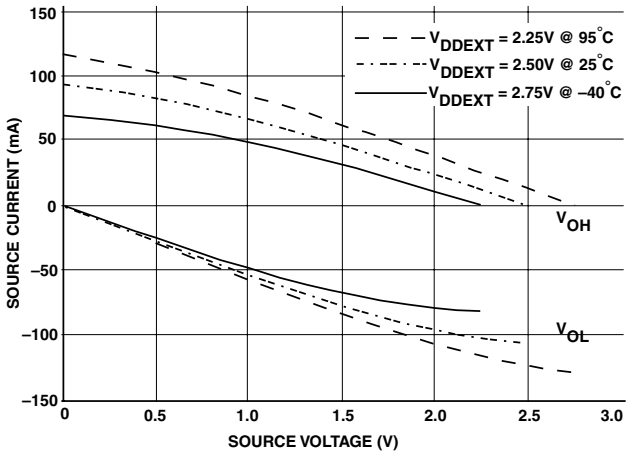


Figure 27. Drive Current B (Low V_{DDEXT})

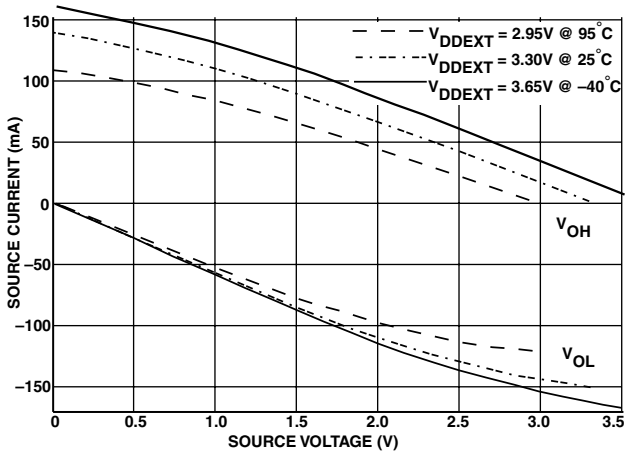


Figure 28. Drive Current B (High V_{DDEXT})

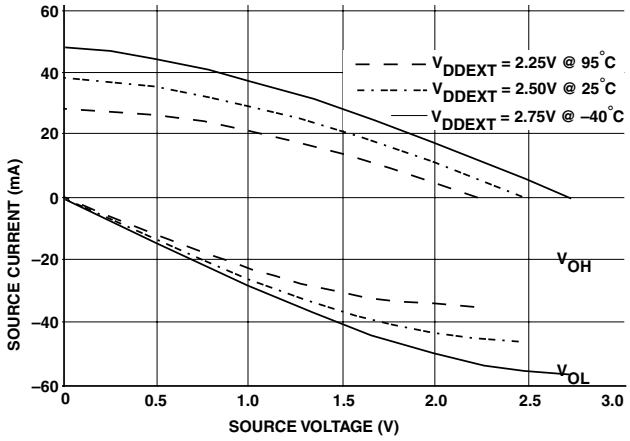


Figure 29. Drive Current C (Low V_{DDEXT})

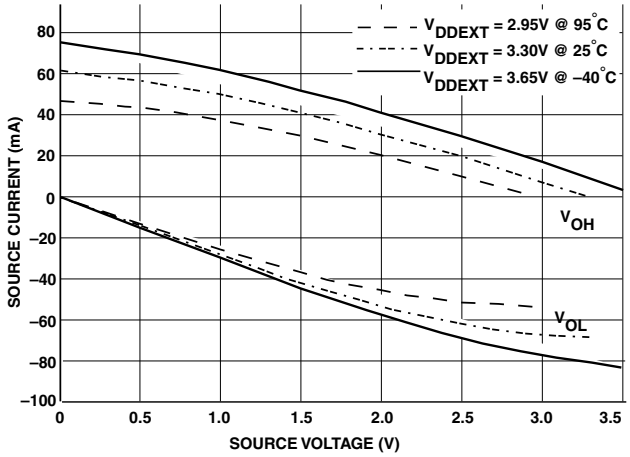


Figure 30. Drive Current C (High V_{DDEXT})

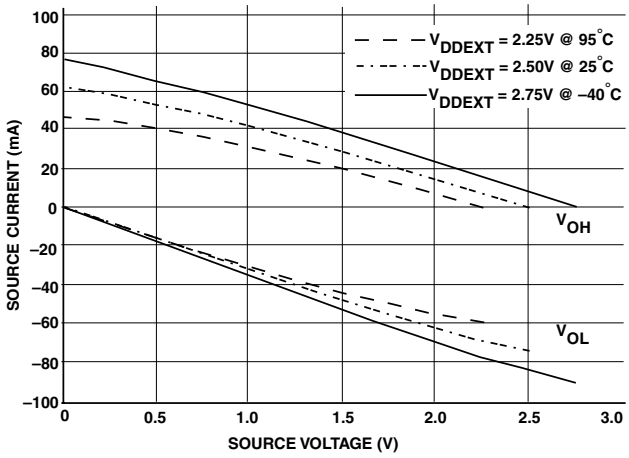


Figure 31. Drive Current D (Low V_{DDEXT})

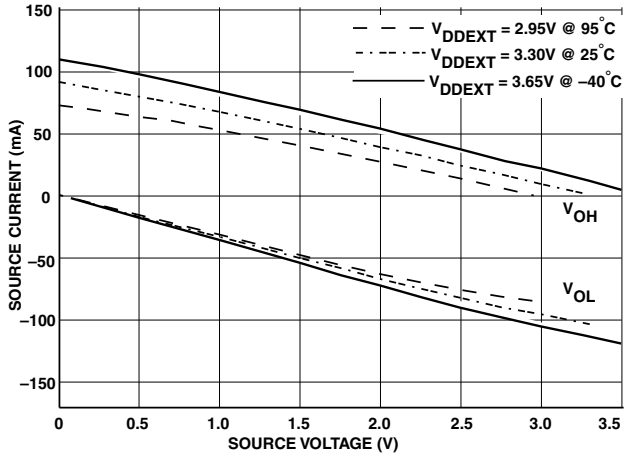


Figure 32. Drive Current D (High V_{DDEXT})

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry (P_{INT}) and one due to the switching of external output drivers (P_{EXT}). Table 32 shows the power dissipation for internal circuitry (V_{DDINT}). Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

Table 32. Internal Power Dissipation[1]

Parameter	Test Conditions[2]				Unit
	f_{CCLK} = 50 MHz V_{DDINT} = 0.8 V	f_{CCLK} = 400 MHz V_{DDINT} = 1.2 V	f_{CCLK} = 500 MHz V_{DDINT} = 1.2 V	f_{CCLK} = 600 MHz V_{DDINT} = 1.2 V	
I_{DDTYP}[3]	26	160	190	220	mA
$I_{DDSLEEP}$[4]	16	37	37	37	mA
$I_{DDDEEPSLEEP}$[4]	14	31	31	31	mA
$I_{DDHIBERNATE}$[5]	50				µA
I_{DDRTC}[6]	30				µA

[1] See EE-229: Estimating Power for ADSP-BF533 Blackfin Processors.
[2] I_{DD} data is specified for typical process parameters. All data at 25°C.
[3] Processor executing 75% dual Mac, 25% ADD with moderate data bus activity.
[4] See the *ADSP-BF53x Blackfin Processor Hardware Reference Manual* for definitions of Sleep and Deep Sleep operating modes.
[5] Measured at V_{DDEXT} = 3.65V with voltage regulator off (V_{DDINT} = 0V).
[6] Measured at V_{DDRTC} = 3.3V at 25°C.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Number of output pins (O) that switch during each cycle
- Maximum frequency (f) at which they can switch
- Their load capacitance (C)
- Their voltage swing (V_{DDEXT})

The external component is calculated using:

$$P_{EXT} = O \times C \times V^2_{DD} \times f$$

The frequency f includes driving the load high and then back low. For example: DATA15–0 pins can drive high and low at a maximum rate of $1/(2 \times t_{SCLK})$ while in SDRAM burst mode.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DD} \times V_{DDINT})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note, as well, that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the Output Enable/Disable diagram (Figure 33). The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches 2.0 V (output high) or 1.0 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.0 V or 2.0 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 33. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF531/2/3 processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (for example, t_{DSDAT} for an SDRAM write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 34). Figure 36 through Figure 43 on Page 44 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

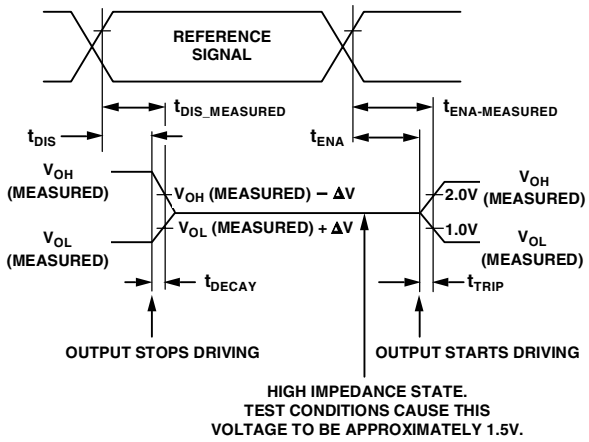


Figure 33. Output Enable/Disable

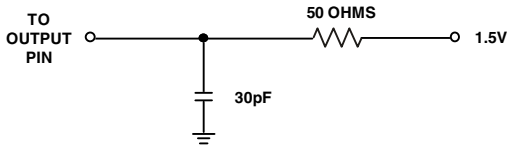


Figure 34. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

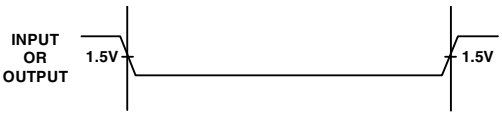


Figure 35. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

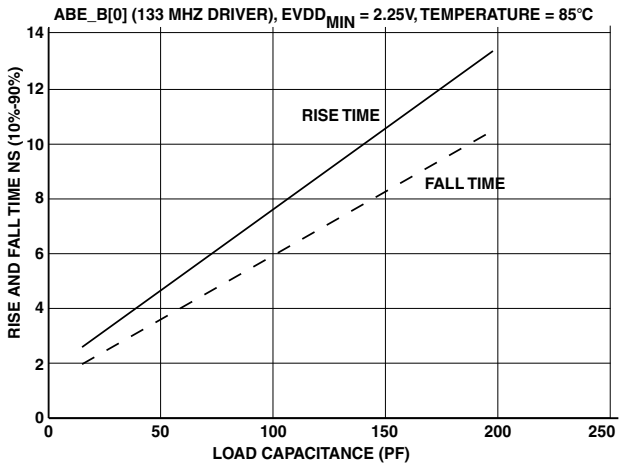


Figure 36. Typical Output Delay or Hold for Driver A at EVDD$_{MIN}$

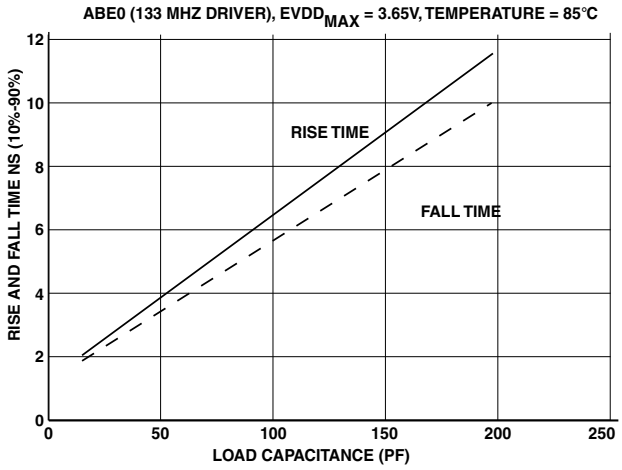


Figure 37. Typical Output Delay or Hold for Driver A at EVDD$_{MAX}$

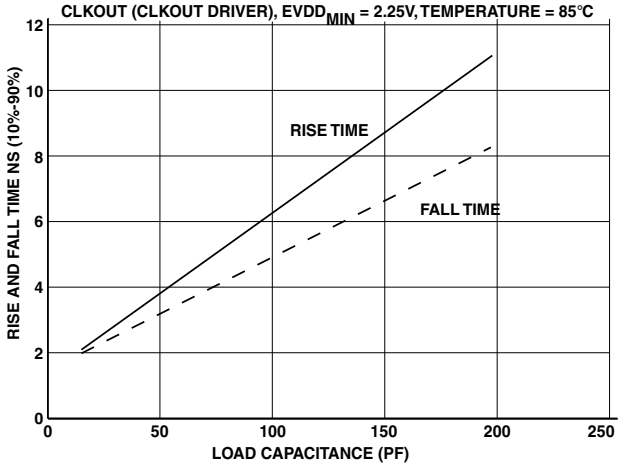


Figure 38. Typical Output Delay or Hold for Driver B at EVDD$_{MIN}$

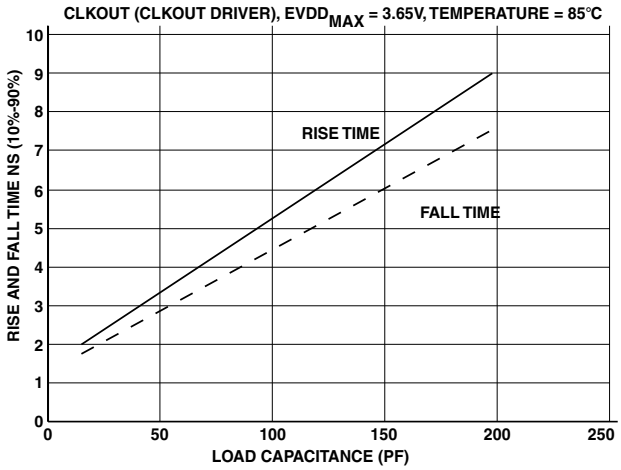


Figure 39. Typical Output Delay or Hold for Driver B at EVDD$_{MAX}$

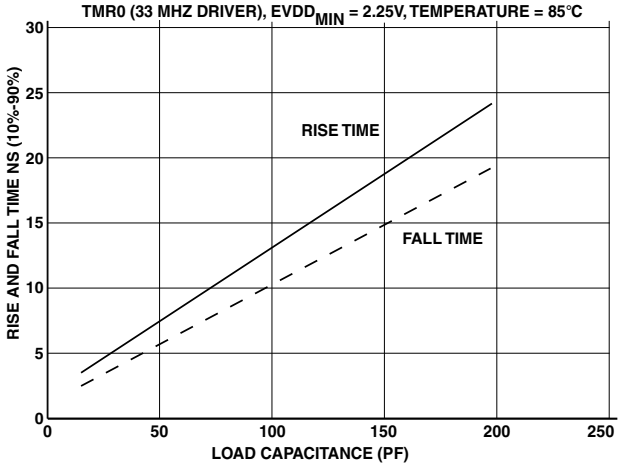


Figure 40. Typical Output Delay or Hold for Driver C at $EVDD_{MIN}$

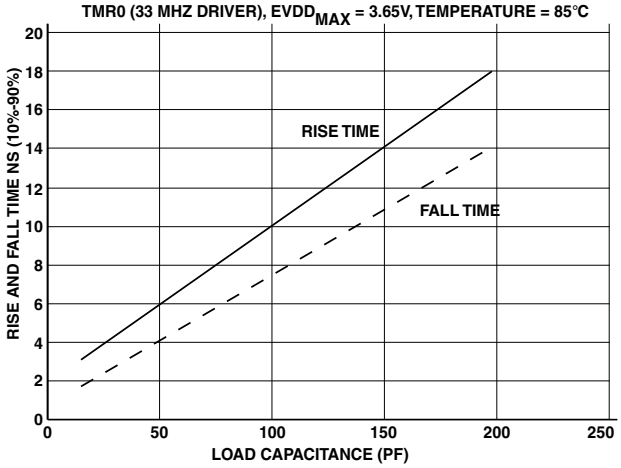


Figure 41. Typical Output Delay or Hold for Driver C at $EVDD_{MAX}$

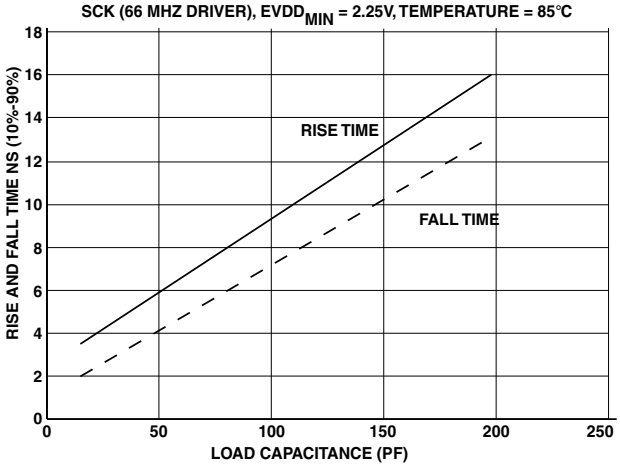


Figure 42. Typical Output Delay or Hold for Driver D at $EVDD_{MIN}$

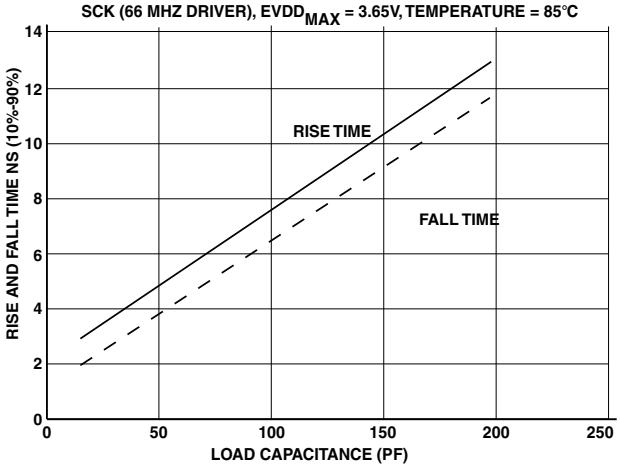


Figure 43. Typical Output Delay or Hold for Driver D at $EVDD_{MAX}$

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 33

P_D = Power dissipation (see Power Dissipation on Page 41 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

In Table 33, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 33 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. θ_{JB} represents the heat extracted from the periphery of the board. Ψ_{JT} represents the correlation between T_J and T_{CASE}. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

Table 33. Thermal Characteristics for BC-160 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	30.1	°C/W
θ_{JMA}	2 Linear m/s Airflow	28.8	°C/W
θ_{JB}	Not applicable	25.55	°C/W
θ_{JC}	Not applicable	8.75	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.13	°C/W

Table 34. Thermal Characteristics for ST-176-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.9	°C/W
θ_{JMA}	1 Linear m/s Airflow	33.0	°C/W
θ_{JMA}	2 Linear m/s Airflow	32.0	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.50	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.75	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.00	°C/W

Table 35. Thermal Characteristics for B-169 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	28.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	24.6	°C/W
θ_{JMA}	2 Linear m/s Airflow	23.8	°C/W
θ_{JB}	Not applicable	21.75	°C/W
θ_{JC}	Not applicable	12.7	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.78	°C/W

160-LEAD BGA PINOUT

Table 36 lists the BGA pinout by signal. Table 37 on Page 47
lists the BGA pinout by ball number.

Table 36. 160-Ball BGA Pin Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{\text{ABE0}}$	H13	DATA12	M5	GND	L6	SCK	D1
$\overline{\text{ABE1}}$	H12	DATA13	N5	GND	L8	SCKE	B13
ADDR1	J14	DATA14	P5	GND	L10	$\overline{\text{SMS}}$	C13
ADDR10	M13	DATA15	P4	GND	M4	$\overline{\text{SRAS}}$	D13
ADDR11	M14	DATA2	P9	GND	M10	$\overline{\text{SWE}}$	D12
ADDR12	N14	DATA3	M8	GND	P14	TCK	P2
ADDR13	N13	DATA4	N8	MISO	E2	TDI	M3
ADDR14	N12	DATA5	P8	MOSI	D3	TDO	N3
ADDR15	M11	DATA6	M7	NMI	B10	TFS0	H3
ADDR16	N11	DATA7	N7	PF0	D2	TFS1	E1
ADDR17	P13	DATA8	P7	PF1	C1	TMR0	L2
ADDR18	P12	DATA9	M6	PF10	A4	TMR1	M1
ADDR19	P11	DR0PRI	K1	PF11	A5	TMR2	K2
ADDR2	K14	DR0SEC	J2	PF12	B5	TMS	N2
ADDR3	L14	DR1PRI	G3	PF13	B6	$\overline{\text{TRST}}$	N1
ADDR4	J13	DR1SEC	F3	PF14	A6	TSCLK0	J1
ADDR5	K13	DT0PRI	H1	PF15	C6	TSCLK1	F1
ADDR6	L13	DT0SEC	H2	PF2	C2	TX	K3
ADDR7	K12	DT1PRI	F2	PF3	C3	VDDEXT	A1
ADDR8	L12	DT1SEC	E3	PF4	B1	VDDEXT	C7
ADDR9	M12	$\overline{\text{EMU}}$	M2	PF5	B2	VDDEXT	C12
$\overline{\text{AMS0}}$	E14	GND	A10	PF6	B3	VDDEXT	D5
$\overline{\text{AMS1}}$	F14	GND	A14	PF7	B4	VDDEXT	D9
$\overline{\text{AMS2}}$	F13	GND	B11	PF8	A2	VDDEXT	F12
$\overline{\text{AMS3}}$	G12	GND	C4	PF9	A3	VDDEXT	G4
$\overline{\text{AOE}}$	G13	GND	C5	PPI0	C8	VDDEXT	J4
ARDY	E13	GND	C11	PPI1	B8	VDDEXT	J12
$\overline{\text{ARE}}$	G14	GND	D4	PPI2	A7	VDDEXT	L7
$\overline{\text{AWE}}$	H14	GND	D7	PPI3	B7	VDDEXT	L11
$\overline{\text{BG}}$	P10	GND	D8	PPI_CLK	C9	VDDEXT	P1
$\overline{\text{BGH}}$	N10	GND	D10	$\overline{\text{RESET}}$	C10	VDDINT	D6
BMODE0	N4	GND	D11	RFS0	J3	VDDINT	E4
BMODE1	P3	GND	F4	RFS1	G2	VDDINT	E11
$\overline{\text{BR}}$	D14	GND	F11	RSCLK0	L1	VDDINT	J11
CLKIN	A12	GND	G11	RSCLK1	G1	VDDINT	L4
CLKOUT	B14	GND	H4	RTXI	A9	VDDINT	L9
DATA0	M9	GND	H11	RTXO	A8	VDDRTC	B9
DATA1	N9	GND	K4	RX	L3	VROUT0	A13
DATA10	N6	GND	K11	SA10	E12	VROUT1	B12
DATA11	P6	GND	L5	$\overline{\text{SCAS}}$	C14	XTAL	A11

Table 37 lists the BGA pinout by ball number. Table 36 on Page 46 lists the BGA pinout by signal.

Table 37. 160-Ball BGA Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	VDDEXT	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	VDDEXT	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	VDDINT	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	VDDEXT	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	VDDEXT	M14	ADDR11
A13	VROUT0	D11	GND	J11	VDDINT	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	VDDEXT	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	VDDINT	K4	GND	N8	DATA4
B7	PPI3	E11	VDDINT	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	VDDRTC	E13	ARDY	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT1	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	VDDEXT
B14	CLKOUT	F4	GND	L4	VDDINT	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	VDDEXT	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	VDDEXT	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	VDDINT	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	VDDEXT	G3	DR1PRI	L11	VDDEXT	P9	DATA2
C8	PPI0	G4	VDDEXT	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	VDDEXT	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

Figure 44 lists the top view of the BGA ball configuration.
Figure 45 lists the bottom view of the BGA ball configuration.

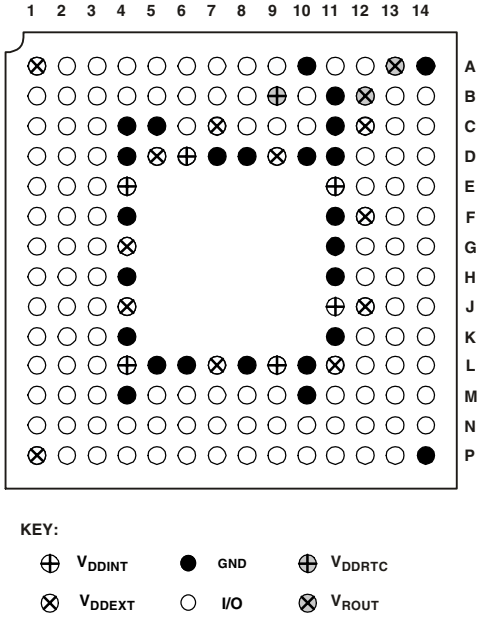


Figure 44. 160-Ball BGA Ball Configuration (Top View)

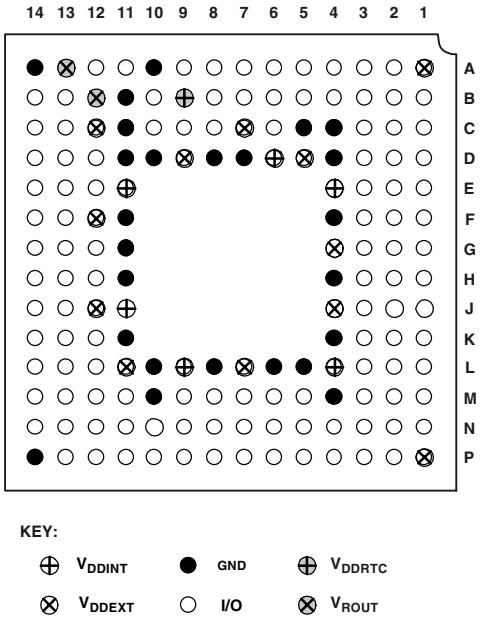


Figure 45. 160-Ball BGA Ball Configuration (Bottom View)

169-BALL PBGA PINOUT

Table 38 lists the PBGA pinout by signal. Table 39 on Page 52 lists the PBGA pinout by ball number.

Table 38. 169-Ball PBGA Pin Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
ABE [0]	H16	DATA [13]	T7	GND	G11	PF [8]	B4	VDD	K12
ABE [1]	H17	DATA [14]	U6	GND	H7	PF [9]	A4	VDD	L12
ADDR [1]	J16	DATA [15]	T6	GND	H8	PPI [0]	B9	VDD	M10
ADDR [10]	N16	DATA [2]	U13	GND	H9	PPI [1]	A9	VDD	M11
ADDR [11]	P17	DATA [3]	T11	GND	H10	PPI [2]	B8	VDD	M12
ADDR [12]	P16	DATA [4]	U12	GND	H11	PPI [3]	A8	VROUT	B12
ADDR [13]	R17	DATA [5]	U11	GND	J7	PPI_CLK	B10	VROUT	B13
ADDR [14]	R16	DATA [6]	T10	GND	J8	RESET	A12	XTAL	A13
ADDR [15]	T17	DATA [7]	U10	GND	J9	RFS0	N1		
ADDR [16]	U15	DATA [8]	T9	GND	J10	RFS1	J1		
ADDR [17]	T15	DATA [9]	U9	GND	J11	RSCLK0	N2		
ADDR [18]	U16	DR0PRI	M2	GND	K7	RSCLK1	J2		
ADDR [19]	T14	DR0SEC	M1	GND	K8	RTCVDD	F10		
ADDR [2]	J17	DR1PRI	H1	GND	K9	RTXI	A10		
ADDR [3]	K16	DR1SEC	H2	GND	K10	RTXO	A11		
ADDR [4]	K17	DT0PRI	K2	GND	K11	RX	T1		
ADDR [5]	L16	DT0SEC	K1	GND	L7	SA10	B15		
ADDR [6]	L17	DT1PRI	F1	GND	L8	SCAS	A16		
ADDR [7]	M16	DT1SEC	F2	GND	L9	SCK	D1		
ADDR [8]	M17	EMU	U1	GND	L10	SCKE	B14		
ADDR [9]	N17	EVDD	B2	GND	L11	SMS	A17		
AMS [0]	D17	EVDD	F6	GND	M9	SRAS	A15		
AMS [1]	E16	EVDD	F7	GND	T16	SWE	B17		
AMS [2]	E17	EVDD	F8	MISO	E2	TCK	U4		
AMS [3]	F16	EVDD	F9	MOSI	E1	TDI	U3		
AOE	F17	EVDD	G6	NMI	B11	TDO	T4		
ARDY	C16	EVDD	H6	PF [0]	D2	TFS0	L1		
ARE	G16	EVDD	J6	PF [1]	C1	TFS1	G2		
AWE	G17	EVDD	K6	PF [10]	B5	TMR0	R1		
BG	T13	EVDD	L6	PF [11]	A5	TMR1	P2		
BGH	U17	EVDD	M6	PF [12]	A6	TMR2	P1		
BMODE [0]	U5	EVDD	M7	PF [13]	B6	TMS	T3		
BMODE [1]	T5	EVDD	M8	PF [14]	A7	TRST	U2		
BR	C17	EVDD	T2	PF [15]	B7	TSCLK0	L2		
CLKIN	A14	GND	B16	PF [2]	B1	TSCLK1	G1		
CLKOUT	D16	GND	F11	PF [3]	C2	TX	R2		
DATA [0]	U14	GND	G7	PF [4]	A1	VDD	F12		
DATA [1]	T12	GND	G8	PF [5]	A2	VDD	G12		
DATA [10]	T8	GND	G9	PF [6]	B3	VDD	H12		
DATA [11]	U8	GND	G10	PF [7]	A3	VDD	J12		

Table 39 lists the PBGA pinout by ball number. Table 38 on Page 51 lists the PBGA pinout by signal.

Table 39. 169-Ball PBGA Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	PF [4]	D16	CLKOUT	J2	RSCLK1	M12	VDD	U8	DATA [11]
A2	PF [5]	D17	AMS [0]	J6	EVDD	M16	ADDR [7]	U9	DATA [9]
A3	PF [7]	E1	MOSI	J7	GND	M17	ADDR [8]	U10	DATA [7]
A4	PF [9]	E2	MISO	J8	GND	N1	RFS0	U11	DATA [5]
A5	PF [11]	E16	AMS [1]	J9	GND	N2	RSCLK0	U12	DATA [4]
A6	PF [12]	E17	AMS [2]	J10	GND	N16	ADDR [10]	U13	DATA [2]
A7	PF [14]	F1	DT1PRI	J11	GND	N17	ADDR [9]	U14	DATA [0]
A8	PPI [3]	F2	DT1SEC	J12	VDD	P1	TMR2	U15	ADDR [16]
A9	PPI [1]	F6	EVDD	J16	ADDR [1]	P2	TMR1	U16	ADDR [18]
A10	RTXI	F7	EVDD	J17	ADDR [2]	P16	ADDR [12]	U17	BGH
A11	RTXO	F8	EVDD	K1	DT0SEC	P17	ADDR [11]		
A12	RESET	F9	EVDD	K2	DT0PRI	R1	TMR0		
A13	XTAL	F10	RTCVDD	K6	EVDD	R2	TX		
A14	CLKIN	F11	GND	K7	GND	R16	ADDR [14]		
A15	SRAS	F12	VDD	K8	GND	R17	ADDR [13]		
A16	SCAS	F16	AMS [3]	K9	GND	T1	RX		
A17	SMS	F17	AOE	K10	GND	T2	EVDD		
B1	PF [2]	G1	TSCLK1	K11	GND	T3	TMS		
B2	EVDD	G2	TFS1	K12	VDD	T4	TDO		
B3	PF [6]	G6	EVDD	K16	ADDR [3]	T5	BMODE [1]		
B4	PF [8]	G7	GND	K17	ADDR [4]	T6	DATA [15]		
B5	PF [10]	G8	GND	L1	TFS0	T7	DATA [13]		
B6	PF [13]	G9	GND	L2	TSCLK0	T8	DATA [10]		
B7	PF [15]	G10	GND	L6	EVDD	T9	DATA [8]		
B8	PPI [2]	G11	GND	L7	GND	T10	DATA [6]		
B9	PPI [0]	G12	VDD	L8	GND	T11	DATA [3]		
B10	PPI_CLK	G16	ARE	L9	GND	T12	DATA [1]		
B11	NMI	G17	AWE	L10	GND	T13	BG		
B12	VROUT	H1	DR1PRI	L11	GND	T14	ADDR [19]		
B13	VROUT	H2	DR1SEC	L12	VDD	T15	ADDR [17]		
B14	SCKE	H6	EVDD	L16	ADDR [5]	T16	GND		
B15	SA10	H7	GND	L17	ADDR [6]	T17	ADDR [15]		
B16	GND	H8	GND	M1	DR0SEC	U1	EMU		
B17	SWE	H9	GND	M2	DR0PRI	U2	TRST		
C1	PF [1]	H10	GND	M6	EVDD	U3	TDI		
C2	PF [3]	H11	GND	M7	EVDD	U4	TCK		
C16	ARDY	H12	VDD	M8	EVDD	U5	BMODE [0]		
C17	BR	H16	ABE [0]	M9	GND	U6	DATA [14]		
D1	SCK	H17	ABE [1]	M10	VDD	U7	DATA [12]		
D2	PF [0]	J1	RFS1	M11	VDD	U8	DATA [11]		

176-LEAD LQFP PINOUT

Table 40 lists the LQFP pinout by signal. Table 41 on Page 52 lists the LQFP pinout by lead number.

Table 40. 176-Lead LQFP Pin Assignment (Alphabetically by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
$\overline{\text{ABE0}}$	151	DATA11	102	GND	88	PPI_CLK	21	VDDEXT	71
$\overline{\text{ABE1}}$	150	DATA12	101	GND	89	PPI0	22	VDDEXT	93
ADDR1	149	DATA13	100	GND	90	PPI1	23	VDDEXT	107
ADDR10	137	DATA14	99	GND	91	PPI2	24	VDDEXT	118
ADDR11	136	DATA15	98	GND	92	PPI3	26	VDDEXT	134
ADDR12	135	DATA2	114	GND	97	$\overline{\text{RESET}}$	13	VDDEXT	145
ADDR13	127	DATA3	113	GND	106	RFS0	75	VDDEXT	156
ADDR14	126	DATA4	112	GND	117	RFS1	64	VDDEXT	171
ADDR15	125	DATA5	110	GND	128	RSCLK0	76	VDDINT	25
ADDR16	124	DATA6	109	GND	129	RSCLK1	65	VDDINT	52
ADDR17	123	DATA7	108	GND	130	RTXI	17	VDDINT	66
ADDR18	122	DATA8	105	GND	131	RTXO	16	VDDINT	80
ADDR19	121	DATA9	104	GND	132	RX	82	VDDINT	111
ADDR2	148	DR0PRI	74	GND	133	SA10	164	VDDINT	143
ADDR3	147	DR0SEC	73	GND	144	$\overline{\text{SCAS}}$	166	VDDINT	157
ADDR4	146	DR1PRI	63	GND	155	SCK	53	VDDINT	168
ADDR5	142	DR1SEC	62	GND	170	SCKE	173	VDDRTC	18
ADDR6	141	DT0PRI	68	GND	174	$\overline{\text{SMS}}$	172	VROUT1	5
ADDR7	140	DT0SEC	67	GND	175	$\overline{\text{SRAS}}$	167	VROUT2	4
ADDR8	139	DT1PRI	59	GND	176	$\overline{\text{SWE}}$	165	XTAL	11
ADDR9	138	DT1SEC	58	MISO	54	TCK	94		
$\overline{\text{AMS0}}$	161	$\overline{\text{EMU}}$	83	MOSI	55	TDI	86		
$\overline{\text{AMS1}}$	160	GND	1	NMI	14	TDO	87		
$\overline{\text{AMS2}}$	159	GND	2	PF0	51	TFS0	69		
$\overline{\text{AMS3}}$	158	GND	3	PF1	50	TFS1	60		
$\overline{\text{AOE}}$	154	GND	7	PF10	34	TMR0	79		
ARDY	162	GND	8	PF11	33	TMR1	78		
$\overline{\text{ARE}}$	153	GND	9	PF12	32	TMR2	77		
$\overline{\text{AWE}}$	152	GND	15	PF13	29	TMS	85		
$\overline{\text{BG}}$	119	GND	19	PF14	28	$\overline{\text{TRST}}$	84		
$\overline{\text{BGH}}$	120	GND	30	PF15	27	TSCLK0	72		
BMODE0	96	GND	39	PF2	49	TSCLK1	61		
BMODE1	95	GND	40	PF3	48	TX	81		
$\overline{\text{BR}}$	163	GND	41	PF4	47	VDDEXT	6		
CLKIN	10	GND	42	PF5	46	VDDEXT	12		
CLKOUT	169	GND	43	PF6	38	VDDEXT	20		
DATA0	116	GND	44	PF7	37	VDDEXT	31		
DATA1	115	GND	56	PF8	36	VDDEXT	45		
DATA10	103	GND	70	PF9	35	VDDEXT	57		

Table 41 lists the LQFP pinout by lead number. Table 40 on Page 51 lists the LQFP pinout by signal.

Table 41. 176-Lead LQFP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	41	GND	81	TX	121	ADDR19	161	$\overline{\text{AMS0}}$
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	$\overline{\text{EMU}}$	123	ADDR17	163	$\overline{\text{BR}}$
4	VROUT2	44	GND	84	$\overline{\text{TRST}}$	124	ADDR16	164	SA10
5	VROUT1	45	VDDEXT	85	TMS	125	ADDR15	165	$\overline{\text{SWE}}$
6	VDDEXT	46	PF5	86	TDI	126	ADDR14	166	$\overline{\text{SCAS}}$
7	GND	47	PF4	87	TDO	127	ADDR13	167	$\overline{\text{SRAS}}$
8	GND	48	PF3	88	GND	128	GND	168	VDDINT
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	VDDEXT
12	VDDEXT	52	VDDINT	92	GND	132	GND	172	$\overline{\text{SMS}}$
13	$\overline{\text{RESET}}$	53	SCK	93	VDDEXT	133	GND	173	SCKE
14	NMI	54	MISO	94	TCK	134	VDDEXT	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	VDDEXT	97	GND	137	ADDR10		
18	VDDRTC	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	VDDEXT	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	VDDINT		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	VDDINT	65	RSCLK1	105	DATA8	145	VDDEXT		
26	PPI3	66	VDDINT	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	VDDEXT	147	ADDR3		
28	PF14	68	DT0PRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	$\overline{\text{ABE1}}$		
31	VDDEXT	71	VDDEXT	111	VDDINT	151	$\overline{\text{ABE0}}$		
32	PF12	72	TSCLK0	112	DATA4	152	$\overline{\text{AWE}}$		
33	PF11	73	DR0SEC	113	DATA3	153	$\overline{\text{ARE}}$		
34	PF10	74	DR0PRI	114	DATA2	154	$\overline{\text{AOE}}$		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	VDDEXT		
37	PF7	77	TMR2	117	GND	157	VDDINT		
38	PF6	78	TMR1	118	VDDEXT	158	$\overline{\text{AMS3}}$		
39	GND	79	TMR0	119	$\overline{\text{BG}}$	159	$\overline{\text{AMS2}}$		
40	GND	80	VDDINT	120	$\overline{\text{BGH}}$	160	$\overline{\text{AMS1}}$		

OUTLINE DIMENSIONS

Dimensions in Figure 46—160-Ball Plastic Ball Grid Array, mini-BGA (BC-160), Figure 47—176-LEAD LQFP (ST-176-1) and Figure 48—169-Ball Plastic Ball Grid Array, mini-BGA (B-169) are shown in millimeters.

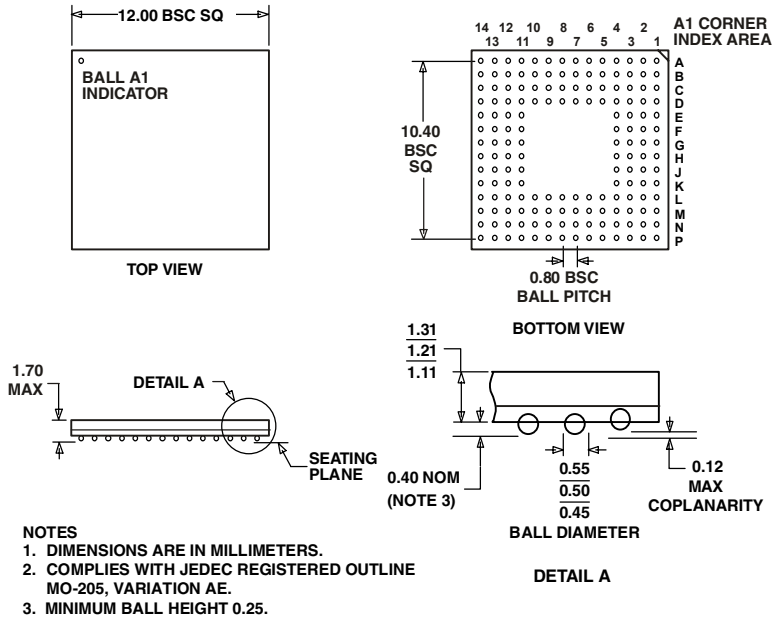


Figure 46. 160-Ball Plastic Ball Grid Array, mini-BGA (BC-160)

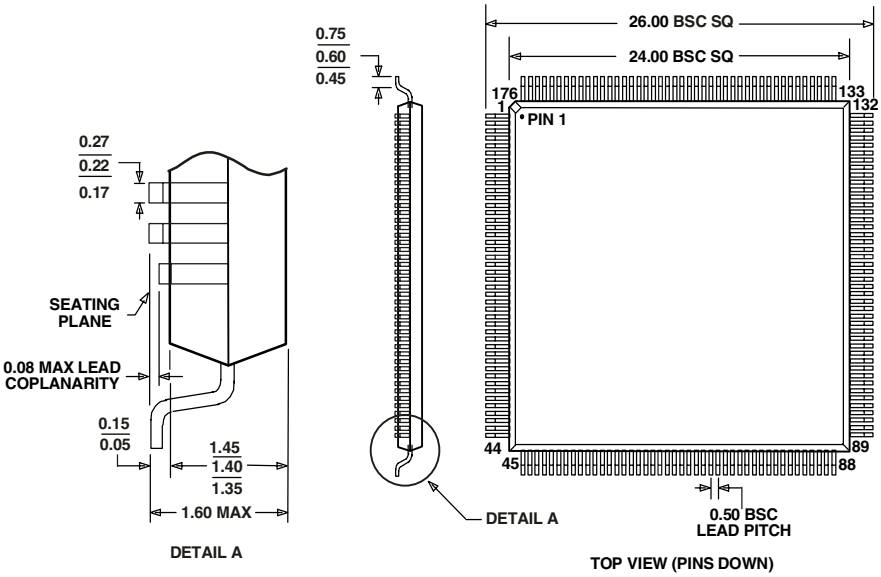
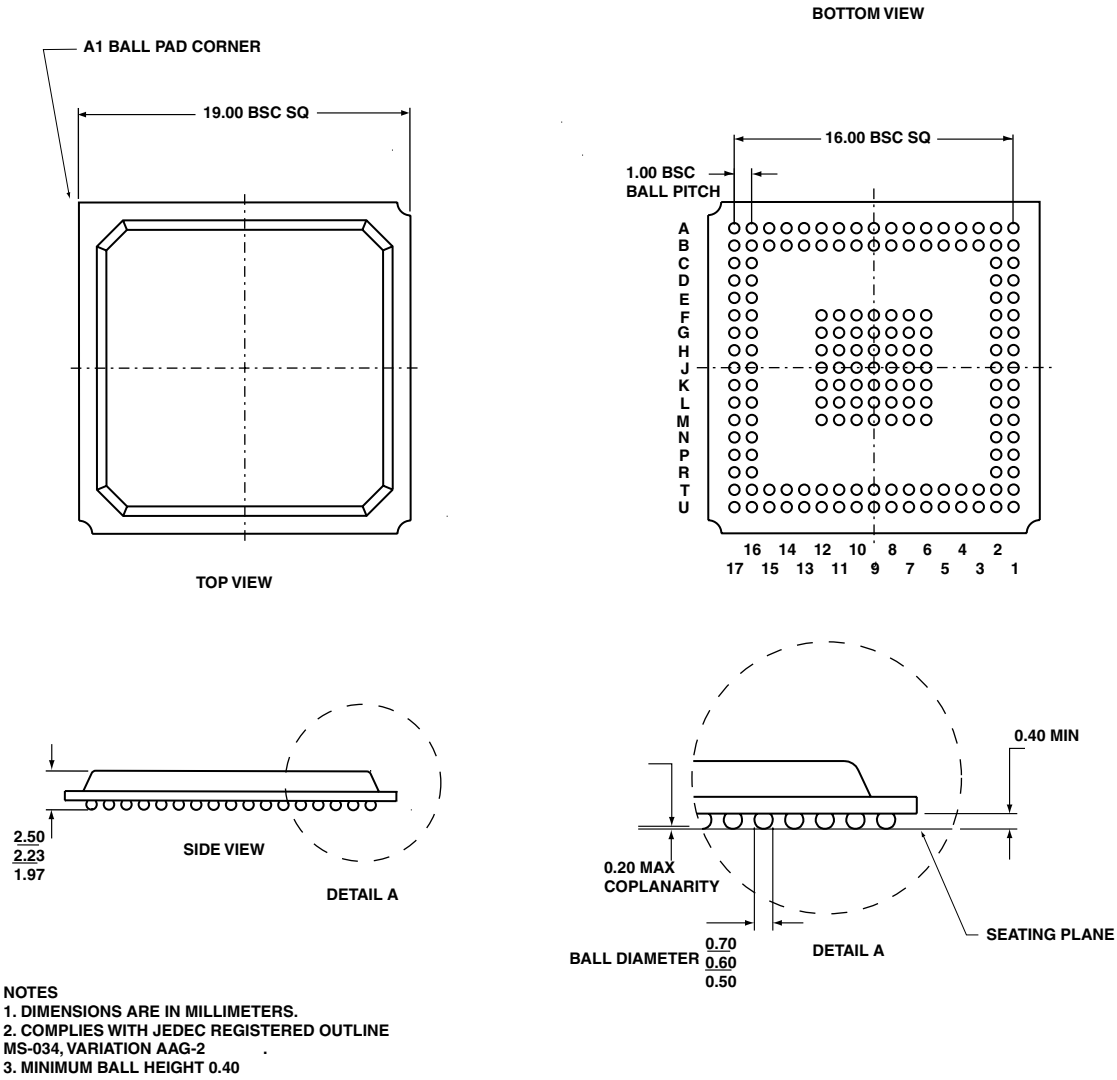


Figure 47. 176-LEAD LQFP (ST-176-1)



NOTES
1. DIMENSIONS ARE IN MILLIMETERS.
2. COMPLIES WITH JEDEC REGISTERED OUTLINE MS-034, VARIATION AAG-2 .
3. MINIMUM BALL HEIGHT 0.40

Figure 48. 169-Ball Plastic Ball Grid Array, mini-BGA (B-169)

ORDERING GUIDE

Part Number	Temperature Range (Ambient)	Package Description	Instruction Rate (Max)	Operating Voltage
ADSP-BF533SKBC600	0°C to 70°C	Chip Scale Package Ball Grid Array (mini-BGA) BC-160	600 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF533SBBC500	–40°C to 85°C	Chip Scale Package Ball Grid Array (mini-BGA) BC-160	500 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF533SBBZ500[1]	–40°C to 85°C	Plastic Ball Grid Array (PBGA) B-169	500 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF532SBBC400	–40°C to 85°C	Chip Scale Package Ball Grid Array (mini-BGA) BC-160	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF532SBST400	–40°C to 85°C	Quad Flatpack (LQFP) ST-176-1	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF532SBBZ400[1]	–40°C to 85°C	Plastic Ball Grid Array (PBGA) B-169	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF531SBBC400	–40°C to 85°C	Chip Scale Package Ball Grid Array (mini-BGA) BC-160	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF531SBST400	–40°C to 85°C	Quad Flatpack (LQFP) ST-176-1	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O
ADSP-BF531SBBZ400[1]	–40°C to 85°C	Plastic Ball Grid Array (PBGA) B-169	400 MHz	1.2 V internal, 2.5 V or 3.3 V I/O

[1] Z = Pb-free part.

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