

ANALOG EMI/EMC Compliant, ±15 kV ESD Protected, PS_232 Line Drivers/Deceivers

ADM202E/ADM1181A

FEATURES

Complies with 89/336/EEC EMC Directive ESD Protection to IEC1000-4-2 (801.2)

±8 kV: Contact Discharge ±15 kV: Air-Gap Discharge ±15 kV: Human Body Model

EFT Fast Transient Burst Immunity (IEC1000-4-4)

Low EMI Emissions (EN55022) 230 kbits/s Data Rate Guaranteed **TSSOP Package Option**

Upgrade for MAX202E, 232E, LT1181A

APPLICATIONS General Purpose RS-232 Data Link Portable Instruments **PDAs**

GENERAL DESCRIPTION

The ADM202E and ADM1181A are robust, high speed, 2channel RS232/V.28 interface devices that operate from a single +5 V power supply. Both products are suitable for operation in harsh electrical environments and are compliant with the EU directive on EMC (89/336/EEC). Both the level of electromagnetic emissions and immunity are in compliance. EM immunity includes ESD protection in excess of ±15 kV on all I/O lines, Fast Transient burst protection (1000-4-4) and Radiated Immunity (1000-4-3). EM emissions include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

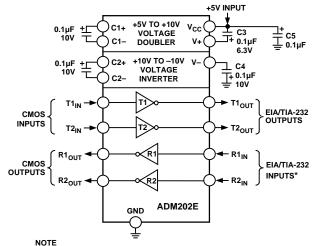
The ADM202E and ADM1181A conform to the EIA-232E and CCITT V.28 specifications and operate at data rates up to 230 kbps.

Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter permitting operation from a single +5 V supply.

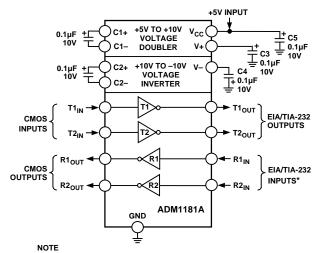
The ADM202E provides a robust pin-compatible upgrade for existing ADM202, ADM232L or MAX202E/MAX232E sockets. It is available in a 16-pin DIP, wide and narrow SO and also a space saving TSSOP package. The TSSOP package gives a 44% space saving over SOIC.

The ADM1181A provides a robust pin compatible upgrade for the LTC1181A, and it is available in 16-pin DIP and 16-lead SO packages.

FUNCTIONAL BLOCK DIAGRAMS



*INTERNAL $5 \mathrm{k}\Omega$ PULL-DOWN RESISTOR ON EACH RS-232 INPUT



*INTERNAL $5 \mathrm{k}\Omega$ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM202EAN	-40°C to +85°C	N-16
ADM202EARW	-40°C to +85°C	R-16W
ADM202EARN	-40°C to +85°C	R-16N
ADM202EARU	-40°C to +85°C	RU-16
ADM1181AAN	-40°C to +85°C	N-16
ADM1181AARW	-40°C to +85°C	R-16W

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$ADM202E/ADM1181A-SPECIFICATIONS~(V_{CC} = +5.0~V~\pm~10\%,~C1-C4 = 0.1~\mu F.~All~specifications~T_{MIN}~to~T_{MAX}~unless~otherwise~noted.)$

Parameter	Min	Тур	Max	Units	Test Conditions/Comments
DC CHARACTERISTICS Operating Voltage Range V _{CC} Power Supply Current	4.5	5.0 2.0 15	5.5 3.0 18	Volts mA mA	No Load $R_L = 3 \ k\Omega \ to \ GND$
LOGIC Input Logic Threshold Low, V _{INL} Input Logic Threshold High, V _{INH} CMOS Output Voltage Low, V _{OL} CMOS Output Voltage High, V _{OH} Input Leakage Current	2.4	0.01	0.8 0.4 ±10	V V V V μA	T_{IN} T_{IN} $I_{OUT} = 3.2 \text{ mA}$ $I_{OUT} = -1 \text{ mA}$ $T_{IN} = \text{GND to V}_{CC}$
RS-232 RECEIVER EIA-232 Input Voltage Range EIA-232 Input Threshold Low EIA-232 Input Threshold High EIA-232 Input Hysteresis EIA-232 Input Resistance	-30 0.4	0.8 1.1 0.7 5	+30 2.4 7	V V V kΩ	
RS-232 TRANSMITTER Output Voltage Swing Transmitter Output Resistance RS-232 Output Short Circuit Current	±5.0 300	±9.0 ±15	±60	Volts Ω mA	All Transmitter Outputs Loaded with 3 k Ω to Ground $V_{\rm CC}=0$ V, $V_{\rm OUT}=\pm2$ V
TIMING CHARACTERISTICS Maximum Data Rate Receiver Propagation Delay TPHL TPLH Transmitter Propagation Delay Transition Region Slew Rate	230	0.3 0.6 1.2 10	1 1 1.5 30	kbps µs µs µs µs V/µs	$R_L=3~k\Omega~to~7~k\Omega,~C_L=50~pF~to~2500~pF$ $R_L=3~k\Omega,~C_L=2500~pF$ $R_L=3~k\Omega,~C_L=2500~pF$ $Measured~from~+3~V~to~-3~V~or\\ -3~V~to~+3~V$
EM IMMUNITTY ESD Protection (I/O pins) EFT Protection (I/O pins) EMI Immunity		±15 ±15 ±8 kV ±2 10		kV kV kV kV V/m	Human Body Model IEC1000-4-2 Air Discharge IEC1000-4-2 Contact Discharge IEC1000-4-4 IEC1000-4-3

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
$(T_A = +25^{\circ}C \text{ unless otherwise noted})$
V_{CC} 0.3 V to +6 V
V+ (V $_{CC}$ – 0.3 V) to +14 V
V
Input Voltages
T_{IN} 0.3 V to (V+, +0.3 V)
$R_{IN} \ \dots \ \pm 30 \ V$
Output Voltages
T_{OUT} $\pm 15 \text{ V}$
R_{OUT} 0.3 V to $(V_{CC} + 0.3 \text{ V})$
Short Circuit Duration
T _{OUT} Continuous
Power Dissipation
Power Dissipation N-16
(Derate 6 mW/°C above +50°C)
θ_{JA} , Thermal Impedance

Power Dissipation R-16
(Derate 6 mW/°C above +50°C)
θ_{JA} , Thermal Impedance
Power Dissipation RU-16500 mW
(Derate 6 mW/°C above +50°C)
θ _{JA} , Thermal Impedance
Operating Temperature Range
Industrial (A Version)40°C to +85°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10 sec)+300°C
ESD Rating (MIL-STD-883B) (I/O Pins) ±15 kV
ESD Rating MIL-STD-883B (Except I/O) ±3 kV
ESD Rating (IEC1000-4-2 Air) (I/O Pins) ±15 kV
ESD Rating (IEC1000-4-2 Contact) (I/O Pins) ±8 kV
EFT Rating (IEC1000-4-4) (I/O Pins) ±2 kV
*This is a stress rating only and functional operation of the device at these or any

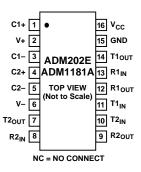
 $^{{}^*\}mathrm{This}$ is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

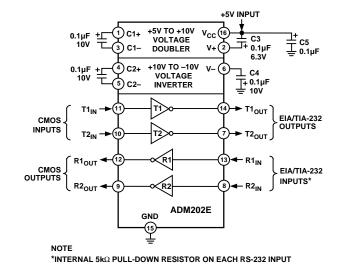
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PIN FUNCTION DESCRIPTION

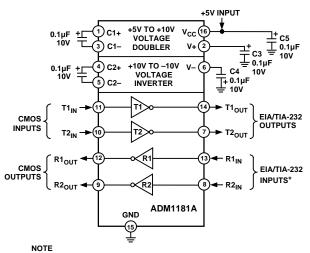
Mnemonic	Function
$\overline{V_{CC}}$	Power Supply Input: +5 V ± 10%.
V+	Internally Generated Positive Supply (+9 V nominal).
V-	Internally Generated Negative Supply (-9 V nominal).
GND	Ground Pin. Must Be Connected to 0 V.
C1+, C1-	External Capacitor 1 is connected between these pins. $0.1~\mu F$ capacitor is recommended but larger capacitors up to 47 μF may be used.
C2+, C2-	External Capacitor 2 is connected between these pins. 0.1 μF capacitor is recommended but larger capacitors up to 47 μF may be used.
$T_{\rm IN}$	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 signal levels (typically ±9 V).
$R_{\rm IN}$	Receiver Inputs. These inputs accept RS-232 signal levels. An Internal 5 k Ω pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are CMOS output logic levels.

PIN CONNECTIONS





ADM202E Typical Operating Circuit



*INTERNAL 5k Ω PULL-DOWN RESISTOR ON EACH RS-232 INPUT

ADM1181A Typical Operating Circuit

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GENERAL DESCRIPTION

The ADM202E/ADM1181E are ruggedized RS-232 line drivers/receivers. Step-up voltage converters coupled with level shifting transmitters and receivers allow RS-232 levels to be developed while operating from a single +5 V supply.

Features include low power consumption, high transmission rates and compatibility with the EU directive on Electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference including high levels of Electrostatic Discharge.

All inputs and outputs contain protection against Electrostatic Discharges up to ± 15 kV and Electrical Fast Transients up to ± 2 kV. This ensures compliance to IE1000-4-2 and IEC1000-4-4 requirements.

The devices are ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions.

CMOS technology is used to keep the power dissipation to an absolute minimum allowing maximum battery life in portable applications.

The ADM202E/ADM1181A is a modification, enhancement and improvement to the AD230-AD241 family and its derivatives. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of four main sections. These are:

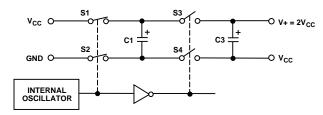
- 1. A charge pump voltage converter
- 2. 5 V logic to EIA-232 transmitters
- 3. EIA-232 to 5 V logic receivers.
- 4. Transient protection circuit on all I/O lines

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an 200 kHz oscillator and a switching matrix. The converter generates a $\pm\,10$ V supply from the input +5 V level. This is done in two stages using a switched capacitor technique as illustrated below. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate –10 V using C2 as the storage element.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be increased if desired. On the ADM202E, capacitor C3 is shown connected between V+

and $V_{\rm CC},$ while it is connected between V+ and GND on the ADM1181A. It is acceptable to use either configuration with both the ADM202E and ADM1181A. If desired, larger capacitors (up to 47 $\mu F)$ can be used for capacitors C1–C4. This facilitates direct substitution with older generation charge pump RS-232 transceivers.



NOTE: C3 CONNECTS BETWEEN V+ AND GND ON THE ADM1181A

Figure 1. Charge Pump Voltage Doubler

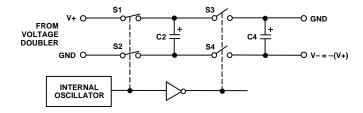


Figure 2. Charge Pump Voltage Inverter

Transmitter (Driver) Section

The drivers convert 5 V logic input levels into RS-232 output levels. With V_{CC} = +5 V and driving an RS-232 load, the output voltage swing is typically ± 9 V.

Receiver Section

The receivers are inverting level shifters which accept RS-232 input levels and translate them into 5 V logic output levels. The inputs have internal 5 k Ω pull-down resistors to ground and are also protected against overvoltages of up to ± 30 V. Unconnected inputs are pulled to 0 V by the internal 5 k Ω pull-down resistor. This, therefore, results in a Logic 1 output level for unconnected inputs or for inputs connected to GND.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

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HIGH BAUD RATE

The ADM202E/ADM1181A feature high slew rates permitting data transmission at rates well in excess of the EIA/RS-232-E specifications. RS-232 voltage levels are maintained at data rates up to 230 kb/s even under worst case loading conditions. This allows for high speed data links between two terminals or indeed it is suitable for the new generation $I_{\rm SDN}$ modem standards which requires data rates of 230 kbps. The slew rate is internally controlled to less than 30 V/µs in order to minimize EMI interference.

ESD/EFT TRANSIENT PROTECTION SCHEME.

The ADM202E/ADM1181A use protective clamping structures on all inputs and outputs which clamp the voltage to a safe level and dissipate the energy present in ESD (Electrostatic) and EFT (Electrical Fast Transients) discharges. A simplified schematic of the protection structure is shown in Figure 3. Each input and output contains two back-to-back high speed clamping diodes. During normal operation with maximum RS-232 signal levels, the diodes have no effect as one or the other is reverse biased depending on the polarity of the signal. If however the voltage exceeds about 50 V in either direction, reverse breakdown occurs and the voltage is clamped at this level. The diodes are large p-n junctions that are designed to handle the instantaneous current surge which can exceed several amperes.

The transmitter outputs and receiver inputs have a similar protection structure. The receiver inputs can also dissipate some of the energy through the internal 5 k Ω resistor to GND as well as through the protection diodes.

The protection structure achieves ESD protection up to $\pm 15~kV$ and EFT protection up to $\pm 2~kV$ on all RS-232 I/O lines. The methods used to test the protection scheme are discussed later.

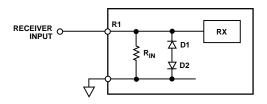


Figure 3a. Receiver Input Protection Scheme

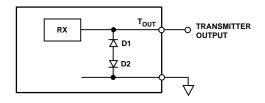


Figure 3b. Transmitter Output Protection Scheme

Typical Performance Curves

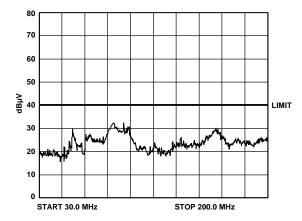


Figure 4. EMC Radiated Emissions

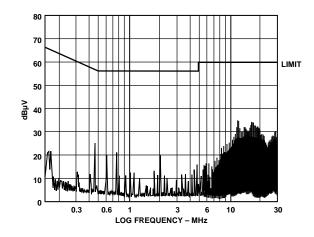


Figure 5. EMC Conducted Emissions

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Typical Performance Curves

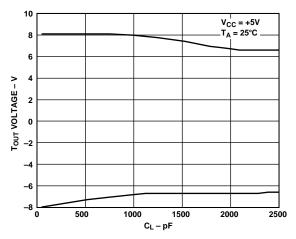


Figure 6. Transmitter Output Voltage High/Low vs. Load Capacitance @ 230 kbps

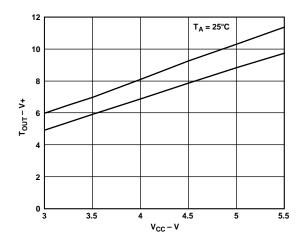


Figure 7. Transmitter Output Voltage High vs. V_{CC}

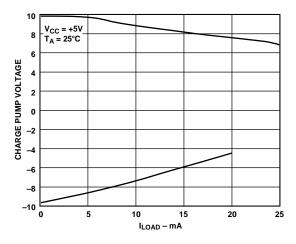


Figure 8. Charge Pump V+, V- vs. Current

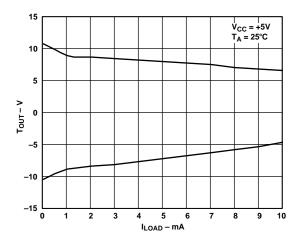


Figure 9. Transmitter Output Voltage Low/High vs. Load Current

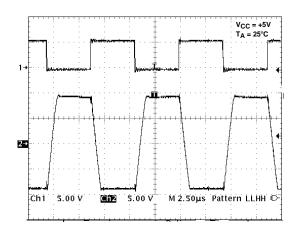


Figure 10. 230 kbps Data Transmission

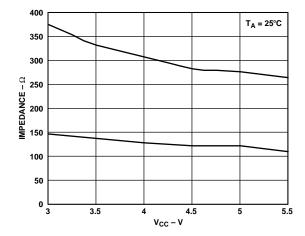


Figure 11. Charge Pump Impedance vs. V_{CC}

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ESD TESTING (IEC1000-4-2)

IEC1000-4-2 (previously 801-2) specifies compliance testing using two coupling methods, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved towards the unit under test developing an arc across the air gap, hence the term air-gap discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method while less realistic is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable can result in a static discharge which can damage or completely destroy the interface product connected to the I/O port. Traditional ESD test methods such as the MIL-STD-883B method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the traditional test and the IEC test:

- a. The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.
- b. The current rise time is significantly faster in the IEC test.
- c. The IEC test is carried out while power is applied to the device.

It is possible that the ESD discharge could induce latch-up in the device under test. This test therefore is more representative of a real-world I/O discharge where the equipment is operating normally with power applied. For maximum peace of mind, however, both tests should be performed therefore ensuring maximum protection both during handling and later during field service.

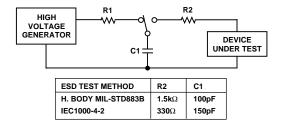


Figure 12. ESD Test Standards

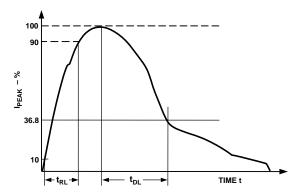


Figure 13. Human Body Model ESD Current Waveform

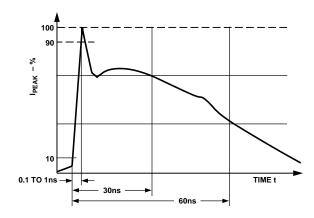


Figure 14. IEC1000-4-2 ESD Current Waveform

The ADM202E/ADM1181E products are tested using both the above mentioned test methods. All pins are tested with respect to all other pins as per the MIL-STD-883B specification. In addition all I/O pins are tested as per the IEC test specification. The products were tested under the following conditions:

- a. Power-On
- b. Power-Off

There are four levels of compliance defined by IEC1000-4-2. The ADM202E/ADM1181A products meet the most stringent compliance level for both contact and for air-gap discharge. This means that the products are able to withstand contact discharges in excess of 8 kV and air-gap discharges in excess of 15 kV.

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Table I. IEC1000-4-2 Compliance Levels

Level	Contact Discharge	Air Discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

Table II. ADM202E/ADM1181A ESD Test Results

ESD Test Method	I/O Pins	Other Pins
MIL-STD-883B IEC1000-4-2	±15 kV	±3 kV
Contact	±8 kV	
Air	±15 kV	

FAST TRANSIENT BURST TESTING (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast-transient/burst (EFT) immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when for example a power relay disconnects an inductive load. A spark is generated due to the well known back EMF effect. In fact the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line therefore consists of a bust of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient burst test defined in IEC1000-4-4 simulates this arcing and its waveform is illustrated in Figure 11. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

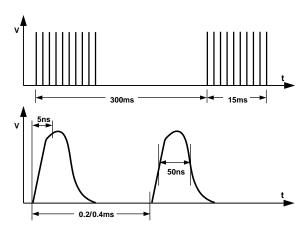


Figure 15. IEC1000-4-4 Fast Transient Waveform

A simplified circuit diagram of the actual EFT generator is illustrated in Figure 16.

The transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 m long and it completely surrounds the cable providing maximum coupling capacitance (50 pF to 200 pF typ) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns) as specified by the standard result in very effective coupling. This test is very severe since high voltages are coupled onto the signal lines. The repetitive transients can often cause problems where single pulses don't. Destructive latchup may be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and are transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst case transient current on an I/O line can be as high as 40 A.

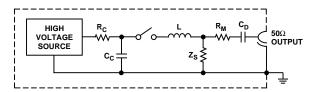


Figure 16. IEC1000-4-4 Fast Transient Generator

Test results are classified according to the following:

- 1. Normal performance within specification limits.
- 2. Temporary degradation or loss of performance that is self-recoverable.
- 3. Temporary degradation or loss of function or performance that requires operator intervention or system reset.
- 4. Degradation or loss of function that is not recoverable due to damage.

The ADM202E/ADM1181A have been tested under worst case conditions using unshielded cables and meet Classification 2. Data transmission during the transient condition is corrupted, but it may be resumed immediately following the EFT event without user intervention.

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IEC1000-4-3 RADIATED IMMUNITY

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers or any other device which generates continuous wave radiated electromagnetic energy. Its scope has since been broadened to include spurious EM energy which can be radiated from fluorescent lights, thyristor drives, inductive loads, etc.

Testing for immunity involves irradiating the device with an EM field. There are various methods of achieving this including use of anechoic chamber, stripline cell, TEM cell, GTEM cell. A stripline cell consists of two parallel plates with an electric field developed between them. The device under test is placed within the cell and exposed to the electric field. There are three severity levels having field strengths ranging from 1 V to 10 V/m. Results are classified in a similar fashion to those for IEC1000-4-2.

- 1. Normal Operation.
- Temporary Degradation or loss of function that is selfrecoverable when the interfering signal is removed.
- 3. Temporary degradation or loss of function that requires operator intervention or system reset when the interfering signal is removed.
- Degradation or loss of function that is not recoverable due to damage.

The ADM202E/ADM1181A products easily meet Classification 1 at the most stringent (Level 3) requirement. In fact field strengths up to 30~V/m showed no performance degradation, and error-free data transmission continued even during irradiation.

Table III. Test Severity Levels (IEC1000-4-3)

Level	Field Strength V/m
1	1
2	3
3	10

EMISSIONS/INTERFERENCE

EN55 022, CISPR22 defines the permitted limits of radiated and conducted interference from Information Technology (IT) equipment. The objective of the standard is to minimize the level of emissions both conducted and radiated.

For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz and radiated emissions are assumed to predominate above 30 MHz.

CONDUCTED EMISSIONS

This is a measure of noise that gets conducted onto the mains power supply. Switching transients from the charge pump that are 20 V in magnitude and contain significant energy can lead to conducted emissions. Other sources of conducted emissions can be due to overlap in switch on-times in the charge pump voltage converter. In the voltage doubler shown below, if S2 has not fully turned off before S4 turns on, this results in a transient

current glitch between $V_{\rm CC}$ and GND which results in conducted emissions. It is, therefore, important that the switches in the charge pump guarantee break-before-make switching under all conditions so that instantaneous short circuit conditions do not occur.

The ADM202E has been designed to minimize the switching transients and ensure break-before-make switching thereby minimizing conducted emissions. This has resulted in the level of emissions being well below the limits required by the specification. No additional filtering/decoupling other than the recommended $0.1~\mu F$ capacitor is required.

Conducted emissions are measured by monitoring the mains line. The equipment used consists of a LISN (Line Impedance Stabilizing Network) that essentially presents a fixed impedance at RF, and a spectrum analyzer. The spectrum analyzer scans for emissions up to 30 MHz and a plot for the ADM202E is shown in Figure 19.

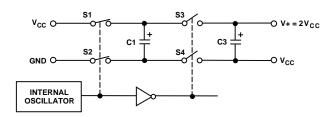


Figure 17. Charge Pump Voltage Doubler

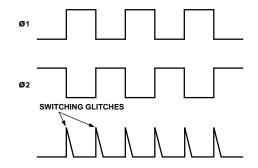


Figure 18. Switching Glitches

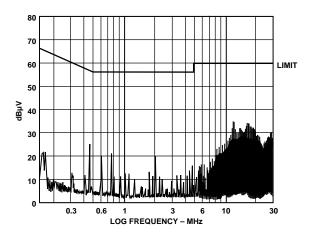


Figure 19. ADM202E Conducted Emissions Plot

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RADIATED EMISSIONS

Radiated emissions are measured at frequencies in excess of 30 MHz. RS-232 outputs designed for operation at high baud rates while driving cables can radiate high frequency EM energy. The reasons already discussed that cause conducted emissions can also be responsible for radiated emissions. Fast RS-232 output transitions can radiate interference, especially when lightly loaded and driving unshielded cables. Charge pump devices are also prone to radiating noise due to the high frequency oscillator and high voltages being switched by the charge pump. The move towards smaller capacitors in order to conserve board space has resulted in higher frequency oscillators being employed in the charge pump design. This has resulted in higher levels of emission, both conducted and radiated.

The RS-232 outputs on the ADM202E products feature a controlled slew rate in order to minimize the level of radiated emissions, yet are fast enough to support data rates up to 230 kBaud.

Figure 21 shows a plot of radiated emissions vs. frequency. This shows that the levels of emissions are well within specifications without the need for any additional shielding or filtering components. The ADM202E was operated at maximum baud rates and configured as in a typical RS-232 interface.

Testing for radiated emissions was carried out in a shielded anechonic chamber.

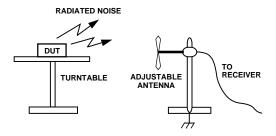


Figure 20. Radiated Emissions Test Setup

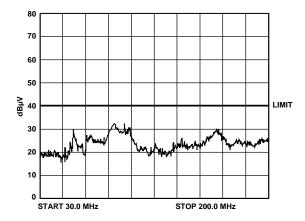


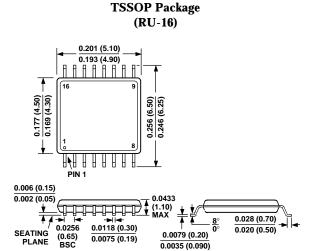
Figure 21. ADM202E Radiated Emissions Plot

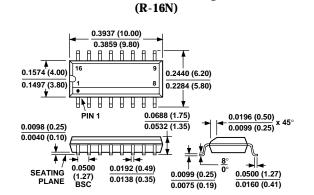
-10- REV. 0

OUTLINE DIMENSIONS

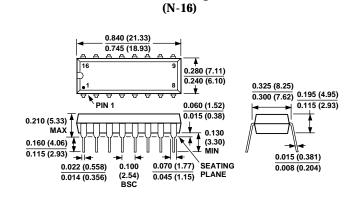
Dimensions shown in inches and (mm).

SOIC (Wide) Package (R-16W) 0.4133 (10.50) 0.3977 (10.00) 0.2992 (7.60) 0.2914 (7.40) 0.4193 (10.65) 0.3937 (10.00) 848 8 8 8 8 0.1043 (2.65) 0.0291 (0.74) 0.0098 (0.25) x 45° PIN 1 0.0118 (0.30) 0.0926 (2.35) 0.0040 (0.10) 0.0500 (1.27) 0.0192 (0.49) 0.0157 (0.40) 0.0192 (0.49) 0.0138 (0.35) SEATING 0.0125 (0.32) PLANE 0.0091 (0.23) BSC 0.0091 (0.23)





SOIC (Narrow) Package



DIP Package

REV. 0 -11-