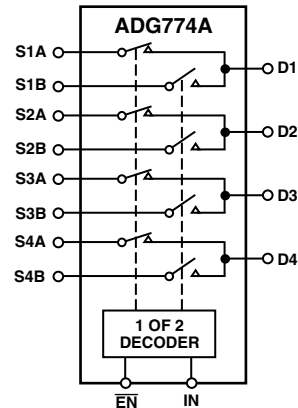


FEATURES

Bandwidth >400 MHz
Low Insertion Loss and On Resistance: 2.2 Ω Typical
On-Resistance Flatness 0.3 Ω Typical
Single 3 V/5 V Supply Operation
Very Low Distortion: <0.3%
Low Quiescent Supply Current (1 nA Typical)
Fast Switching Times
 t_{ON} 6 ns
 t_{OFF} 3 ns
TTL/CMOS Compatible

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG774A is a monolithic CMOS device comprising four 2:1 multiplexer/demultiplexers with high impedance outputs. The CMOS process provides low power dissipation yet gives high switching speed and low on resistance. The on-resistance variation is typically less than 0.5 Ω over the input signal range.

The bandwidth of the ADG774A is typically 400 MHz and this, coupled with low distortion (typically 0.3%), makes the part suitable for switching of high-speed data signals.

The on-resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion. CMOS construction ensures ultralow power dissipation.

The ADG774A operates from a single 3.3 V/5 V supply and is TTL logic compatible. The control logic for each switch is shown in the Truth Table.

These switches conduct equally well in both directions when ON. In the OFF condition, signal levels up to the supplies are blocked. The ADG774A switches exhibit break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Wide bandwidth data rates >400 MHz.
2. Ultralow Power Dissipation.
3. Low leakage over temperature.
4. Break-Before-Make Switching.
This prevents channel shorting when the switches are configured as a multiplexer.
5. Crosstalk is typically -70 dB @ 10 MHz.
6. Off isolation is typically -65 dB @ 10 MHz.

REV. 0

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ADG774A—SPECIFICATIONS

SINGLE SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 to 2.5	V	
On Resistance (R_{ON})	2.2		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
	3.5	4	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.15		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.3		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		0.6	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.001		nA typ	$V_D = 3\text{ V}$, $V_S = 1\text{ V}$; $V_D = 1\text{ V}$, $V_S = 3\text{ V}$; Test Circuit 2
	± 0.1	± 0.25	nA max	
Drain OFF Leakage I_D (OFF)	± 0.001		nA typ	$V_D = 3\text{ V}$, $V_S = 1\text{ V}$; $V_D = 1\text{ V}$, $V_S = 3\text{ V}$; Test Circuit 2
	± 0.1	± 0.25	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.001		nA typ	$V_D = V_S = 3\text{ V}$; $V_D = V_S = 1\text{ V}$; Test Circuit 3
	± 0.1	± 0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance		3	pF typ	
DYNAMIC CHARACTERISTICS ²				
t_{ON} , $t_{ON}(\overline{EN})$		6	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_S = 2\text{ V}$; Test Circuit 4
		12	ns max	
t_{OFF} , $t_{OFF}(\overline{EN})$		3	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_S = 2\text{ V}$; Test Circuit 4
		6	ns max	
Break-Before-Make Time Delay, t_D		3	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_{S1} = V_{S2} = 2\text{ V}$; Test Circuit 5
		1	ns min	
Off Isolation		-65	dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Test Circuit 7
Channel-to-Channel Crosstalk		-70	dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Test Circuit 8
Bandwidth -3 dB		400	MHz typ	Test Circuit 6, $R_L = 50\ \Omega$;
Distortion		0.3	% typ	$R_L = 100\ \Omega$
Charge Injection		6	pC typ	$C_L = 1\text{ nF}$; Test Circuit 9, $V_S = 0\text{ V}$
C_S (OFF)		5	pF typ	
C_D (OFF)		7.5	pF typ	
C_D , C_S (ON)		12	pF typ	
POWER REQUIREMENTS				
I_{DD}		1	μA max	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or V_{DD}
	0.001		μA typ	

NOTES

¹Temperature ranges are as follows: B Version, -40°C to $+85^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 to 1.5	V	
On Resistance (R_{ON})	4		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
	6	7	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.15		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		3	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.001		nA typ	$V_D = 2\text{ V}$, $V_S = 1\text{ V}$; $V_D = 1\text{ V}$, $V_S = 2\text{ V}$; Test Circuit 2
	± 0.1	± 0.25	nA max	
Drain OFF Leakage I_D (OFF)	± 0.001		nA typ	$V_D = 2\text{ V}$, $V_S = 1\text{ V}$; $V_D = 1\text{ V}$, $V_S = 2\text{ V}$; Test Circuit 2
	± 0.1	± 0.25	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.001		nA typ	$V_D = V_S = 2\text{ V}$; $V_D = V_S = 1\text{ V}$; Test Circuit 3
	± 0.1	± 0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance		3	pF typ	
DYNAMIC CHARACTERISTICS²				
t_{ON} , $t_{ON}(\overline{EN})$		7	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_S = 1.5\text{ V}$; Test Circuit 4
		14	ns max	
t_{OFF} , $t_{OFF}(\overline{EN})$		4	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_S = 1.5\text{ V}$; Test Circuit 4
		8	ns max	
Break-Before-Make Time Delay, t_D		3	ns typ	$C_L = 35\text{ pF}$, $R_L = 50\ \Omega$; $V_{S1} = V_{S2} = 1.5\text{ V}$; Test Circuit 5
		1	ns min	
Off Isolation		-65	dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$, Test Circuit 7
Channel-to-Channel Crosstalk		-70	dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$, Test Circuit 8
Bandwidth -3 dB		400	MHz typ	Test Circuit 6; $R_L = 50\ \Omega$
Distortion		1.5	% typ	$R_L = 100\ \Omega$
Charge Injection		4	pC typ	$C_L = 1\text{ nF}$; Test Circuit 9, $V_S = 0\text{ V}$
C_S (OFF)		5	pF typ	
C_D (OFF)		7.5	pF typ	
C_D , C_S (ON)		12	pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001	1	μA max μA typ	$V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or V_{DD}

NOTES

¹Temperature ranges are as follows: B Version, -40°C to $+85^\circ\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Table I. Truth Table

\overline{EN}	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

ADG774A

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

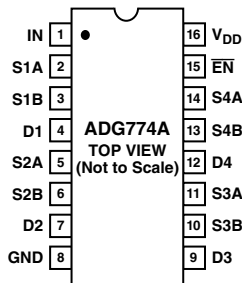
V _{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs ²	−0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QSOP Package, Power Dissipation	566 mW
θ _{JA} Thermal Impedance	149.97°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

² Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATION (QSOP)



TERMINOLOGY

V _{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
$\overline{\text{EN}}$	Logic Control Input.
R _{ON}	Ohmic resistance between D and S.
ΔR _{ON}	On Resistance match between any two channels i.e., R _{ON} max – R _{ON} min.
R _{FLAT(ON)}	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I _S (OFF)	Source Leakage Current with the switch “OFF.”
I _D (OFF)	Drain Leakage Current with the switch “OFF.”
I _D , I _S (ON)	Channel Leakage Current with the switch “ON.”
V _D (V _S)	Analog Voltage on Terminals D, S.
C _S (OFF)	“OFF” Switch Source Capacitance.
C _D (OFF)	“OFF” Switch Drain Capacitance.
C _D , C _S (ON)	“ON” Switch Capacitance.
t _{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t _{OFF}	Delay between applying the digital control input and the output switching Off.
t _D	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
Bandwidth	Frequency response of the switch in the ON state measured at 3 dB down.
Distortion	R _{FLAT(ON)} /R _L

ORDERING GUIDE

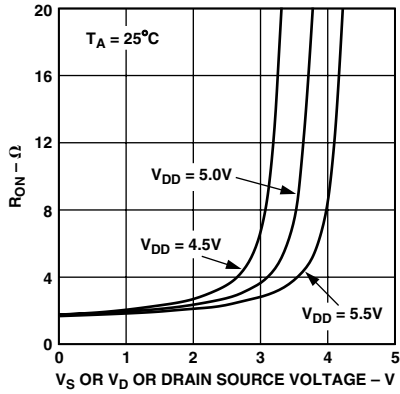
Model	Temperature Range	Package Descriptions	Package Options
ADG774ABRQ	−40°C to +85°C	RQ = 0.15" Quarter Size Outline Package (QSOP)	RQ-16

CAUTION

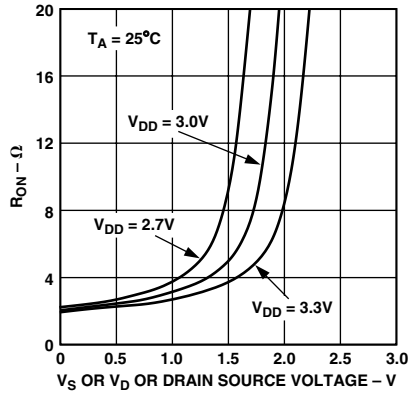
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG774A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



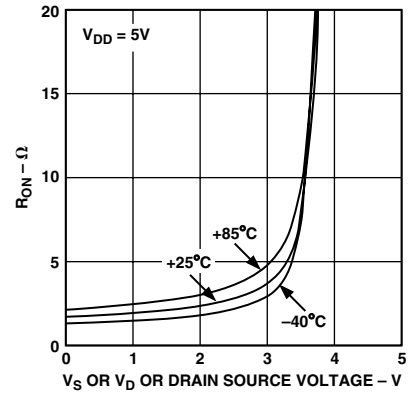
Typical Performance Characteristics—ADG774A



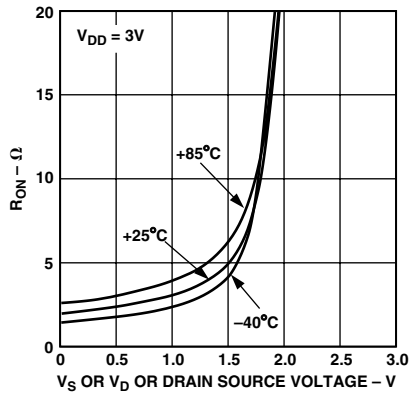
TPC 1. On Resistance as a Function of V_D (V_S) for Various Single Supplies



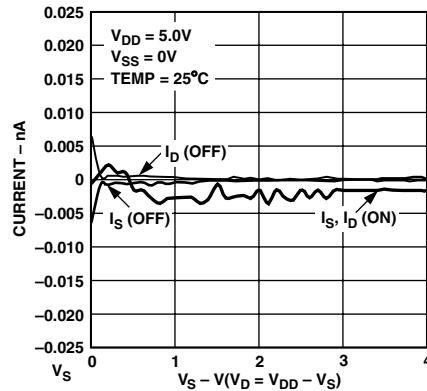
TPC 2. On Resistance as a Function of V_D (V_S) for Various Single Supplies



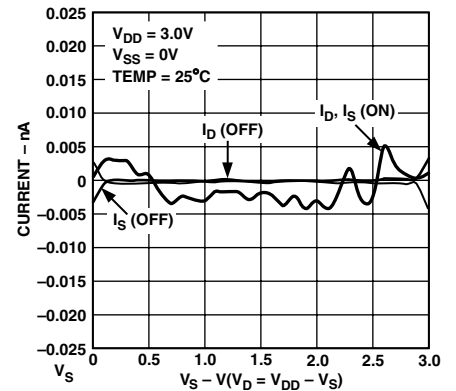
TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures with 5 V Single Supplies



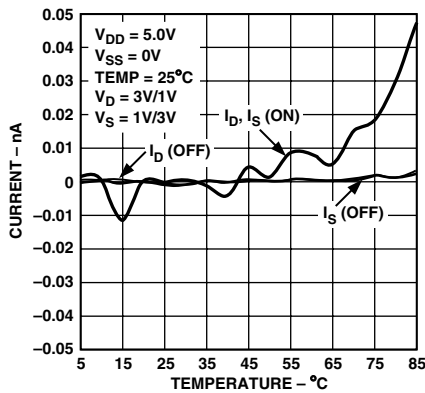
TPC 4. On Resistance as a Function of V_D (V_S) for Different Temperatures with 3 V Single Supplies



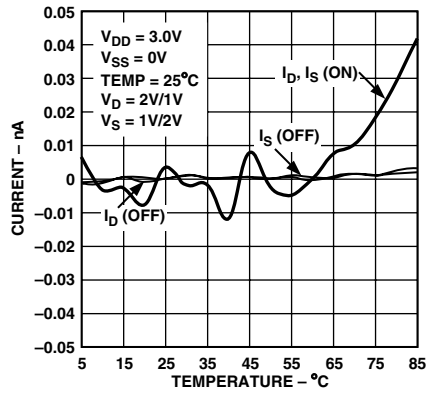
TPC 5. Leakage Current as a Function of V_D (V_S)



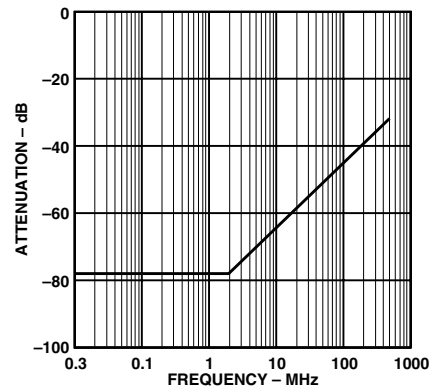
TPC 6. Leakage Current as a Function of V_D (V_S)



TPC 7. Leakage Current as a Function of Temperature

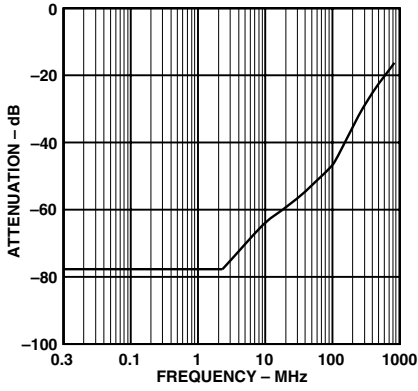


TPC 8. Leakage Current as a Function of Temperature

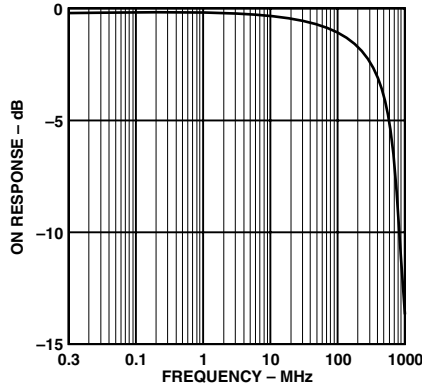


TPC 9. Off Isolation vs. Frequency

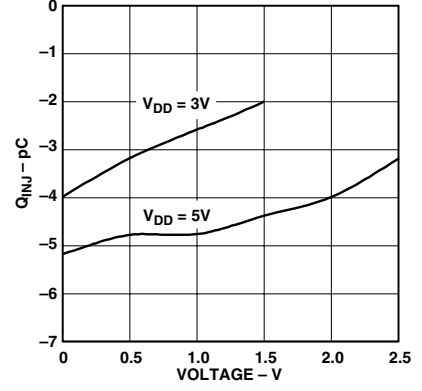
ADG774A



TPC 10. Crosstalk vs. Frequency



TPC 11. Bandwidth



TPC 12. Charge Injection vs. Source Voltage

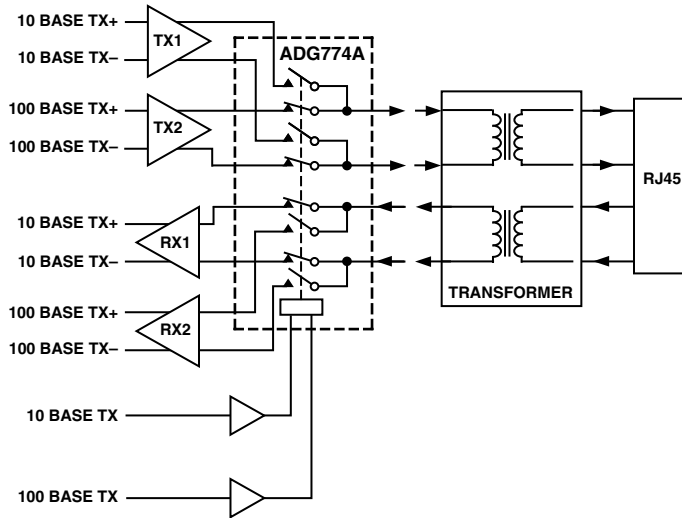


Figure 1. Full Duplex Transceiver

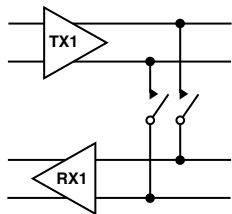


Figure 2. Loop Back

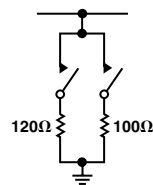


Figure 3. Line Termination

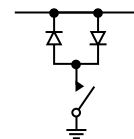
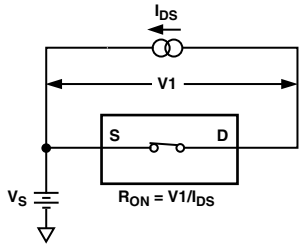
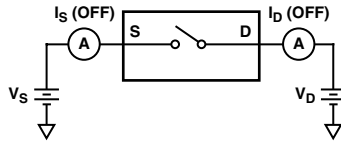


Figure 4. Line Clamp

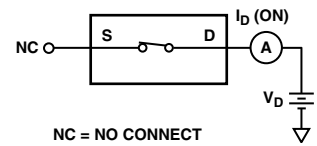
Test Circuits



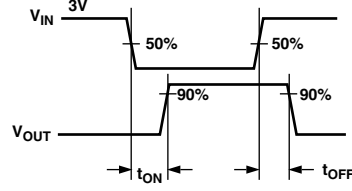
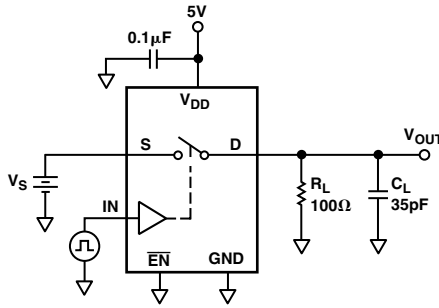
Test Circuit 1. On Resistance



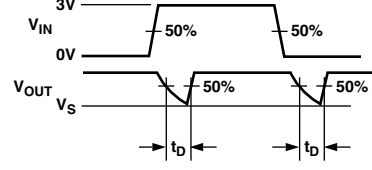
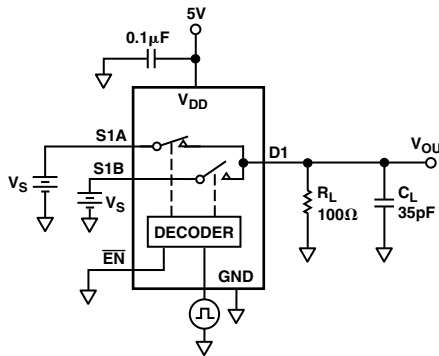
Test Circuit 2. Off Leakage



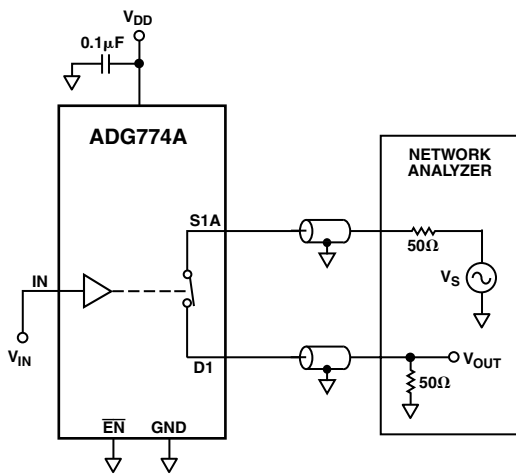
Test Circuit 3. On Leakage



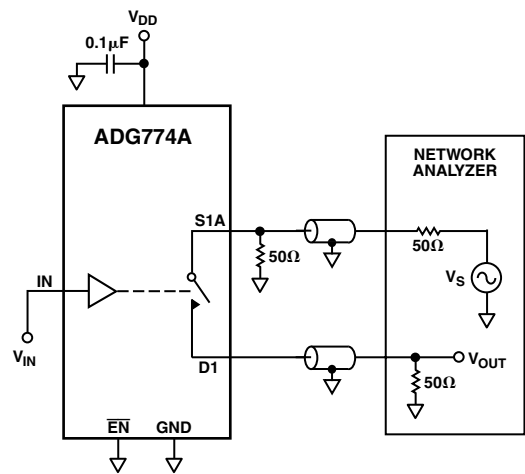
Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay

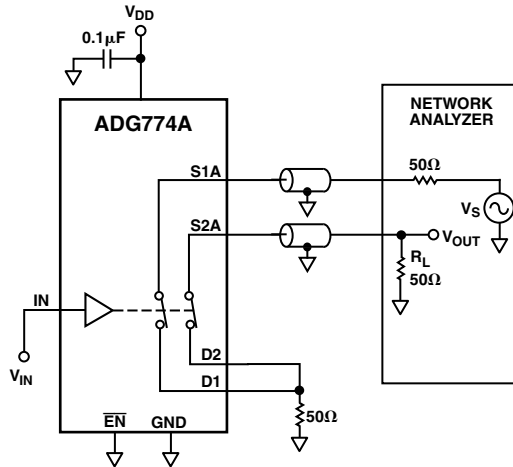


Test Circuit 6. Bandwidth

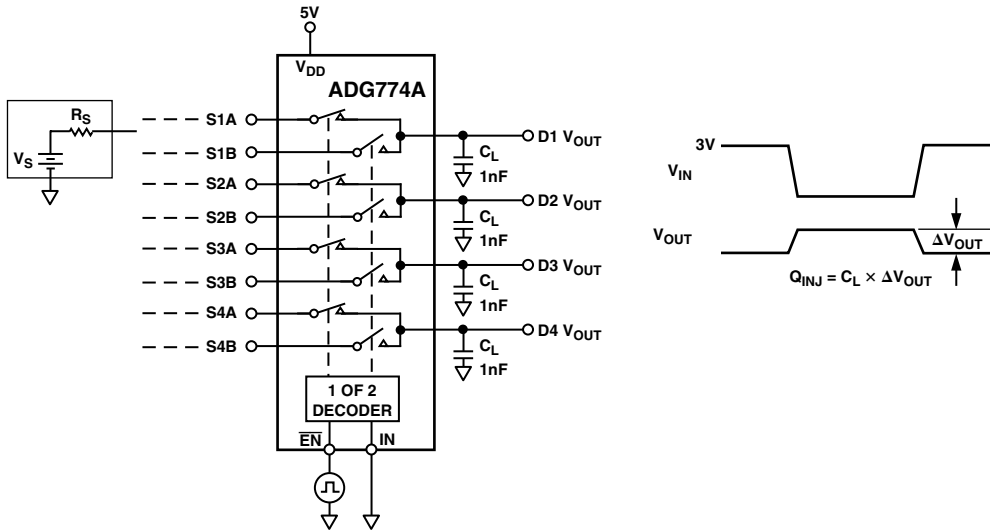


Test Circuit 7. Off Isolation

ADG774A



Test Circuit 8. Channel-to-Channel Crosstalk



Test Circuit 9. Charge Injection

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead QSOP (RQ-16)

