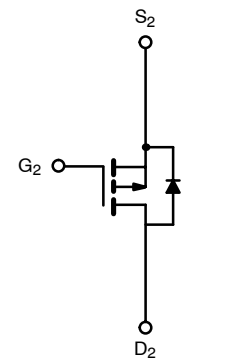
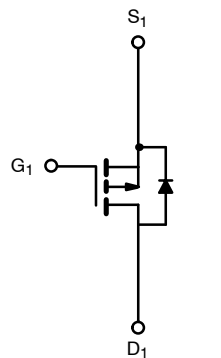
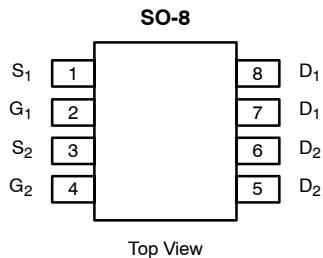




Dual P-Channel 60-V (D-S) 175° MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-60	0.120 @ $V_{GS} = -10$ V	-3.1
	0.150 @ $V_{GS} = -4.5$ V	-2.8



Ordering Information: Si4948BEY—E3 (Lead Free)
Si4948BEY-T1—E3 (Lead Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-60		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-3.1	-2.4	A
		$T_A = 70^\circ\text{C}$	-2.6	-2.0	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	-25			
Continuous Source Current (Diode Conduction) ^a	I_S	-2	-1.1		
Avalanche Current	I_{AS}	15		mJ	
Single Pulse Avalanche Energy		E_{AS}	11		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.4	1.4	W
		$T_A = 70^\circ\text{C}$	1.7	0.95	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	53	62.5	$^\circ\text{C}/\text{W}$
		Steady State	85	110	
Maximum Junction-to-Foot	R_{thJF}	30	37		

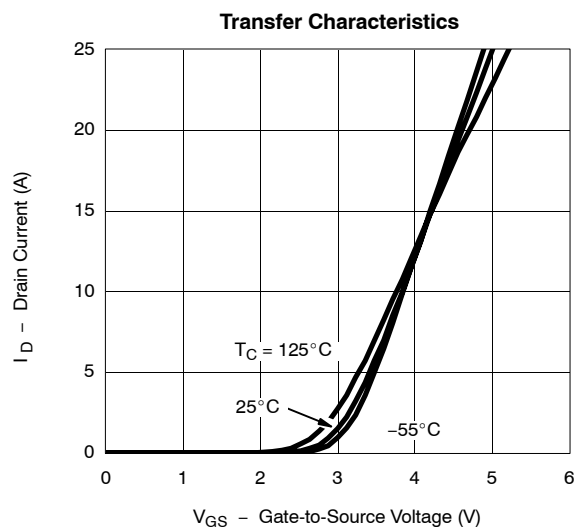
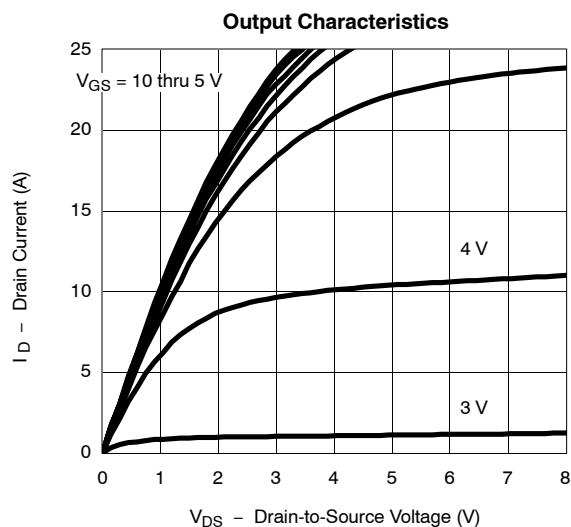
Notes
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1		-3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 70 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-25			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -3.1 A		0.100	0.120	Ω
		V _{GS} = -4.5 V, I _D = -0.2 A		0.126	0.150	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -3.1 A		8.5		S
Diode Forward Voltage ^a	V _{SD}	I _S = -2 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -3.1 A		14.5	22	nC
Gate-Source Charge	Q _{gs}			2.2		
Gate-Drain Charge	Q _{gd}			3.7		
Gate Resistance	R _g	f = 1 MHz		14		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, R _L = 30 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 6 Ω		10	15	ns
Rise Time	t _r			15	22	
Turn-Off Delay Time	t _{d(off)}			50	75	
Fall Time	t _f			35	55	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2 A, di/dt = 100 A/μs		30	50	

Notes

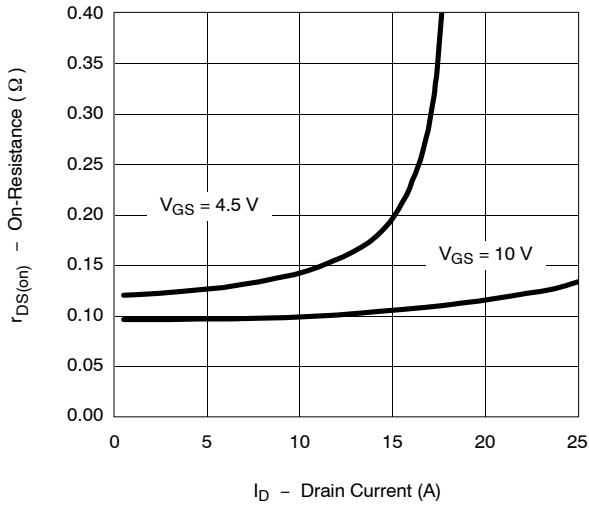
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

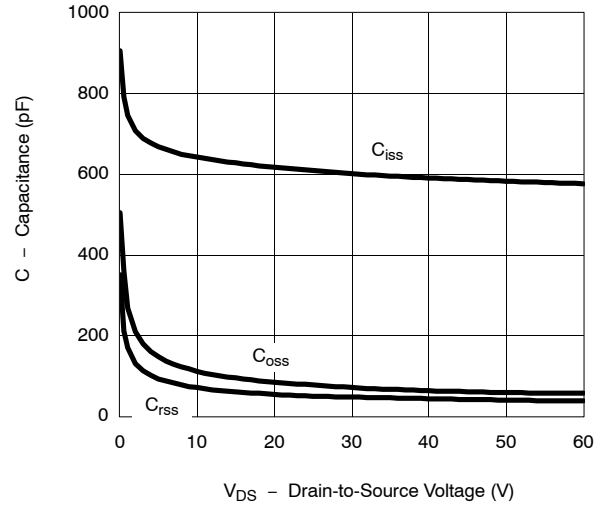


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

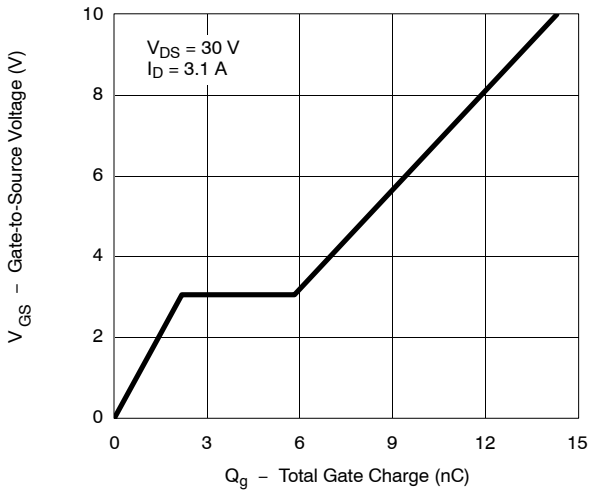
On-Resistance vs. Drain Current



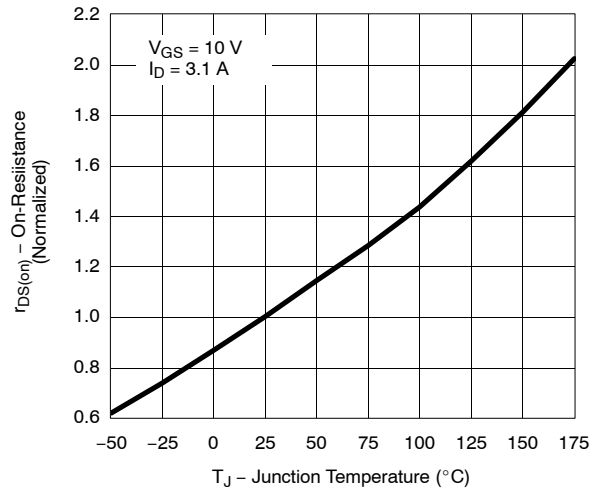
Capacitance



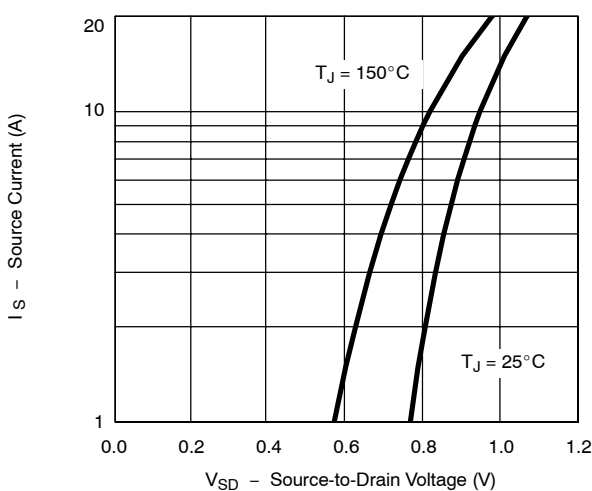
Gate Charge



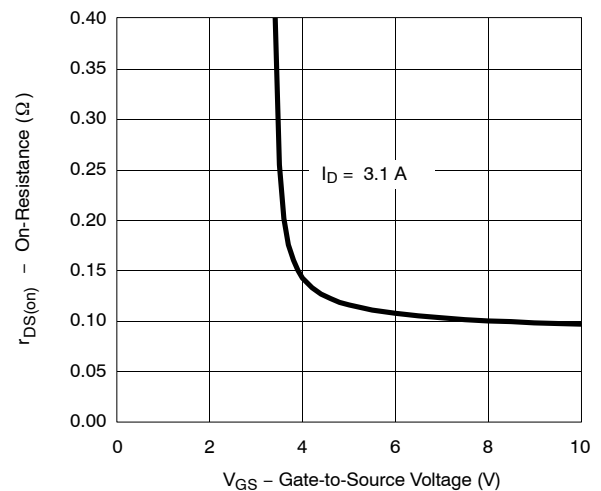
On-Resistance vs. Junction Temperature



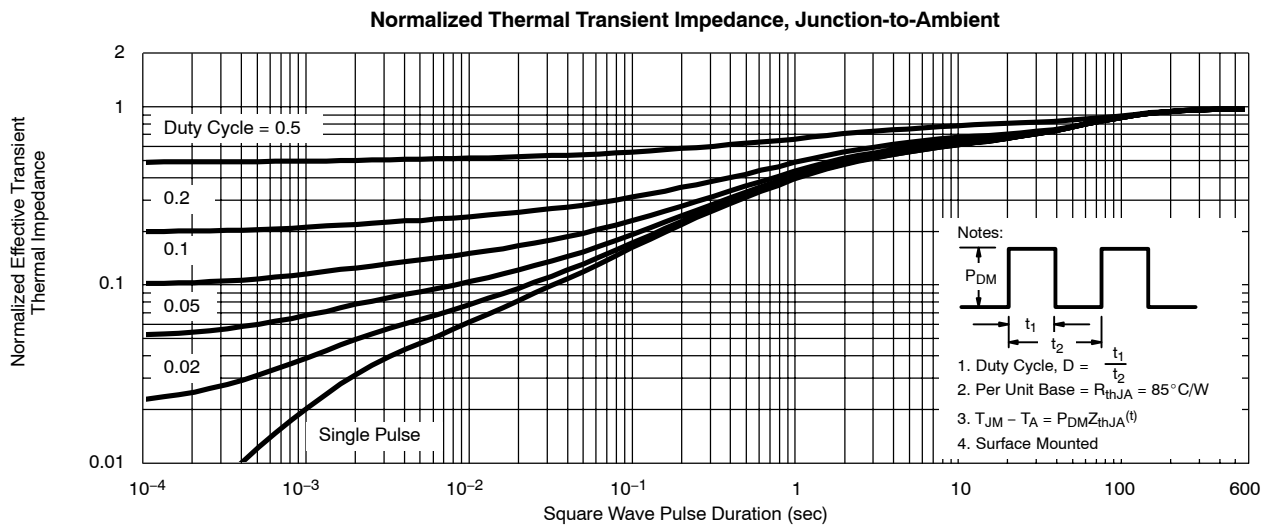
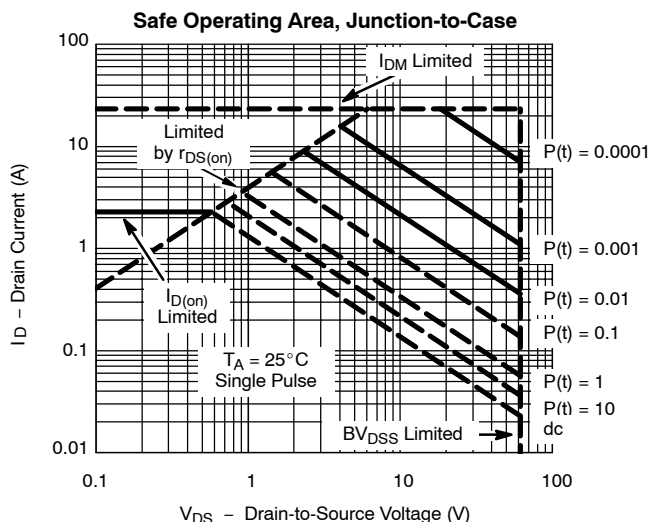
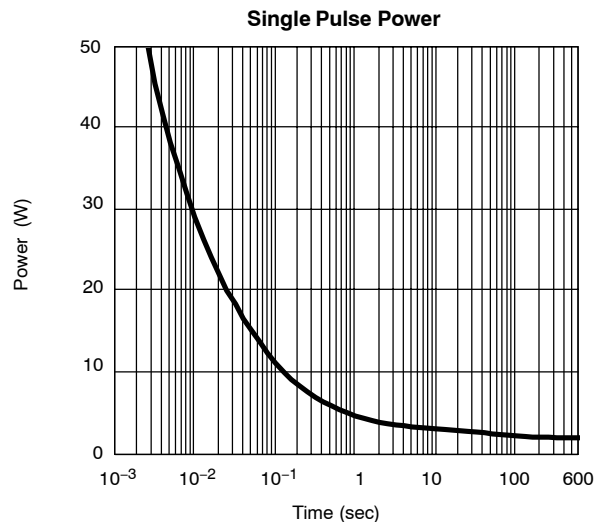
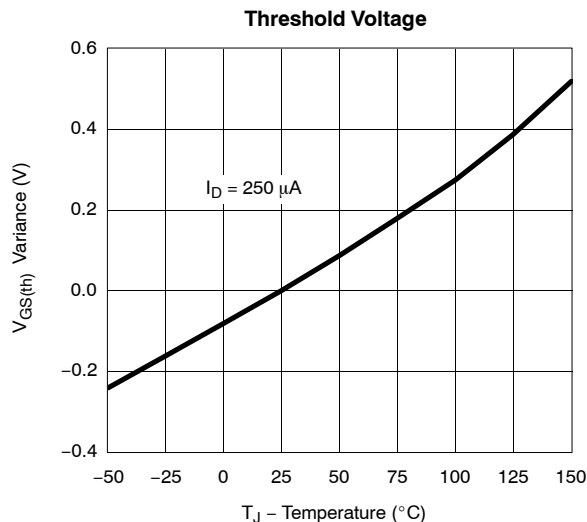
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

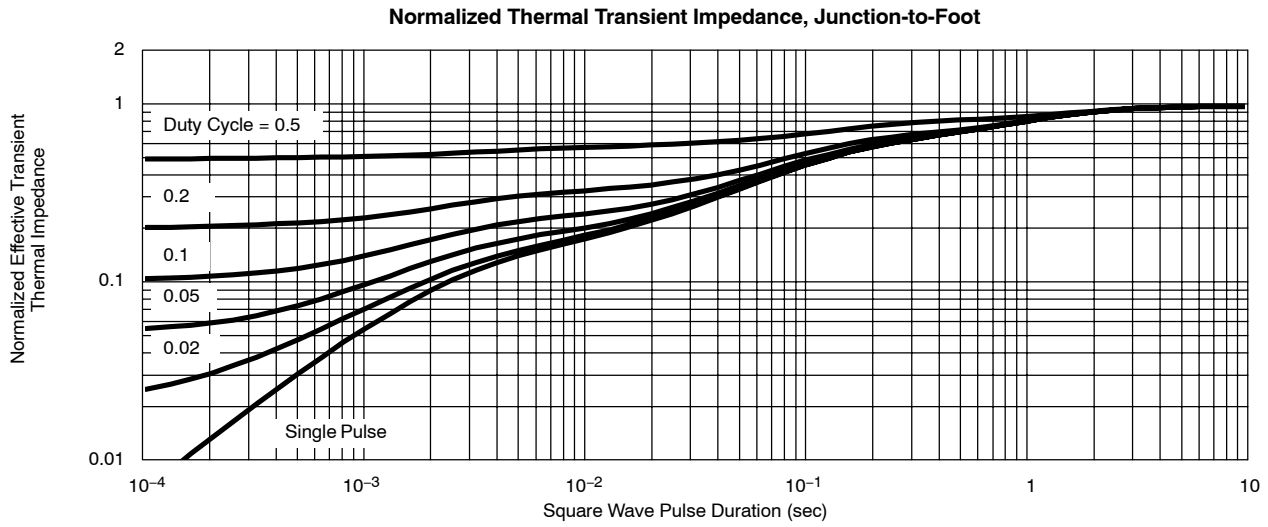


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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