

IRFB11N50APbF

HEXFET® Power MOSFET

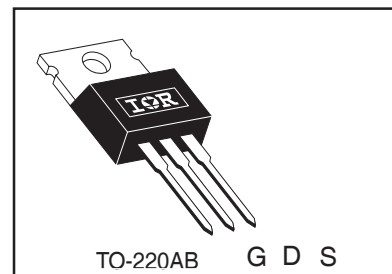
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

V _{DSS}	R _{ds(on)} max	I _D
500V	0.52Ω	11A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	11	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	7.0	
I _{DM}	Pulsed Drain Current ①	44	
P _D @ T _C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	6.9	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Applicable Off Line SMPS Topologies:

- Two Transistor Forward
- Half & Full Bridge
- Power Factor Correction Boost

Notes ① through ③ are on page 8

11/11/03

IRFB11N50APbF

Static @ T_J = 25°C (unless otherwise specified)

International
Rectifier

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 250μA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.52	Ω	V _{GS} = 10V, I _D = 6.6A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 500V, V _{GS} = 0V
		—	—	250		V _{DS} = 400V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	6.1	—	—	S	V _{DS} = 50V, I _D = 6.6A
Q _g	Total Gate Charge	—	—	52	nC	I _D = 11A V _{DS} = 400V V _{GS} = 10V, See Fig. 6 and 13 ④
Q _{gs}	Gate-to-Source Charge	—	—	13		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	18		
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = 250V I _D = 11A R _G = 9.1Ω R _D = 22Ω, See Fig. 10 ④
t _r	Rise Time	—	35	—		
t _{d(off)}	Turn-Off Delay Time	—	32	—		
t _f	Fall Time	—	28	—		
C _{iss}	Input Capacitance	—	1423	—		
C _{oss}	Output Capacitance	—	208	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz, See Fig. 5 V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz V _{GS} = 0V, V _{DS} = 400V, f = 1.0MHz V _{GS} = 0V, V _{DS} = 0V to 400V ⑤
C _{riss}	Reverse Transfer Capacitance	—	8.1	—		
C _{oss}	Output Capacitance	—	2000	—		
C _{oss}	Output Capacitance	—	55	—		
C _{oss eff.}	Effective Output Capacitance	—	97	—		

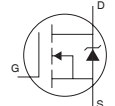
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	275	mJ
I _{AR}	Avalanche Current①	—	11	A
E _{AR}	Repetitive Avalanche Energy①	—	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.75	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	44		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 11A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	510	770	ns	T _J = 25°C, I _F = 11A
Q _{rr}	Reverse Recovery Charge	—	3.4	5.1	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

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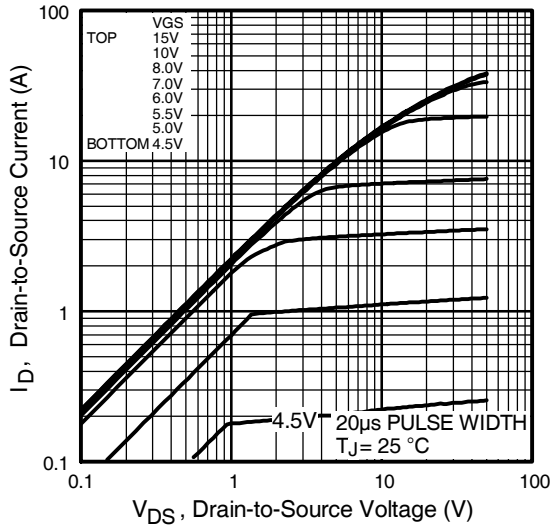


Fig 1. Typical Output Characteristics

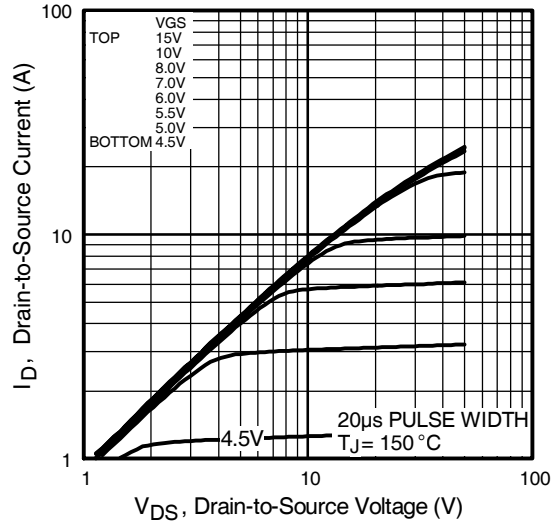


Fig 2. Typical Output Characteristics

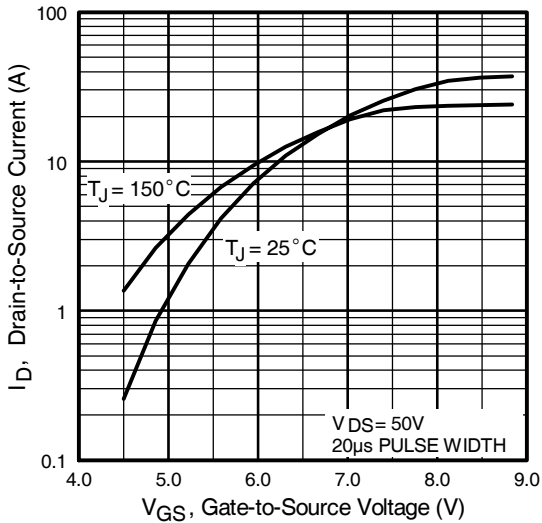


Fig 3. Typical Transfer Characteristics

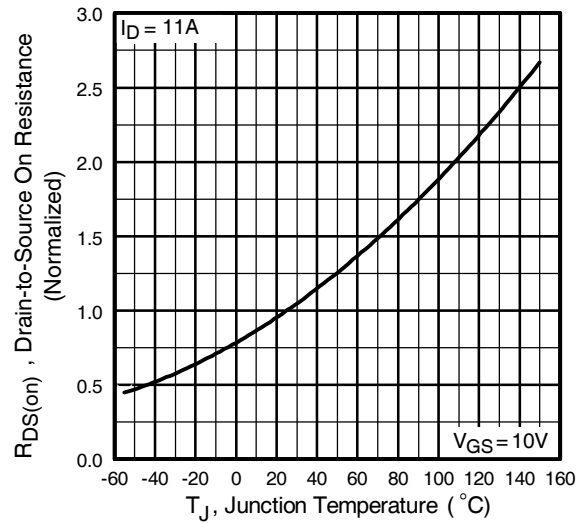


Fig 4. Normalized On-Resistance Vs. Temperature

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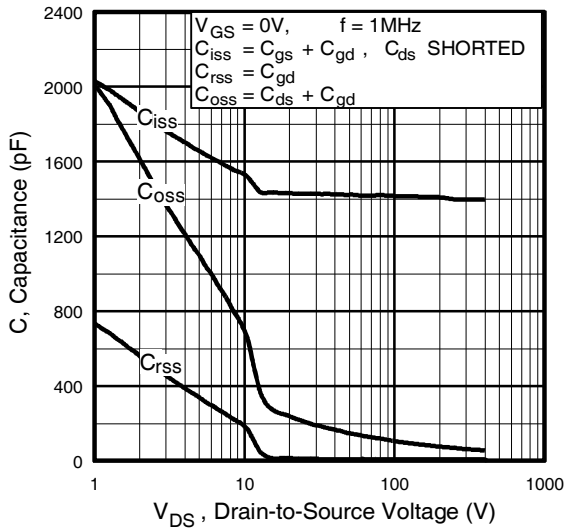


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

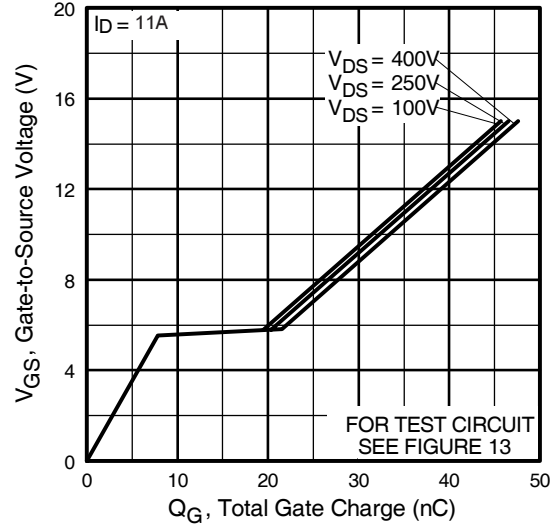


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

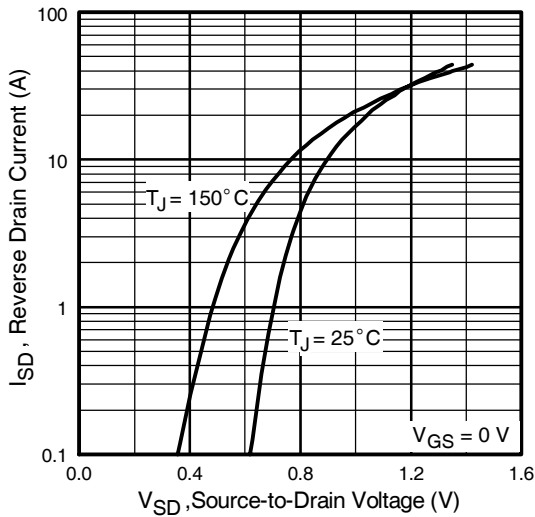


Fig 7. Typical Source-Drain Diode Forward Voltage

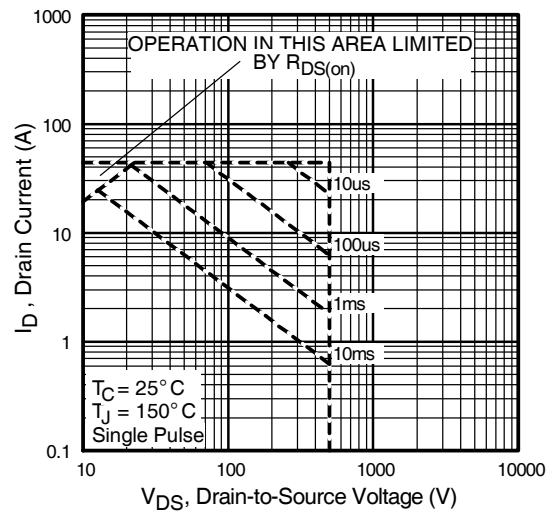


Fig 8. Maximum Safe Operating Area

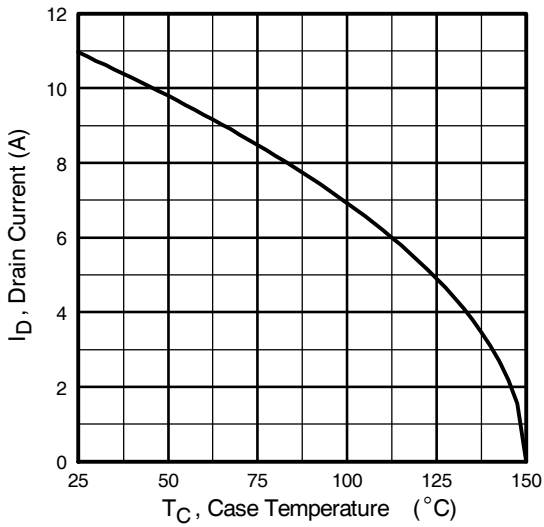


Fig 9. Maximum Drain Current Vs. Case Temperature

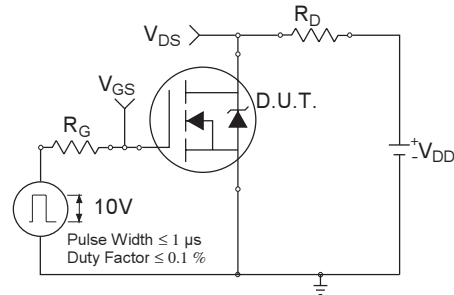


Fig 10a. Switching Time Test Circuit

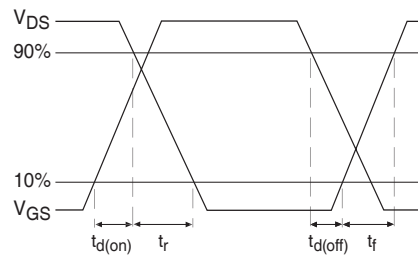


Fig 10b. Switching Time Waveforms

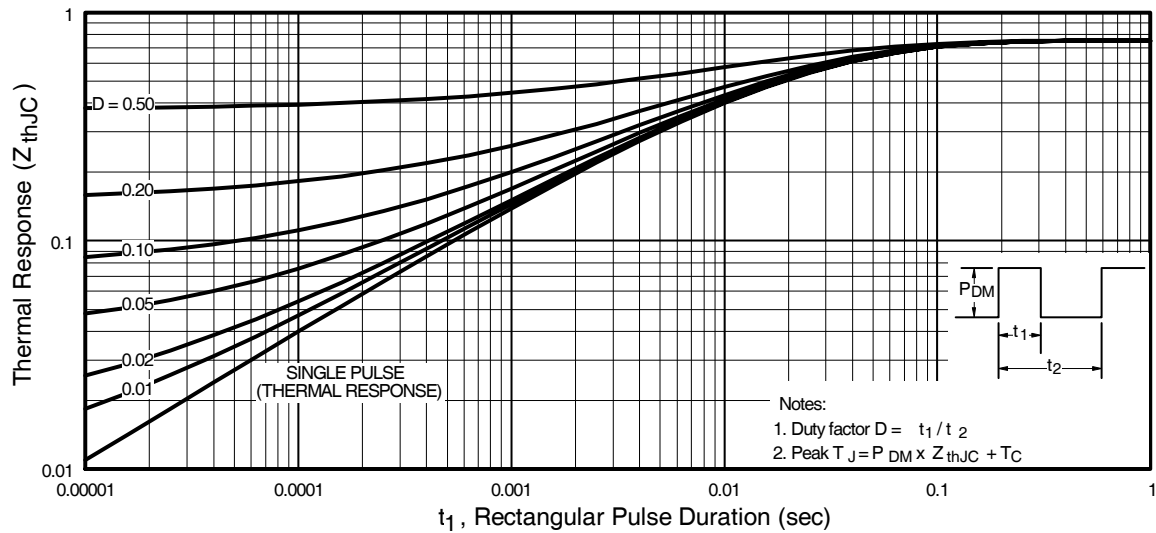


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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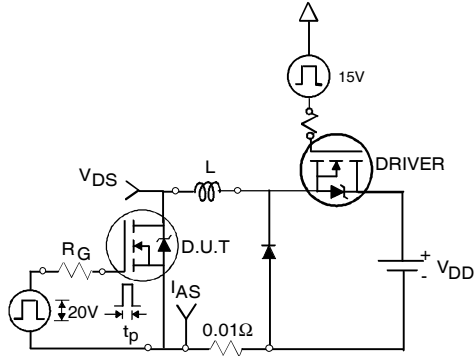


Fig 12a. Unclamped Inductive Test Circuit

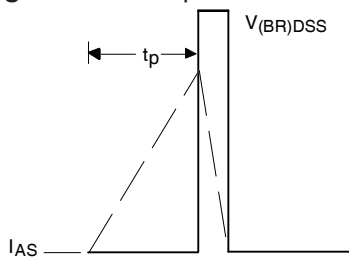


Fig 12b. Unclamped Inductive Waveforms

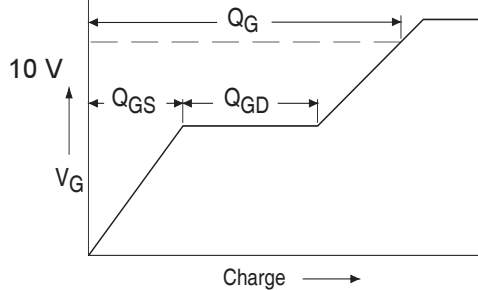


Fig 13a. Basic Gate Charge Waveform

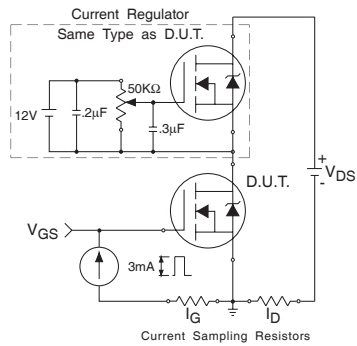


Fig 13b. Gate Charge Test Circuit

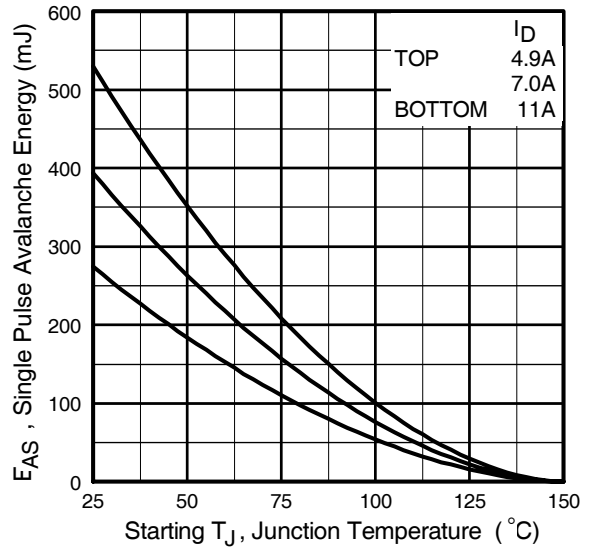


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

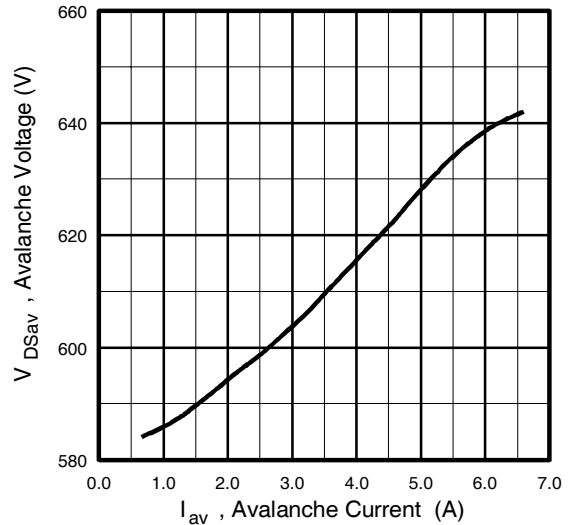
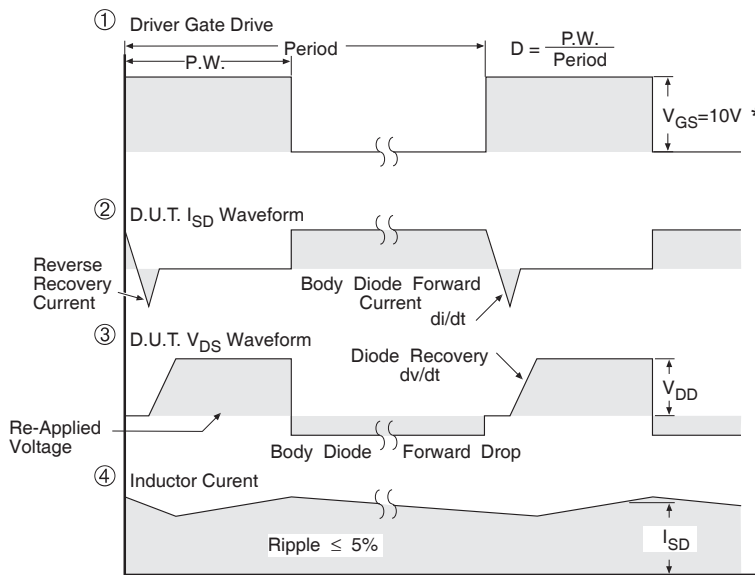
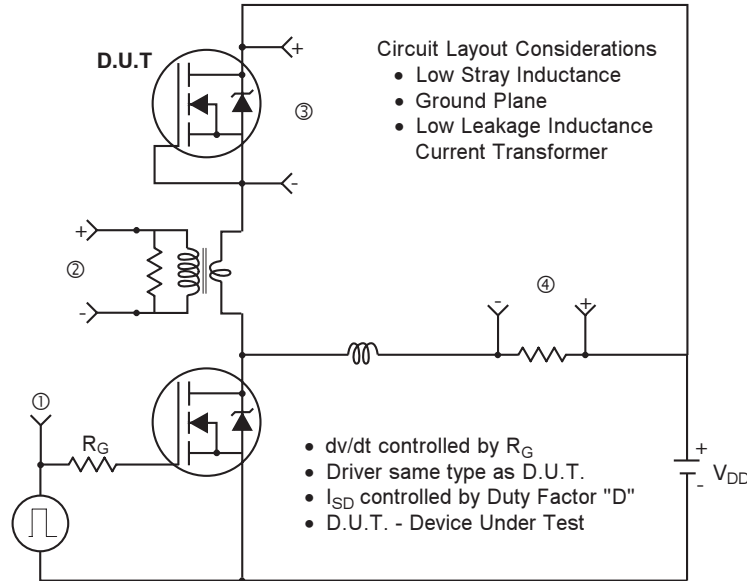


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



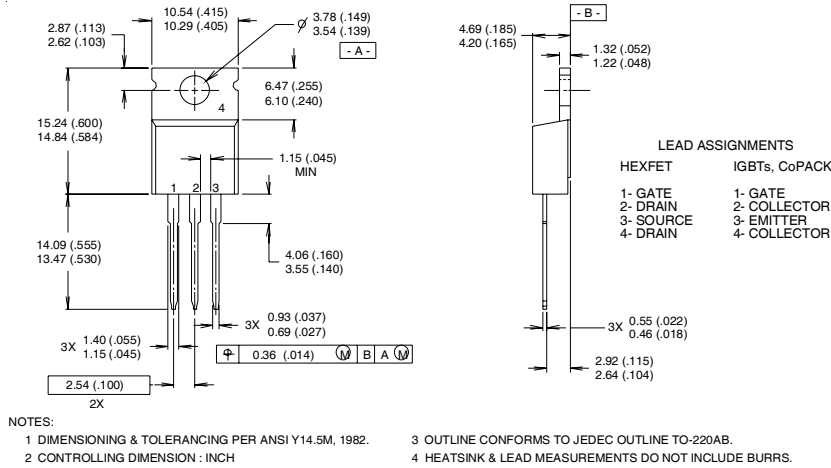
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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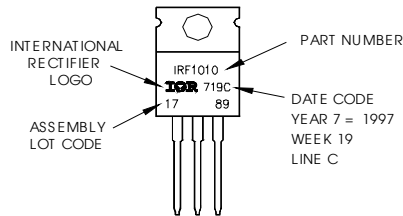


TO-220AB Package Outline



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 4.5\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 11\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 11\text{A}$, $di/dt \leq 140\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.



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