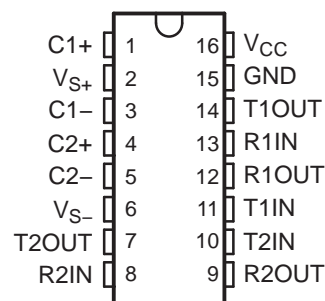# DUAL RS-232 DRIVER/RECEIVER
WITH IEC61000-4-2 PROTECTION

FEATURES

- **Meets or Exceeds TIA/RS-232-F and ITU Recommendation V.28**
- **Operates From a Single 5-V Power Supply With 1.0-µF Charge-Pump Capacitors**
- **Operates up to 120 kbit/s**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typical**
- **ESD Protection Exceeds JESD22**
  - **2000-V Human-Body Model (HBM) (A114-A)**
- **Upgrade With Improved ESD (15-kV HBM) and 0.1-µF Charge-Pump Capacitors Is Available With the TRS202**

APPLICATIONS

- **TIA/RS-232-F**
- **Battery-Powered Systems**
- **Terminals**
- **Modems**
- **Computers**

D, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

C1+	1	16	V_{CC}
V_{S+}	2	15	GND
C1−	3	14	T1OUT
C2+	4	13	R1IN
C2−	5	12	R1OUT
$V_{S−}$	6	11	T1IN
T2OUT	7	10	T2IN
R2IN	8	9	R2OUT

DESCRIPTION/ORDERING INFORMATION

The TRS232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/RS-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/RS-232-F inputs to 5-V TTL/CMOS levels. This receiver has a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinASIC is a trademark of Texas Instruments.

ORDERING INFORMATION

T_A	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 25	TRS232CN	TRS232CN
	SOIC – D	Tube of 40	TRS232CD	TRS232C
		Reel of 2500	TRS232CDR	
	SOIC – DW	Tube of 40	TRS232CDW	TRS232C
		Reel of 2000	TRS232CDWR	
	SOP – NS	Reel of 2000	TRS232CNSR	TRS232C
	TSSOP – PW	Tube of 25	TRS232CPW	TRS232C
		Reel of 2000	TRS232CPWR	
–40°C to 85°C	PDIP – N	Tube of 25	TRS232IN	TRS232IN
	SOIC – D	Tube of 40	TRS232ID	TRS232I
		Reel of 2500	TRS232IDR	
	SOIC – DW	Tube of 40	TRS232IDW	TRS232I
		Reel of 2000	TRS232IDWR	
	SOP – NS	Reel of 2000	TRS232INSR	TRS232I
	TSSOP – PW	Tube of 25	TRS232IPW	TRS232I
		Reel of 2000	TRS232IPWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
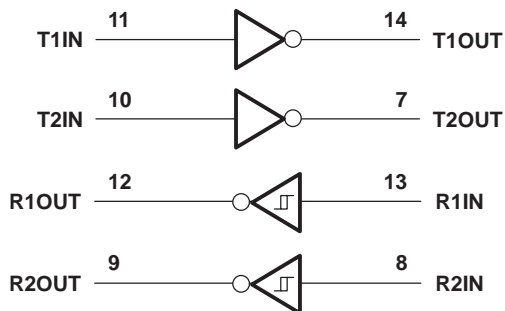
Product Folder Link(s): *TRS232*

FUNCTION TABLES

Each Driver[1]

INPUT TnIN	OUTPUT TnOUT
L	H
H	L

(1) H = high level, L = low level

Each Receiver[1]

INPUT RnIN	OUTPUT RnOUT
L	H
H	L

(1) H = high level, L = low level

LOGIC DIAGRAM (POSITIVE LOGIC)

T1IN 11 ▷○ 14 T1OUT

T2IN 10 ▷○ 7 T2OUT

R1OUT 12 ○◁ 13 R1IN

R2OUT 9 ○◁ 8 R2IN

Product Folder Link(s): TRS232

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Input supply voltage range[2]		−0.3	6	V
V_{S+}	Positive-output supply voltage range		V_{CC} − 0.3	15	V
V_{S-}	Negative-output supply voltage range		−0.3	−15	V
V_I	Input voltage range	Driver	−0.3	V_{CC} + 0.3	V
		Receiver		±30	
V_O	Output voltage range	T1OUT, T2OUT	V_{S-} − 0.3	V_{S+} + 0.3	V
		R1OUT, R2OUT	−0.3	V_{CC} + 0.3	
	Short-circuit duration	T1OUT, T2OUT		Unlimited	
θ_{JA}	Package thermal impedance[3][4]	D package		73	°C/W
		DW package		57	
		N package		67	
		NS package		64	
		PW package		108	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J$(max) − $T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	T1IN, T2IN	2			V
V_{IL}	Low-level input voltage	T1IN, T2IN			0.8	V
	Receiver input voltage	R1IN, R2IN			±30	V
T_A	Operating free-air temperature	TRS232C	0		70	°C
		TRS232I	−40		85	

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1−C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics[(1)]

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP[(2)]	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
V_{OL}	Low-level output voltage [(3)]	T1OUT, T2OUT	R_L = 3 kΩ to GND			−7	−5	V
r_o	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-}$ = 0, V_O = ±2 V	300			Ω
I_{OS}[(4)]	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	μA

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

Switching Characteristics[(1)]

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/μs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/μs
	Data rate	One TnOUT switching		120		kbit/s

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	$I_{OH} = -1$ mA		3.5			V
V_{OL}	Low-level output voltage [3]	R1OUT, R2OUT	$I_{OL} = 3.2$ mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	$V_{CC} = 5$ V,	$T_A = 25°C$		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	$V_{CC} = 5$ V,	$T_A = 25°C$	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	$V_{CC} = 5$ V		0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	$V_{CC} = 5$ V,	$T_A = 25°C$	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

Switching Characteristics[1]

V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT
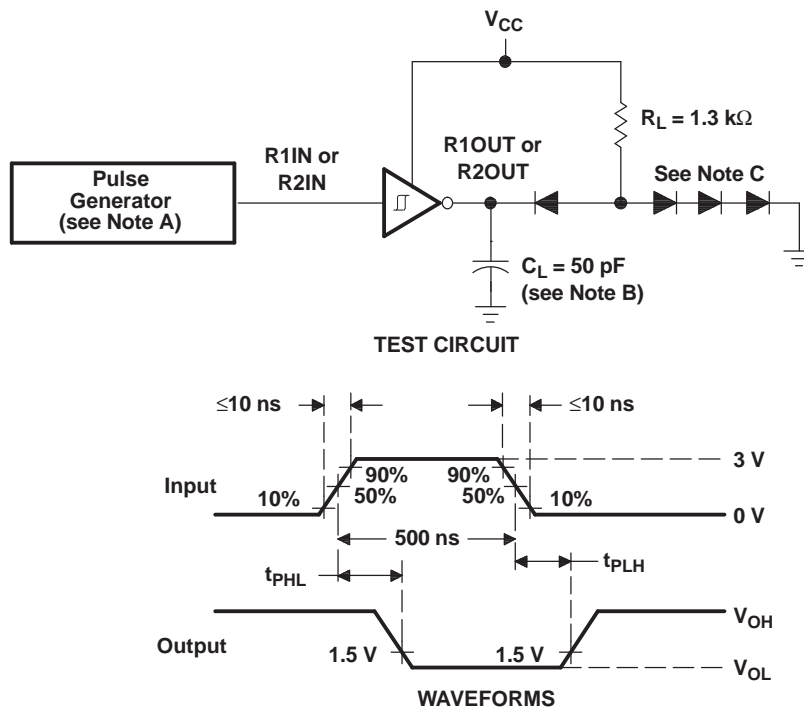
WAVEFORMS

A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.
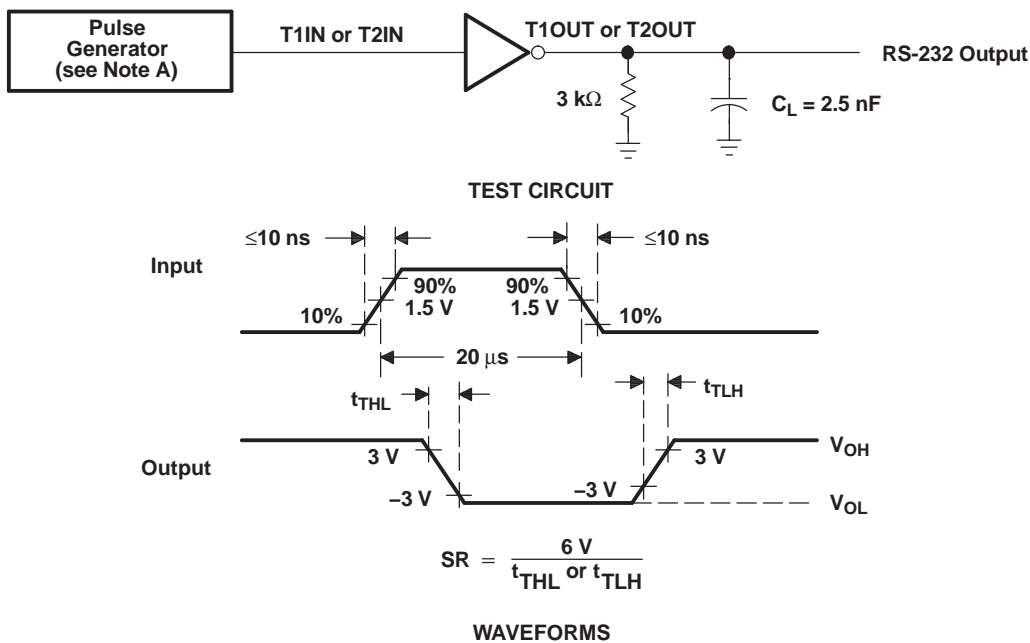
C. All diodes are 1N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION (continued)

Pulse Generator (see Note A) — T1IN or T2IN — T1OUT or T2OUT — RS-232 Output

R_L C_L = 10 pF (see Note B)

TEST CIRCUIT

≤10 ns   ≤10 ns   3 V
Input   90%   90%   50%   50%   10%   10%   0 V
5 µs
t_{PHL} t_{PLH}
Output   90%   90% V_{OH} 10%   10% V_{OL}
t_{THL} t_{TLH}

$$SR = \frac{0.8\,(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} - V_{OH})}{t_{THL}}$$

WAVEFORMS

A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)

Pulse Generator (see Note A) — T1IN or T2IN — T1OUT or T2OUT — RS-232 Output

3 kΩ C_L = 2.5 nF

TEST CIRCUIT

≤10 ns   ≤10 ns
Input   90%   90%   1.5 V   1.5 V   10%   10%
20 µs
t_{THL} t_{TLH}
Output   3 V   3 V V_{OH} −3 V   −3 V V_{OL}

$$SR = \frac{6\,V}{t_{THL} \text{ or } t_{TLH}}$$

WAVEFORMS

A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

APPLICATION INFORMATION
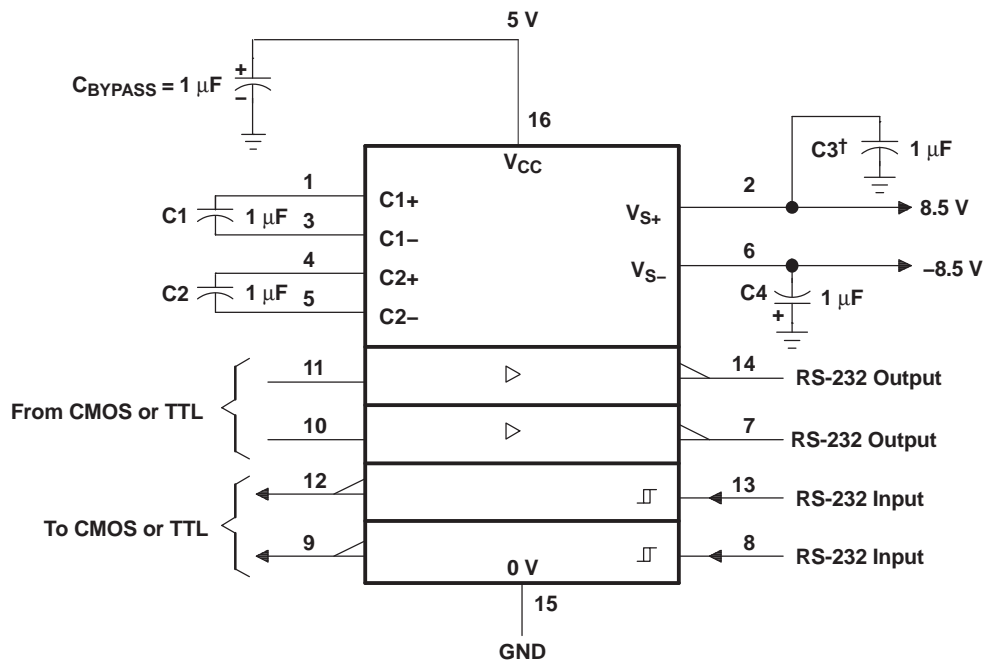
† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the TRS202 can operate with 0.1-µF capacitors.

Figure 4. Typical Operating Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TRS232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS232INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS232N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS232NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS232NS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232NSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS232NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS232NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS232DR	SOIC	D	16	2500	346.0	346.0	33.0
TRS232DR	SOIC	D	16	2500	333.2	345.9	28.6
TRS232DWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRS232IDR	SOIC	D	16	2500	333.2	345.9	28.6
TRS232IDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRS232NSR	SO	NS	16	2000	346.0	346.0	33.0

MECHANICAL DATA

NS (R-PDSO-G)**　　　　　　　　　　　　PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:　A.　All linear dimensions are in millimeters.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/I 10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed .006 (0,15) per end.
        ⚠D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AC.

TEXAS INSTRUMENTS
www.ti.com

D(R−PDSO−G16)

Example Board Layout
(Note C)

0.60

1.27

1.55

5.40

Stencil Openings
(Note D)

0.55

1.27

1.5

5.40

Non Solder Mask Define Pad

0.6

Solder Mask Opening
(Note E)

1.55

Pad Geometry
(Note C)

0.07
ALL AROUND
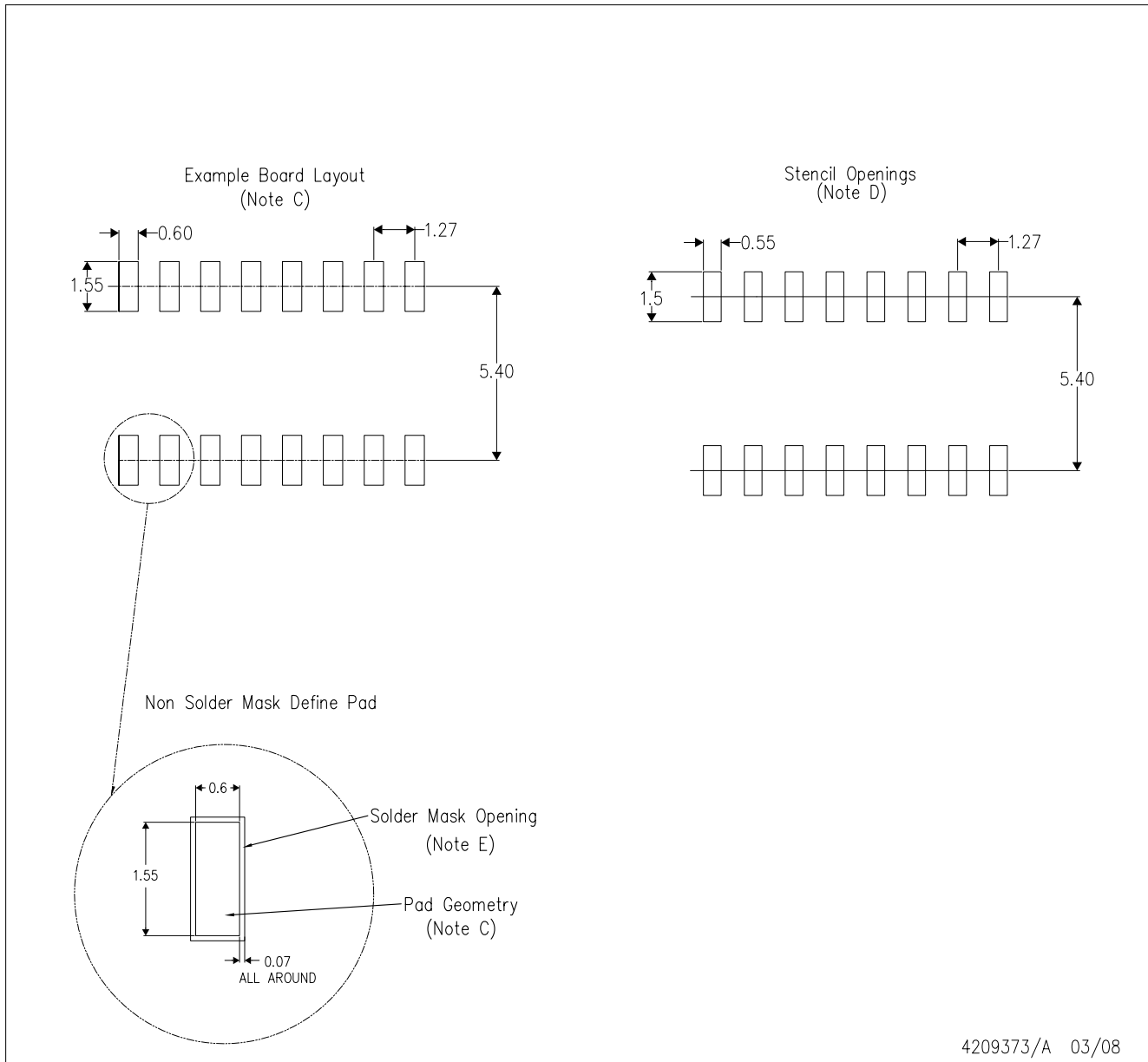
4209373/A   03/08

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Refer to IPC7351 for alternate board design.
           D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525
           E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**TEXAS
INSTRUMENTS**
www.ti.com

DW (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
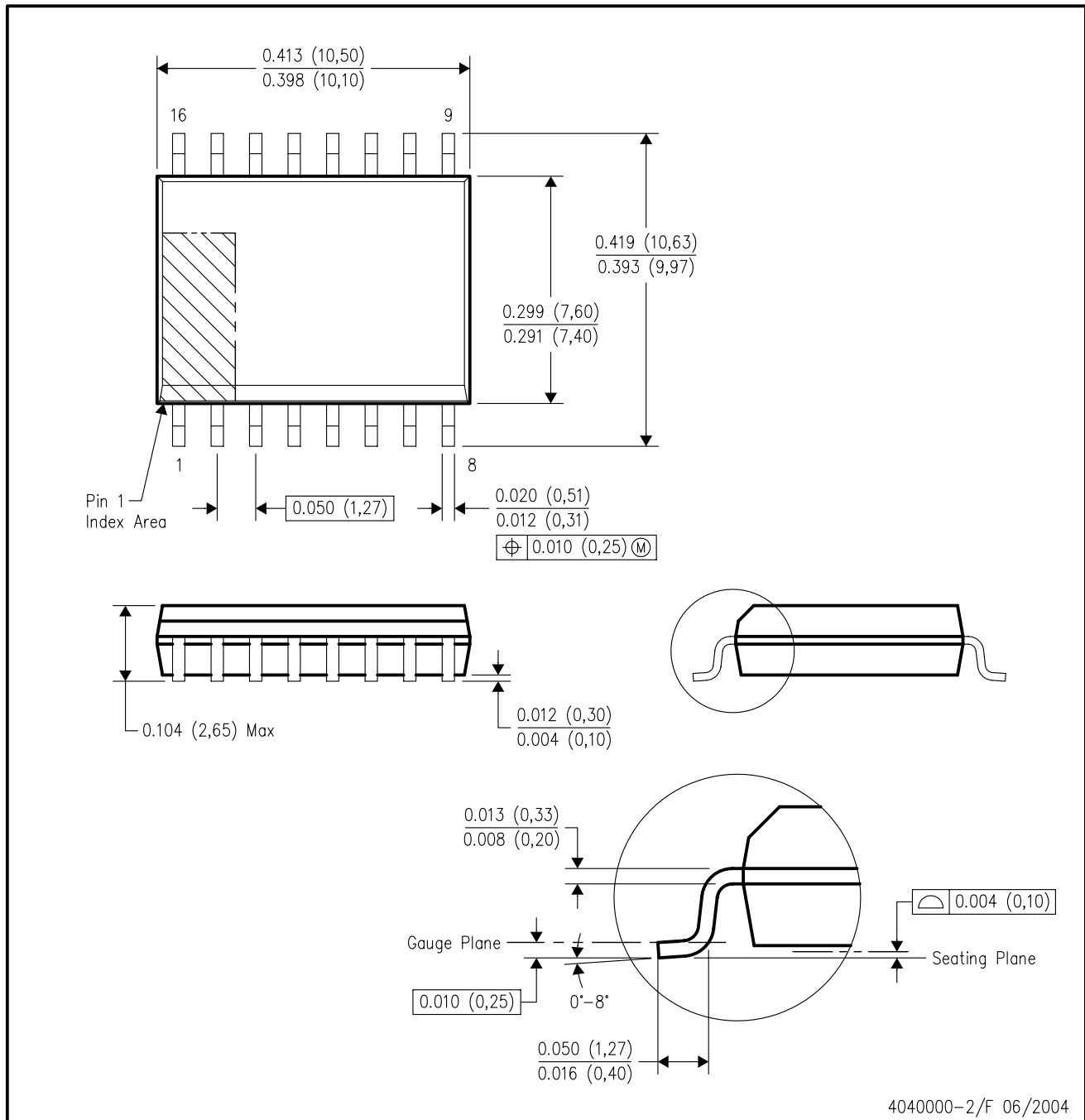
4040000−2/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AA.