HIGH-RESOLUTION ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS1282-HT

FEATURES

- **High Resolution:**
  122-dB SNR (250 SPS, High-Resolution Mode)
  119-dB SNR (250 SPS, Low-Power Mode)
- **High Accuracy:**
  THD: –122 dB
  INL: 0.5 ppm
- **Low-Noise PGA**
- **Two-Channel Input MUX**
- **Inherently-Stable Modulator with Fast Responding Over-Range Detection**
- **Flexible Digital Filter:**
  Sinc + FIR + IIR (Selectable)
  Linear or Minimum Phase Response
  Programmable High-Pass Filter
  Selectable FIR Data Rates: 250 SPS to 4 kSPS
- **Filter Bypass Option**
- **Low Power Consumption:**
  High-Resolution Mode: 30 mW
  Low-Power Mode: 22 mW
  Shutdown: 0.9 mW
- **Offset and Gain Calibration Engine**
- **SYNC Input**
- **Analog Supply:**
  Unipolar (5 V) or Bipolar (±2.5 V)
- **Digital Supply: 1.75 V to 3.3 V**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

APPLICATIONS

- **Energy Exploration**
- **Seismic Monitoring**
- **High-Accuracy Instrumentation**

DESCRIPTION

The ADS1282 is an extremely high-performance, single-chip analog-to-digital converter (ADC) with an integrated, low-noise programmable gain amplifier (PGA) and two-channel input multiplexer (MUX). The ADS1282 is suitable for the demanding needs of energy exploration and seismic monitoring environments.

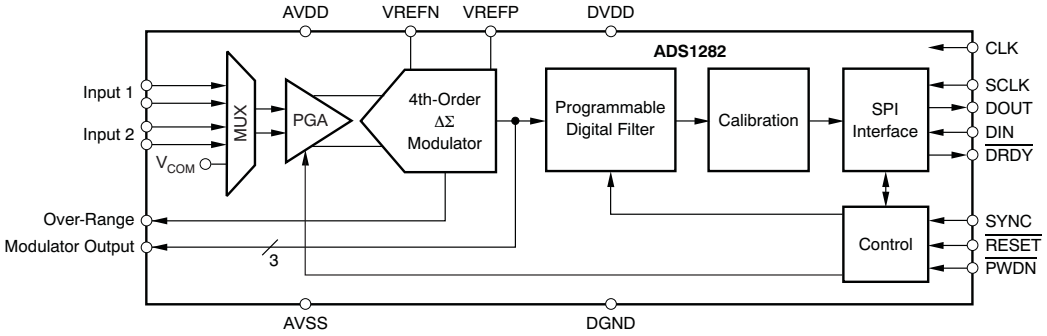
The converter uses a fourth-order, inherently stable, delta-sigma (ΔΣ) modulator that provides outstanding noise and linearity performance. The modulator is used either in conjunction with the on-chip digital filter, or can be bypassed for use with post processing filters.

The flexible input MUX provides an additional external input for measurement, as well as internal self-test connections. The PGA features outstanding low noise (5nV/$\sqrt{\text{Hz}}$) and high input impedance, allowing easy interfacing to geophones and hydrophones over a wide range of gains.

The digital filter provides selectable data rates from 250 to 4000 samples per second (SPS). The high-pass filter (HPF) features an adjustable corner frequency. On-chip gain and offset scaling registers support system calibration.

The synchronization input (SYNC) can be used to synchronize the conversions of multiple ADS1282s. The SYNC input also accepts a clock input for continuous alignment of conversions from an external source.

Two operating modes allow optimization of noise and power. Together, the amplifier, modulator, and filter dissipate 30 mW and only 22 mW in low-power mode. The ADS1282 is fully specified from –55°C to 210°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD	ADS1282SKGDA	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mm	Silicon with backgrind	GND	Al-Si-Cu (0.5%)

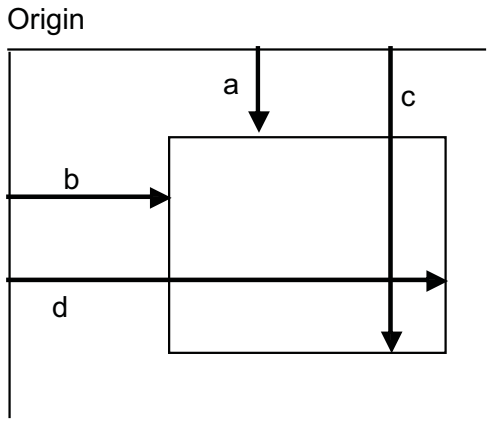
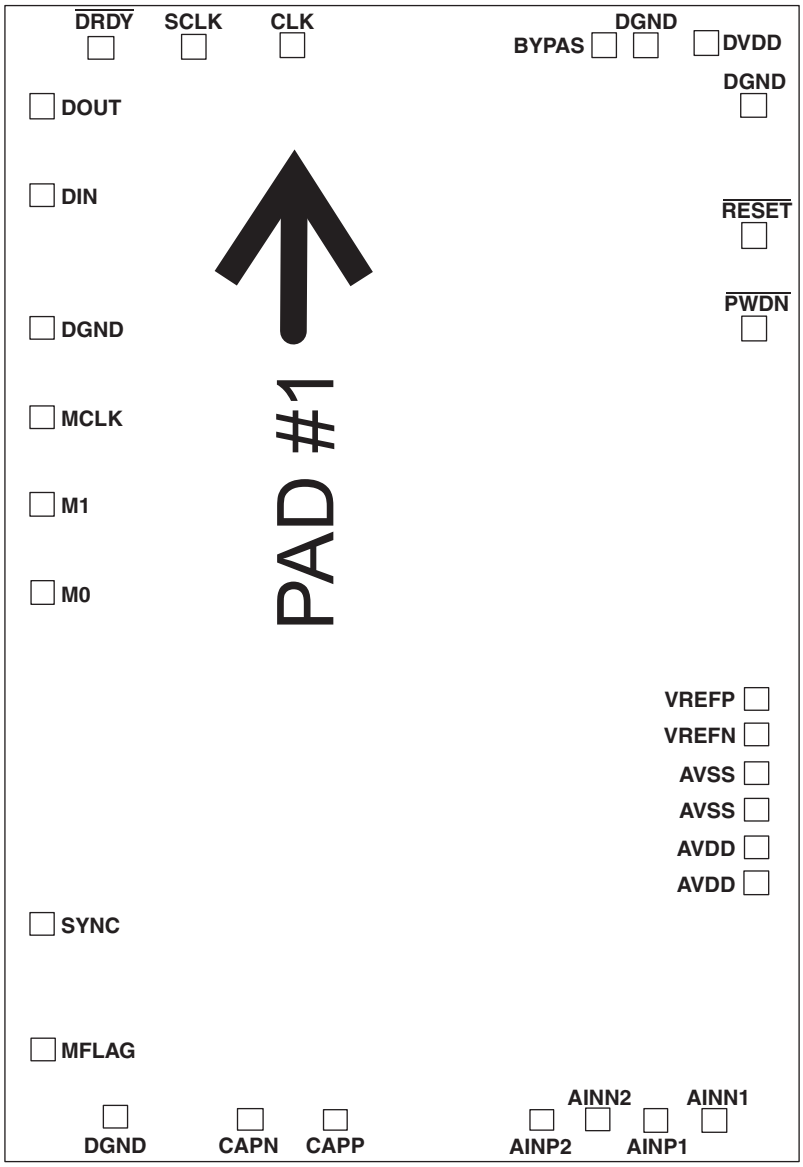


Table 2. Bond Pad Coordinates in Microns - Rev A

DISCRIPTION	PAD NUMBER	a	b	c	d
CLK	1	1512.6	31.45	1588.6	107.45
SCLK	2	1827.6	31.45	1903.6	107.45
DRDY	3	2127.3	31.05	2203.3	107.05
DOUT	4	2310.6	214.35	2386.6	290.35
DIN	5	2310.25	502.25	2386.25	578.25
DGND	6	2310.25	910.05	2386.25	986.05
MCLK	7	2310.6	1199.15	2386.6	1275.15
M1	8	2310.6	1488.35	2386.6	1564.35
M0	9	2310.6	1776.35	2386.6	1852.35
SYNC	10	2310.25	2834.9	2386.25	2910.9
MFLAG	11	2310.65	3233.7	2386.65	3309.7
DGND	12	2084.3	3455.35	2160.3	3531.35
CAPN	13	1655.95	3467.6	1731.95	3543.6
CAPP	14	1386.05	3467.6	1462.05	3543.6
AINP2	15	715.95	3467.6	791.95	3543.6
AINN2	16	526.05	3467.6	602.05	3543.6
AINP1	17	356.05	3467.6	432.05	3543.6
AINN1	18	166.05	3467.6	242.05	3543.6
AVDD	19	25.7	2705.15	101.7	2781.15
AVDD	20	25.7	2609.6	101.7	2685.6
AVSS	21	25.7	2481.2	101.7	2557.2
AVSS	22	25.8	2329.1	101.8	2405.1
VREFN	23	19.2	2220.4	95.2	2296.4
VREFP	24	19.2	2110.4	95.2	2186.4
PWDN	25	31.45	927.5	107.45	1003.5
RESET	26	31.45	630.5	107.45	706.5
DGND	27	31.45	214.1	107.45	290.1
DVDD	28	190.3	31.35	266.3	107.35
DGND	29	389.1	31.35	465.1	107.35
BYPAS	30	503.4	31.35	579.4	107.35



DEVICE INFORMATION

TERMINAL FUNCTIONS

NAME	NO.	FUNCTION	DESCRIPTION
CLK	1	Digital input	Master clock input
SCLK	2	Digital input	Serial clock input
$\overline{\text{DRDY}}$	3	Digital output	Data ready output: read data on falling edge
DOUT	4	Digital output	Serial data output
DIN	5	Digital input	Serial data input
MCLK	7	Digital I/O	Modulator clock output; if in modulator mode: MCLK: Modulator clock output Otherwise, the pin is an unused input (must be tied).
M1	8	Digital I/O	Modulator data output 1; if in modulator mode: M1: Modulator data output 1 Otherwise, the pin is an unused input (must be tied).
M0	9	Digital I/O	Modulator data output 0; if in modulator mode: M0: Modulator data output 0 Otherwise, the pin is an unused input (must be tied).
SYNC	10	Digital input	Synchronize input
MFLAG	11	Digital output	Modulator Over-Range flag: 0 = normal, 1 = modulator over-range
DGND	6, 12, 29, 27	Digital ground	Digital ground, pin 12 is the key ground point
CAPN	13	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN
CAPP	14	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN
AINP2	15	Analog input	Positive analog input 2
AINN2	16	Analog input	Negative analog input 2
AINP1	17	Analog input	Positive analog input 1
AINN1	18	Analog input	Negative analog input 1
AVDD	19, 20	Analog supply	Positive analog power supply
AVSS	21, 22	Analog supply	Negative analog power supply
VREFN	23	Analog input	Negative reference input
VREFP	24	Analog input	Positive reference input
$\overline{\text{PWDN}}$	25	Digital input	Power-down input, active low
$\overline{\text{RESET}}$	26	Digital input	Reset input, active low
DVDD	28	Digital supply	Digital power supply: 1.8 V to 3.3 V
BYPAS	30	Analog	Sub-regulator output: Connect 1-µF capacitor to DGND

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS1282	UNIT
AVDD to AVSS	–0.3 to 5.5	V
AVSS to DGND	–2.8 to 0.3	V
DVDD to DGND	–0.3 to 3.9	V
Input current	100, momentary	mA
Input current	10, continuous	mA
Analog input voltage	AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Operating temperature range	–55 to 210	°C
Storage temperature range	–60 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} (1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS									
Full-scale input voltage		V_{IN} = (AINP – AINN)		$\pm V_{REF}/2 \times$ PGA					V
Absolute input range	AINP or AINN		AVSS + 0.7		AVDD – 1.25	AVSS + 0.7		AVDD – 1.25	V
PGA input voltage noise density				5					nV/√Hz
Differential input impedance(3)				1					GΩ
Common-mode input impedance				100					MΩ
Input bias current				1			1000		nA
Crosstalk		f = 31.25 Hz		–128			–123		dB
MUX on-resistance				30			45		Ω
PGA OUTPUT (CAPP, CAPN)									
Absolute output range			AVSS + 0.4		AVDD – 0.4	AVSS + 0.4		AVDD – 0.4	V
PGA differential output impedance				600			600		Ω
Output impedance tolerance				±10			±10		%
External bypass capacitance				10	100		10	100	nF
Modulator differential input impedance		High-resolution mode		55					kΩ
		Low-power mode		110					kΩ
AC PERFORMANCE									
Signal-to-noise ratio(4)	SNR	High-resolution mode	112	124		110	122		dB
		Low-power mode	109	121		107	119		
Total harmonic distortion(5)	THD	High-resolution mode							
		PGA = 1...16		–122	–99		–102	–99	dB
		PGA = 32		–117	–99		–98	–94	
		PGA = 64		–115			–93		
		Low-power mode							
		PGA = 1...16		–122	–99		–108	–101	dB
		PGA = 32		–113	–99		–95	–91	
		PGA = 64		–109			–87		
Spurious-free dynamic range	SFDR			123					dB
DC PERFORMANCE									
Resolution		No missing codes	31			31			Bits
Data rate	f_{DATA}	FIR filter mode	250		4000	250		4000	SPS
		Sinc filter mode	8000		128,000	8000		128,000	SPS
Integral nonlinearity (INL)(6)		Differential input		0.00005	0.0090		0.002	0.0100	% FSR(7)
Offset error		Shorted input		50	200		99	250	µV
Offset error after calibration(8)				1			2		µV
Offset drift				0.02			0.19		µV/°C

(1) f_{CLK} = system clock.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) Input impedance is improved by disabling input chopping (CHOP bit = 0).
(4) V_{IN} = 20mV_{DC}/PGA, see Table 3.
(5) V_{IN} = 31.25 Hz, –0.5 dBFS.
(6) Best-fit method.
(7) FSR: Full-scale range = $\pm V_{REF}/2 \times$ PGA.
(8) Calibration accuracy is on the level of noise reduced by 4 (calibration averages 16 readings).

ELECTRICAL CHARACTERISTICS (continued)

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} [1] = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C[2]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain error[9]		High-resolution mode	–1.5	–1.0	–0.5	–1.5	–1	–0.5	%
		Low-power mode	–1	–0.5	0	–1	–0.48	0	%
Gain error after calibration[8]				0.0002			0.0002		%
DC PERFORMANCE (continued)									
Gain drift		PGA = 1		2			3		ppm/°C
		PGA = 16		9			10		ppm/°C
Gain matching[10]				0.3	0.8			0.8	%
Common-mode rejection		f_{CM} = 60Hz[11]	82	110		127	137		dB
Power-supply rejection	AVDD, AVSS	f_{PS} = 60Hz[11]	80	90		83	97		dB
	DVDD		90	115		111	117		
VOLTAGE REFERENCE INPUTS									
Reference input voltage		(V_{REF} = VREFP – VREFN)	0.5	5	(AVDD – AVSS) + 0.2	0.5		(AVDD – AVSS) + 0.2	V
Negative reference input	VREFN		AVSS – 0.1		VREFP – 0.5	AVSS – 0.1		VREFP – 0.5	V
Positive reference input	VREFP		VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
Reference input impedance		High-resolution mode		85			85		kΩ
		Low-power mode		170			170		kΩ
DIGITAL FILTER RESPONSE									
Passband ripple					±0.003				dB
Passband (–0.01 dB)				0.375 × f_{DATA}					Hz
Bandwidth (–3 dB)				0.413 × f_{DATA}					Hz
High-pass filter corner			0.1		10				Hz
Stop band attenuation[12]			135						dB
Stop band				0.500 × f_{DATA}					Hz
Group delay		Minimum phase filter		$5/f_{DATA}$					s
		Linear phase filter		$31/f_{DATA}$					
Settling time (latency)		Minimum phase filter		$10/f_{DATA}$					s
		Linear phase filter		$62/f_{DATA}$					
DIGITAL INPUT/OUTPUT									
V_{IH}			0.8 × DVDD		DVDD	0.8 X DVDD		DVDD	V
V_{IL}			DGND		0.2 × DVDD	DGND		0.2 × DVDD	V
V_{OH}		I_{OH} = 1mA	0.8 × DVDD			0.8 X DVDD			V
V_{OL}		I_{OL} = 1mA			0.2 × DVDD			0.2 × DVDD	V
Input leakage		0 < $V_{DIGITAL\ IN}$ < DVDD			±10			±10	µA
Clock input	f_{CLK}		1		4.096	1		4.096	MHz
Serial clock rate	f_{SCLK}				$f_{CLK}/2$			$f_{CLK}/2$	MHz

(9) The PGA output impedance and the modulator input impedance results in –1% systematic gain error (high-resolution mode) and –0.5% error (low-power mode).
(10) Gain match relative to PGA = 1.
(11) f_{CM} is the input common-mode frequency. f_{PS} is the power-supply frequency.
(12) Input frequencies in the range of $Nf_{CLK}/512 \pm f_{DATA}/2$ (N = 1, 2, 3...) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120 dB, typ.

ELECTRICAL CHARACTERISTICS (continued)

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} (1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER	CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(2)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
AVSS		–2.6		0	–2.6		0	V
AVDD		AVSS + 4.75		AVSS + 5.25	AVSS + 4.75		AVSS + 5.25	V
DVDD		1.75		3.6	1.75		3.6	V
AVDD, AVSS current	High-resolution mode		4.5	7.2		5.2	10	|mA|
	Low-power mode		3	4.6		3.5	8	|mA|
	Standby mode		1	16.5		122.5	215	|µA|
	Power-down mode		1	16.5		122.5	214	|µA|
DVDD current	All modes		0.6	1.5		1.2	2	mA
	Modulator mode		0.1			1.1		mA
	Standby mode		25	55		90	100	µA
	Power-down mode(13)		1	16.5		86	96	µA
Power dissipation	High-reolution mode		25	38.5		29.7	56.1	mW
	Low-power mode		17	27.5		21.5	46.1	mW
	Standby mode		90	275		909.5	1405	µW
	Power-down mode		10	137.5		896.3	1386.8	µW

(13) CLK input stopped.

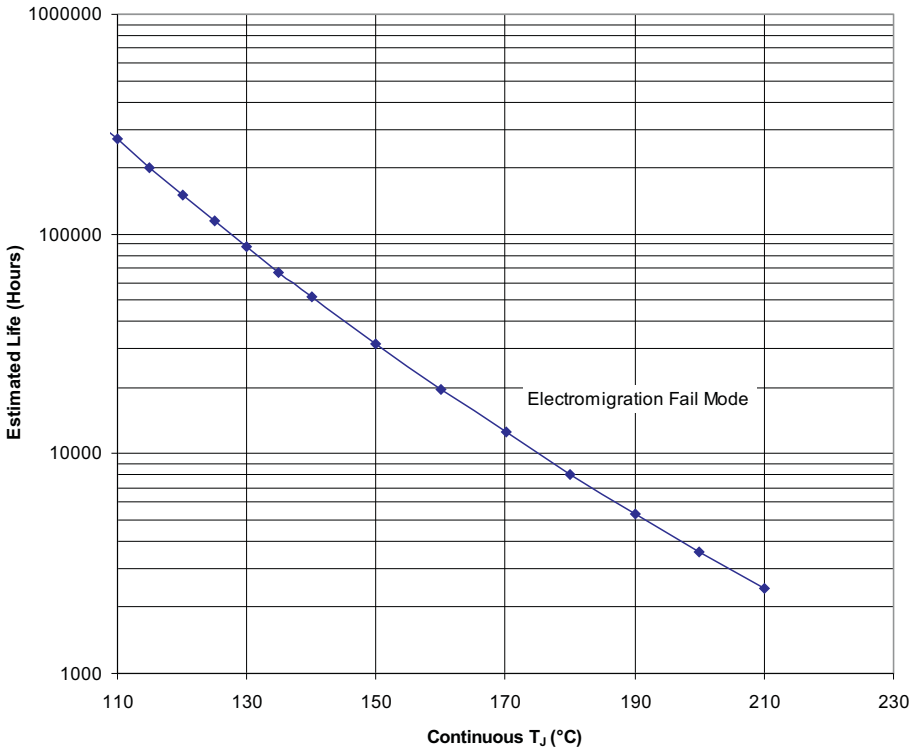
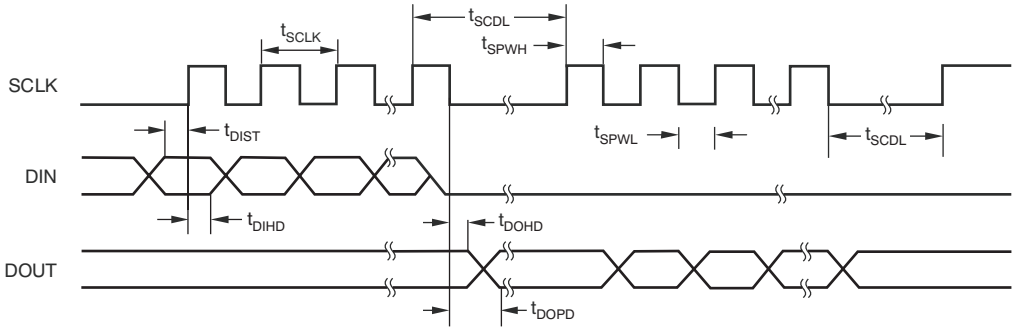


Figure 1. ADS1282SKGD1 Operating Life Derating Chart

TIMING DIAGRAM



TIMING REQUIREMENTS

At T_A = –55°C to 210°C and DVDD = 1.65 V to 3.6 V, unless otherwise noted.

PARAMETER	DESCRIPTION	T_A = –55°C to 125°C		T_A = 210°C		UNITS
		MIN	MAX	MIN	MAX	
t_{SCLK}	SCLK period	2	16	2	16	$1/f_{CLK}$
$t_{SPWH, L}$	SCLK pulse width, high and low(1)	0.8	10	0.8	10	$1/f_{CLK}$
t_{DIST}	DIN valid to SCLK rising edge: setup time	50		50		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	50		50		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: propagation delay(2)		100		100	ns
t_{DOHD}	SCLK falling edge to DOUT invalid: hold time	0		0		ns
t_{SCDL}	Final SCLK rising edge of command to first SCLK rising edge for register read/write data	24		24		$1/f_{CLK}$

(1) Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the serial interface.
(2) Load on DOUT = 20 pF || 100 kΩ.

TYPICAL CHARACTERISTICS

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

OUTPUT SPECTRUM

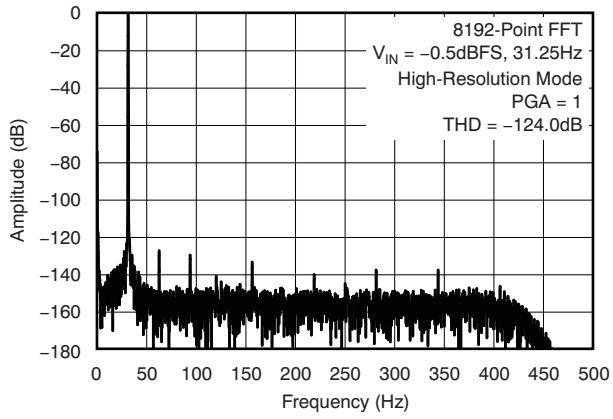


Figure 2.

OUTPUT SPECTRUM

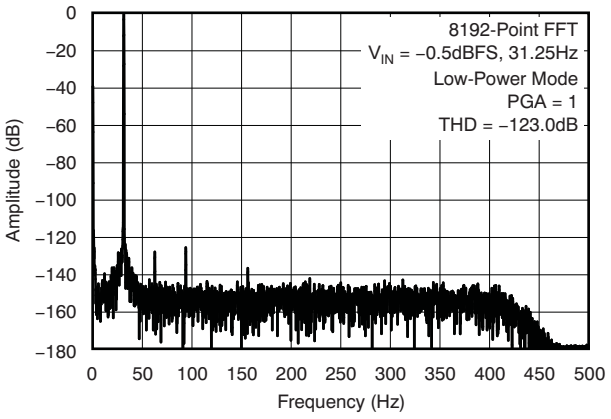


Figure 3.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

OUTPUT SPECTRUM

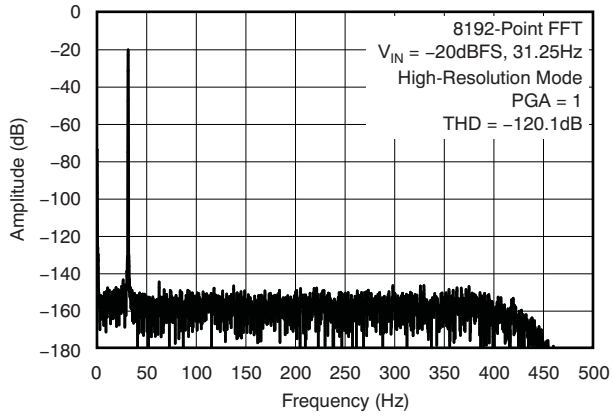


Figure 4.

OUTPUT SPECTRUM

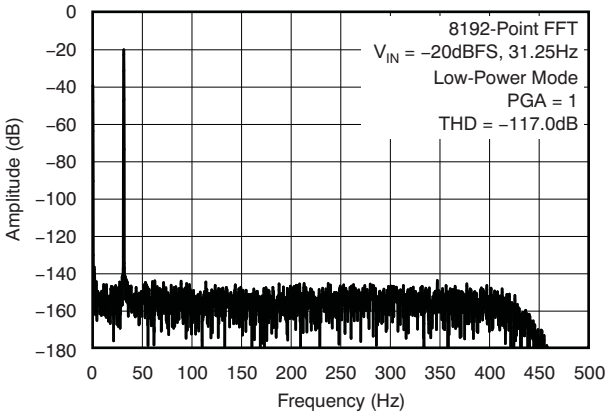


Figure 5.

OUTPUT SPECTRUM

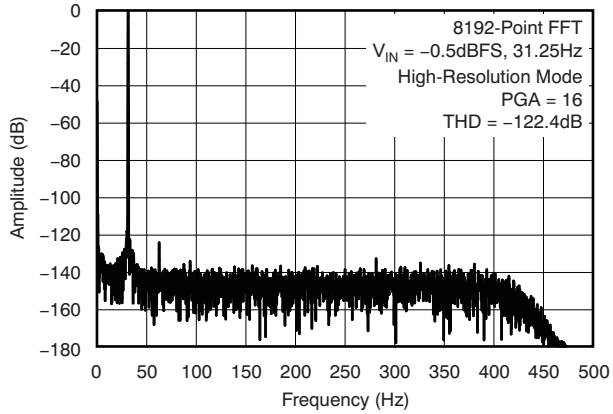


Figure 6.

OUTPUT SPECTRUM

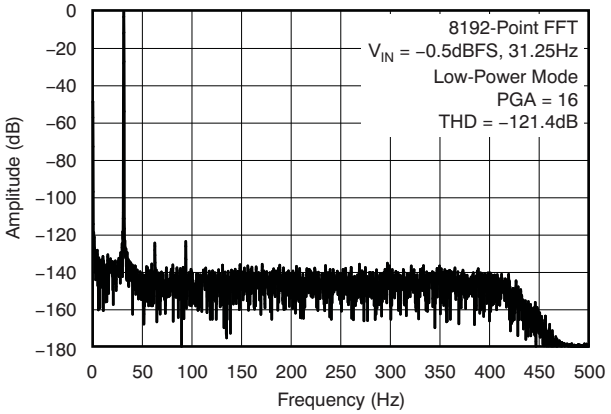


Figure 7.

OUTPUT SPECTRUM

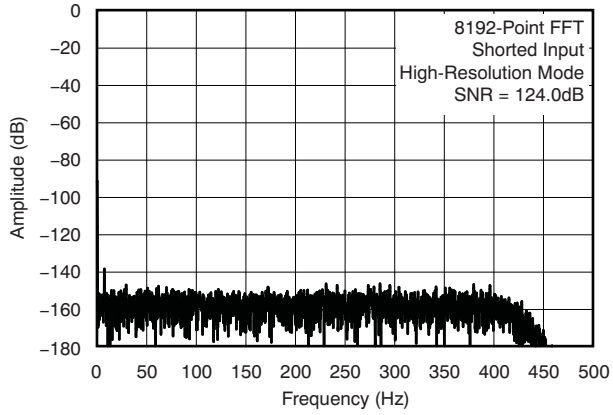


Figure 8.

OUTPUT SPECTRUM

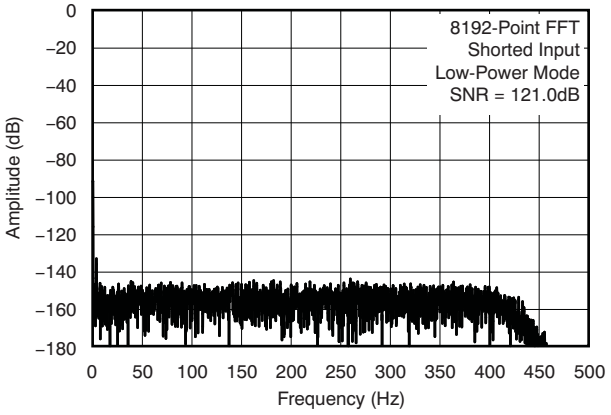


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

OUTPUT SPECTRUM

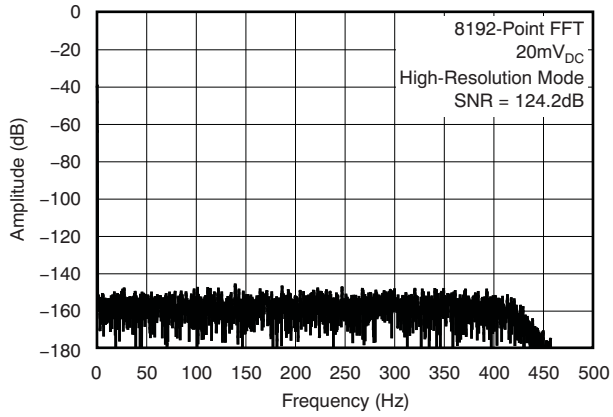


Figure 10.

OUTPUT SPECTRUM

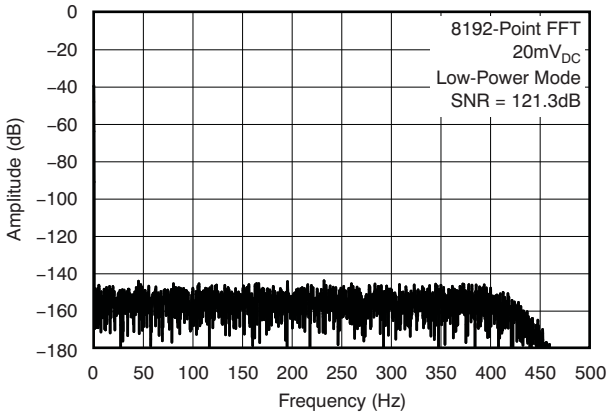


Figure 11.

THD vs INPUT FREQUENCY

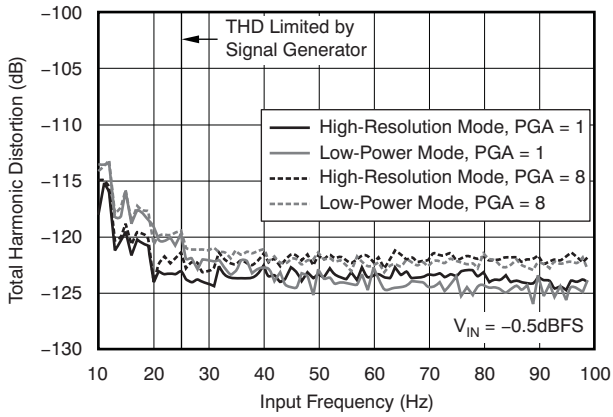


Figure 12.

SNR (1000 SPS) vs TEMPERATURE

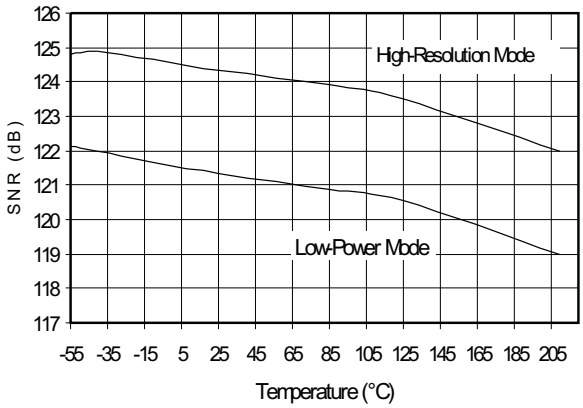


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

THD (G = 8) vs TEMPERATURE

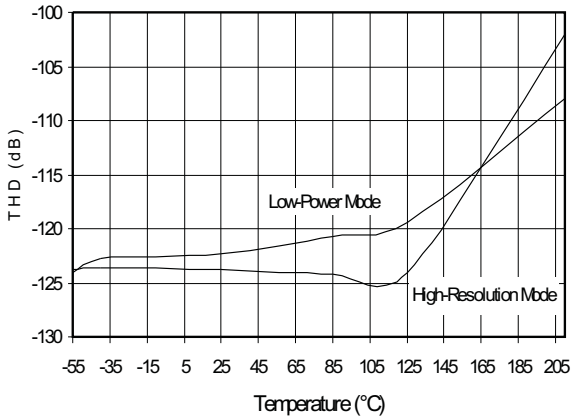


Figure 14.

SNR vs REFERENCE VOLTAGE

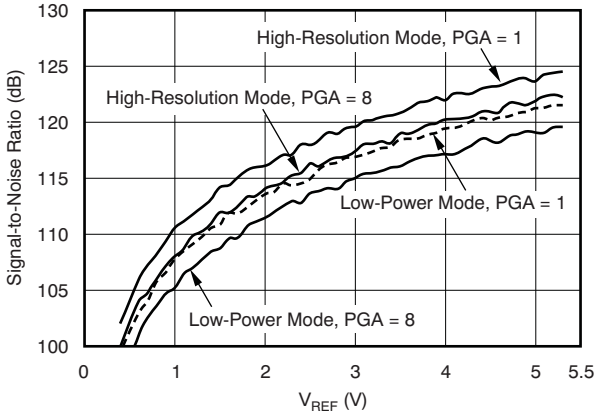


Figure 15.

THD vs REFERENCE VOLTAGE

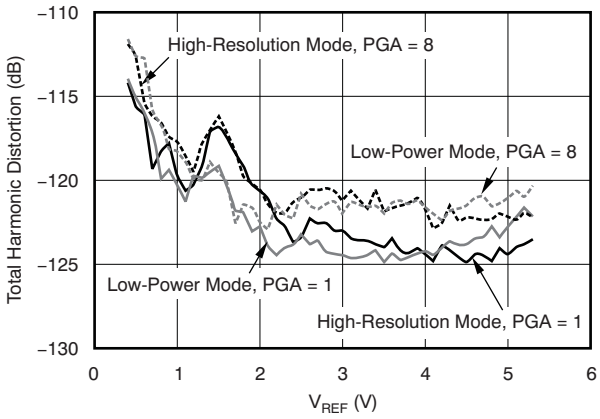


Figure 16.

SNR vs CLOCK FREQUENCY

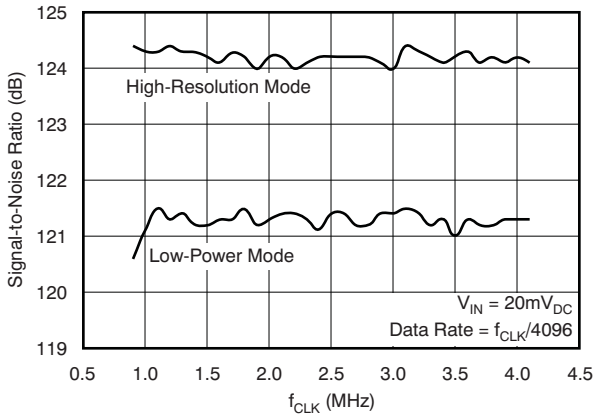


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

THD vs CLOCK FREQUENCY

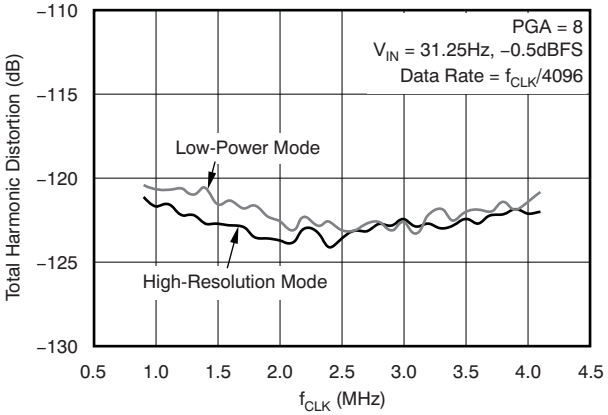


Figure 18.

CMR vs INPUT FREQUENCY

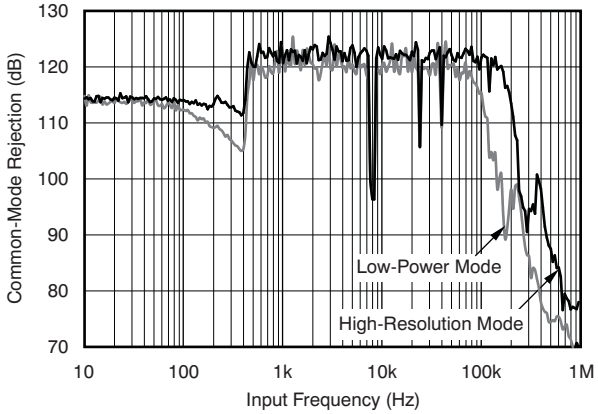


Figure 19.

POWER-SUPPLY REJECTION vs FREQUENCY

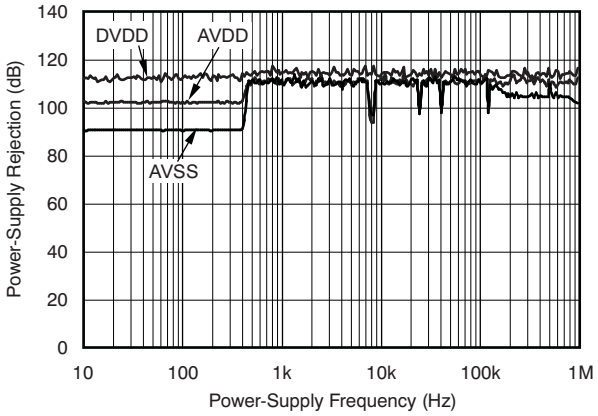


Figure 20.

INL vs INPUT AMPLITUDE

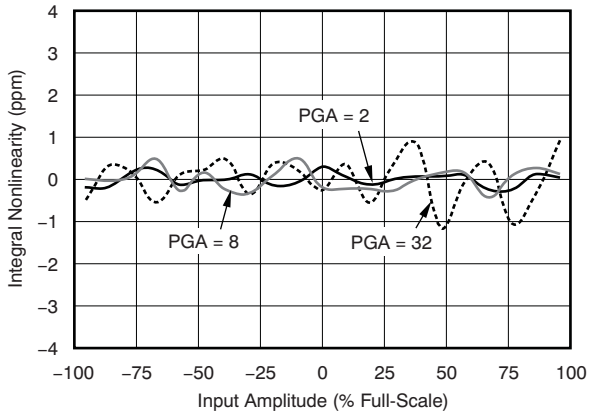


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

INL vs TEMPERATURE

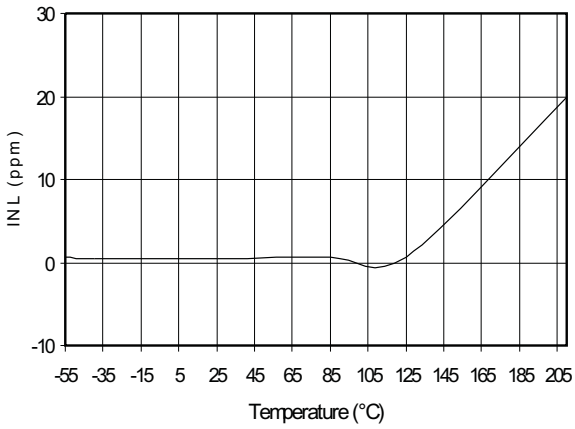


Figure 22.

CROSSTALK OUTPUT SPECTRUM

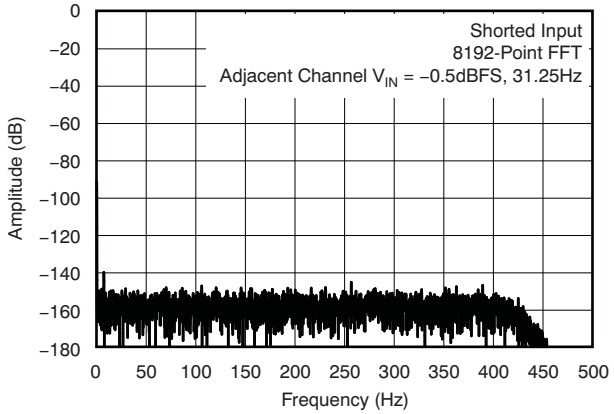


Figure 23.

POWER vs TEMPERATURE

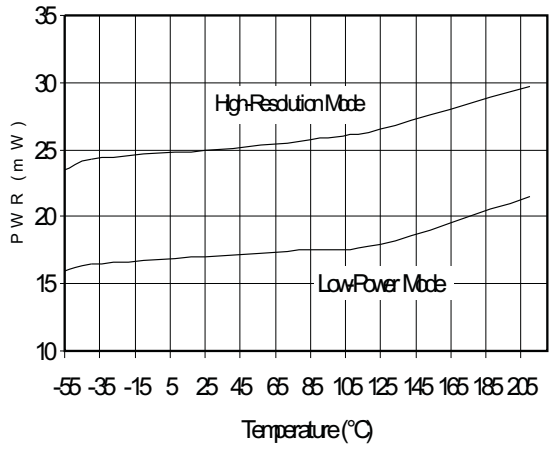


Figure 24.

POWER vs CLOCK FREQUENCY

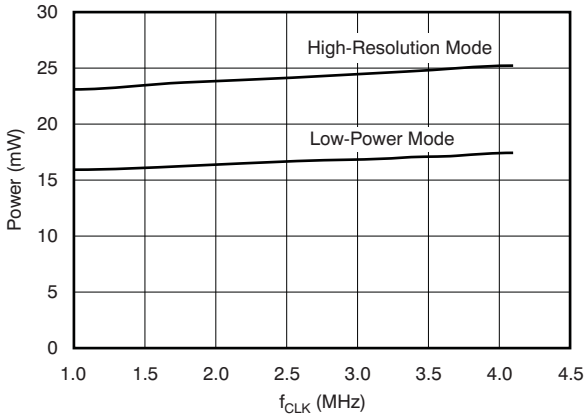


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, High-Resolution Mode, and f_{DATA} = 1000 SPS, unless otherwise noted.

OFFSET HISTOGRAM

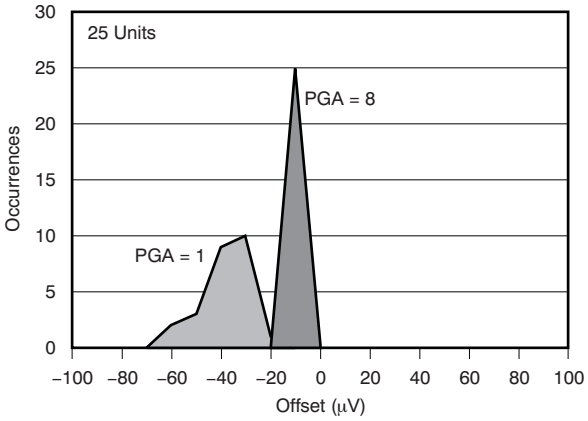


Figure 26.

GAIN ERROR HISTOGRAM

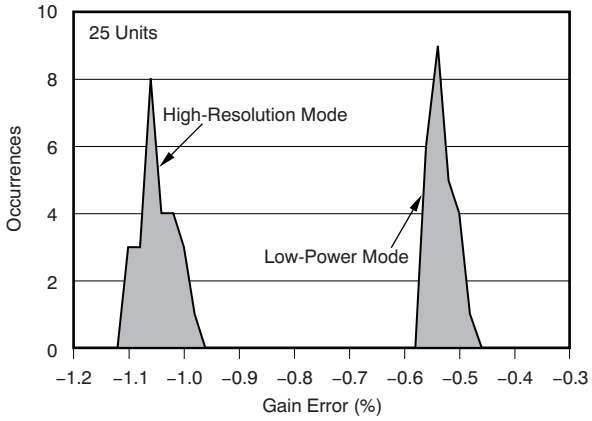


Figure 27.

OFFSET DRIFT HISTOGRAM

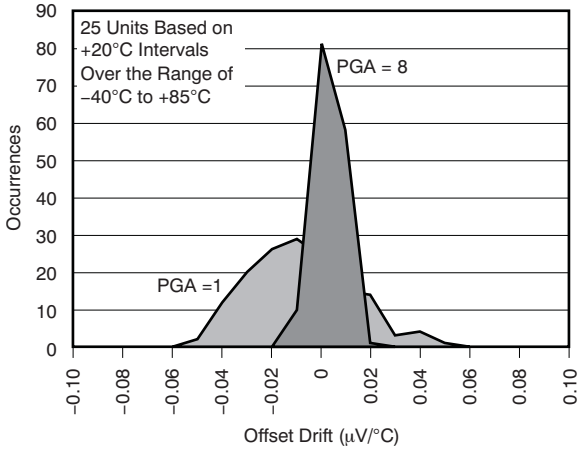


Figure 28.

GAIN DRIFT HISTOGRAM

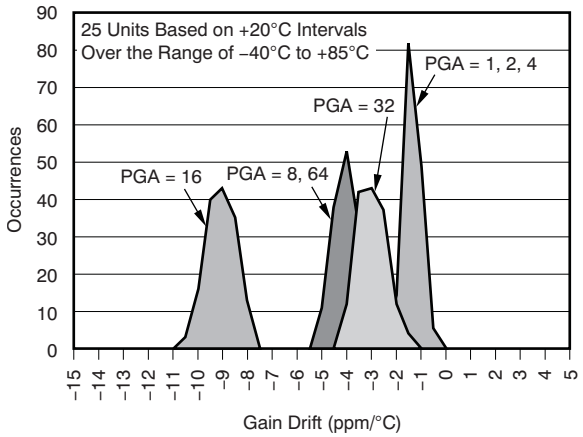


Figure 29.

GAIN MATCH HISTOGRAM

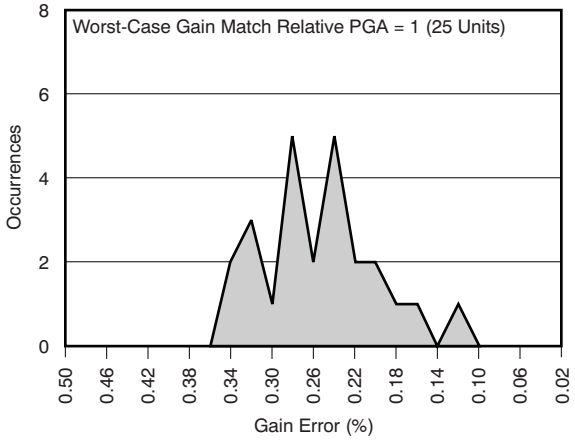


Figure 30.

OVERVIEW

The ADS1282 is a high-performance analog-to-digital converter (ADC) intended for energy exploration, seismic monitoring, chomatography, and other exacting applications. The converter provides 24- or 32-bit output data in data rates from 250 SPS to 4000 SPS. Figure 31 shows the block diagram of the ADS1282.

The two-channel input MUX allows five configurations: Input 1; Input 2; Input 1 and Input 2 shorted together; shorted with 400-Ω test; and common-mode test. The input MUX is followed by a continuous time PGA, featuring very low noise of 5nV/√Hz. The PGA is controlled by register settings, allowing gains of 1 to 64.

The inherently-stable, fourth-order, delta-sigma modulator measures the differential input signal V_{IN} = (AINP – AINN) PGA against the differential reference V_{REF} = (VREFP – VREFN). A digital output (MFLAG) indicates that the modulator is in overload as a result of an overdrive condition. The modulator output is available directly on the MCLK, M0, and M1 output pins. The modulator connects to an on-chip digital filter that provides the output code readings.

The digital filter consists of a variable decimation rate, fifth-order sinc filter followed by a variable phase, decimate-by-32, finite-impulse response (FIR) low-pass filter with programmable phase, and then by an adjustable high-pass filter for dc removal of the output reading. The output of the digital filter can be taken from the sinc, the FIR low-pass, or the infinite impulse response (IIR) high-pass sections.

Gain and offset registers scale the digital filter output to produce the final code value. The scaling feature can be used for calibration and sensor gain matching. The output data word is provided as either a 24-bit word or a full 32-bit word, allowing complete utilization of the inherently high resolution.

The SYNC input resets the operation of both the digital filter and the modulator, allowing synchronization conversions of multiple ADS1282 devices to an external event. The SYNC input supports a continuously-toggled input mode that accepts an external data frame clock locked to the conversion rate.

The $\overline{\text{RESET}}$ input resets the register settings and also restarts the conversion process. The $\overline{\text{PWDN}}$ input sets the device into a micro-power state. Note that register settings are not retained in $\overline{\text{PWDN}}$ mode. Use the STANDBY command in its place if it is desired to retain register settings (the quiescent current in the Standby mode is slightly higher).

Noise-immune Schmitt-trigger and clock-qualified inputs ($\overline{\text{RESET}}$ and SYNC) provide increased reliability in high-noise environments. The serial interface is used to read conversion data, in addition to reading from and writing to the configuration registers.

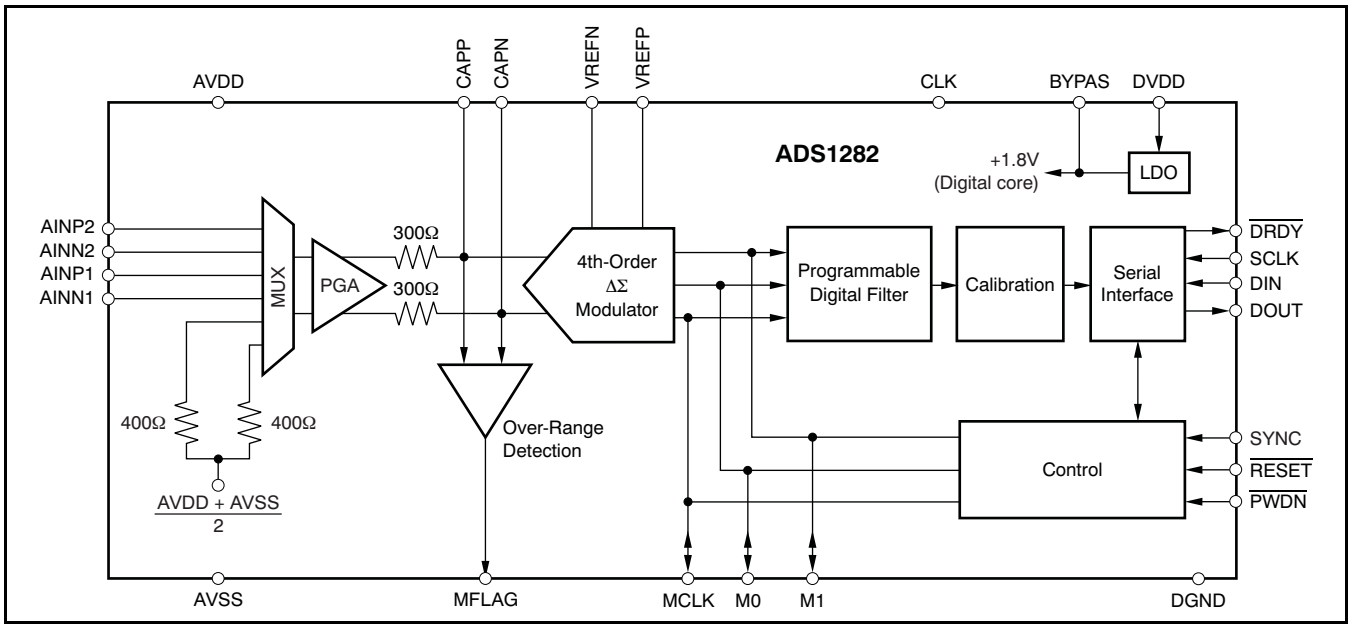


Figure 31. ADS1282 Block Diagram

The device features unipolar and bipolar analog power supplies (AVDD and AVSS, respectively) for input range flexibility and a digital supply accepting 1.8 V to 3.3 V. The analog supplies may be set to 5 V to accept unipolar signals (with input offset) or set lower in the range of ±2.5 V to accept true bipolar input signals (ground referenced).

An internal sub-regulator is used to supply the digital core from DVDD. The BYPAS pin (pin 28) is the sub-regulator output and requires a 1-µF capacitor for noise reduction. BYPAS should not be used to drive external circuitry.

NOISE PERFORMANCE

The ADS1282 offers outstanding noise performance (SNR). SNR depends on the data rate, the PGA setting, and the mode (high-resolution or low-power). As the bandwidth is reduced by decreasing the data rate, the SNR improves correspondingly. Similarly, as the PGA gain is increased, the SNR decreases. In low-power mode, the SNR decreases 3 dB for each setting. Table 3 summarizes the noise performance versus data rate, PGA setting, and mode.

INPUT-REFERRED NOISE

The input-referred noise is related to SNR by Equation 1:

$$SNR = 20\log \frac{FSR_{RMS}}{N_{RMS}} \quad (1)$$

where:

FSR_{RMS} = Full-scale range RMS = $V_{REF}/2 \times \sqrt{2} \times PGA$

N_{RMS} = Noise RMS (input-referred)

IDLE TONES

The ADS1282 modulator incorporates an internal dither signal that randomizes the idle tone energy. Low-level idle tones may still be present, typically –137 dB below full-scale. The low-level idle tones can be shifted out of the passband with an external offset = 20mV/PGA. See the *Application Information* section for the recommended offset circuit.

OPERATING MODE

For applications where minimal power consumption is important, the low-power mode can be selected (register bit MODE = 0). In low-power mode, the power is reduced to 17 mW (from 25 mW) and SNR decreases an average of 3 dB. The default mode is high-resolution.

Table 3. Signal-to-Noise Ratio (dB)(1)

DATA RATE (SPS)	PGA (High-Resolution Mode)							PGA (Low-Power Mode)						
	1	2	4	8	16	32	64	1	2	4	8	16	32	64
250	130	130	129	128	125	119	114	127	127	126	125	122	116	111
500	127	127	126	125	122	116	111	124	124	123	122	119	113	108
1000	124	124	123	122	119	113	108	121	121	120	119	116	110	105
2000	121	121	120	119	116	111	106	118	118	117	116	113	108	103
4000	118	118	117	116	113	108	103	115	115	114	113	110	105	100

(1) $V_{IN} = 20mV_{DC}/PGA$.

ANALOG INPUTS AND MULTIPLEXER

A diagram of the input multiplexer is shown in Figure 32.

ESD diodes protect the multiplexer inputs. If either input is taken below AVSS – 0.3 V or above AVDD + 0.3 V, the ESD protection diodes may turn on. If these conditions are possible, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Also, overdriving one unused input may affect the conversions of the other input. If overdriven inputs are possible, it is recommended to clamp the signal with external Schottky diodes.

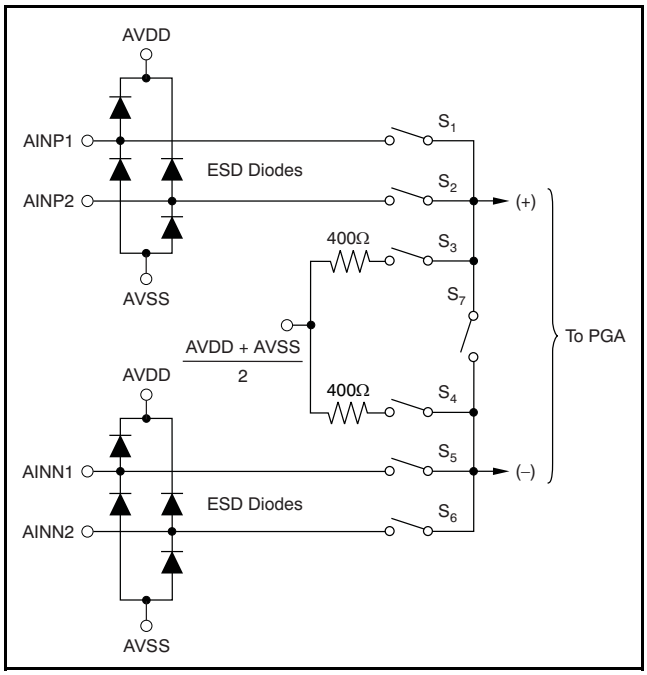


Figure 32. Analog Inputs and Multiplexer

The specified input operating range of the PGA is shown in Equation 2:

$$AVSS + 0.7V < (AINN \text{ or } AINP) < AVDD - 1.25V \quad (2)$$

Absolute input levels (input signal level and common-mode level) should be maintained within these limits for best operation.

The multiplexer connects one of the two external differential inputs to the preamplifier inputs, in addition to internal connections for various self-test modes. Table 4 summarizes the multiplexer configurations for Figure 32.

Table 4. Multiplexer Modes

MUX[2:0]	SWITCHES	DESCRIPTION
000	S_1, S_5	AINP1 and AINN1 connected to preamplifer
001	S_2, S_6	AINP2 and AINN2 connected to preamplifier
010	S_3, S_4	Preamplifier inputs shorted together through 400Ω internal resistors
011	S_1, S_5, S_2, S_6	AINP1, AINN1 and AINP2, AINN2 connected together and to the preamplifier
100	S_6, S_7	External short, preamplifier inputs shorted to AINN2 (common-mode test)

The typical on-resistance (R_{ON}) of the multiplexer switch is 30 Ω. When the multiplexer is used to drive an external load on one input by a signal generator on the other input, on-resistance and on-resistance amplitude dependency can lead to measurement errors. Figure 33 shows THD versus load resistance and amplitude. Note that THD improves with high-impedance loads and with lower amplitude drive signals. The data are measured with the circuit from Figure 34 with MUX[2:0] = 011.

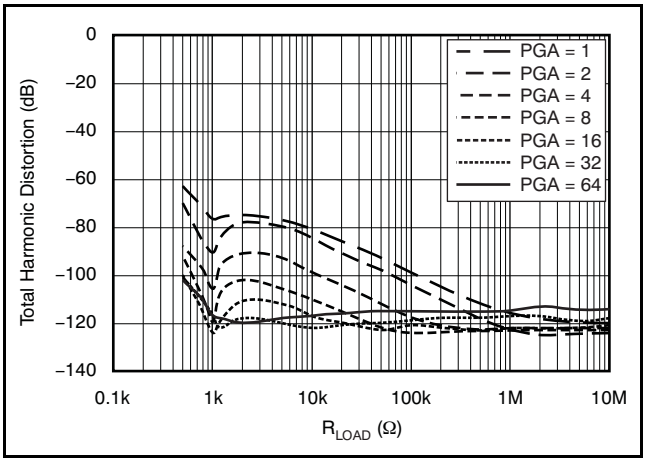


Figure 33. THD versus External Load and Signal Magnitude (PGA) (see Figure 34)

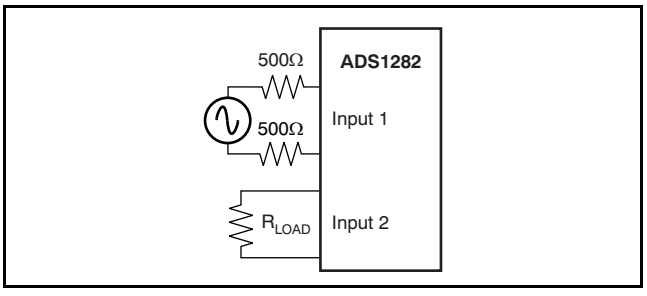


Figure 34. Driving an External Load Through the MUX

PGA (Programmable Gain Amplifier)

The PGA of the ADS1282 is a low-noise, continuous-time, differential-in/differential-out CMOS amplifier. The gain is programmable from 1 to 64, set by register bits, PGA[2:0]. The PGA differentially drives the modulator through 300-Ω internal resistors. A COG capacitor (10nF typical) must be connected to CAPP and CAPN to filter modulator sampling glitches. The external capacitor also serves as an anti-alias filter. The corner frequency is given in Equation 3:

$$f_P = \frac{1}{6.3 \times 600 \times C} \quad (3)$$

Referring to Figure 35, amplifiers A_1 and A_2 are chopped to remove the offset, offset drift, and the 1/f noise. Chopping moves the effects to $f_{CLK}/128$ (8 kHz), which is safely out of the passband. Chopping can be disabled by setting the CHOP register bit = 0. With chopping disabled, the impedance of the PGA increases substantially (>> 1 GΩ). As shown in Figure 36, chopping maintains flat noise density; if chopping is disabled, however, it results in a rising 1/f noise profile.

The PGA has programmable gains from 1 to 64. Table 5 shows the register bit setting for the PGA and resulting full-scale differential range.

The specified output operating range of the PGA is shown in Equation 4:

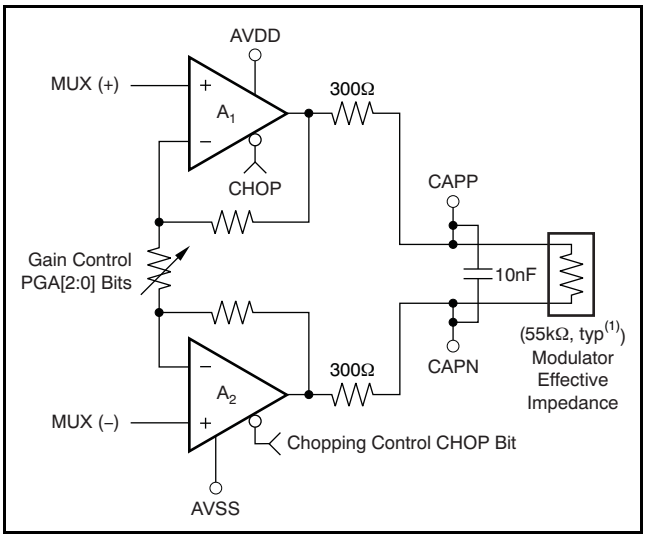
$$AVSS + 0.4V < (CAPN \text{ or } CAPP) < AVDD - 0.4V \quad (4)$$

PGA output levels (signal plus common-mode) should be maintained within these limits for best operation.

Table 5. PGA Gain Settings

PGA[2:0]	GAIN	DIFFERENTIAL INPUT RANGE (V)(1)
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.312
100	16	±0.156
101	32	±0.078
110	64	±0.039

(1) V_{REF} = 5 V.



(1) Low-power mode = 110 kΩ.

Figure 35. PGA Block Diagram

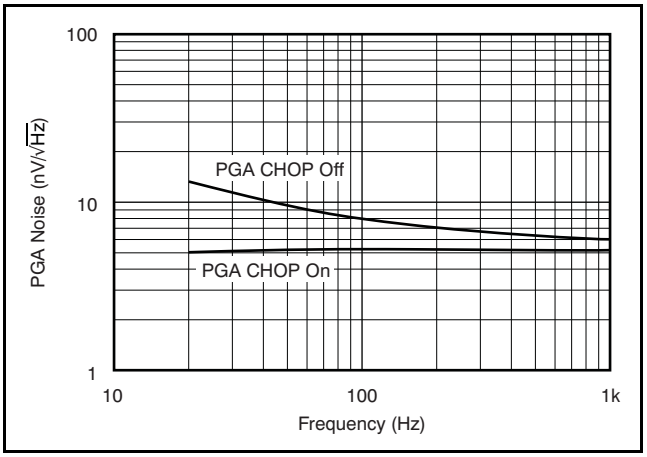


Figure 36. PGA Noise

ADC

The ADC block of the ADS1282 is composed of two sections: a high-accuracy modulator and a programmable digital filter.

MODULATOR

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as Figure 37 shows. It shifts the quantization noise to a higher frequency (out of the passband) where digital filtering can easily remove it. The modulator can be filtered either by the on-chip digital filter or by use of post-processing filters.

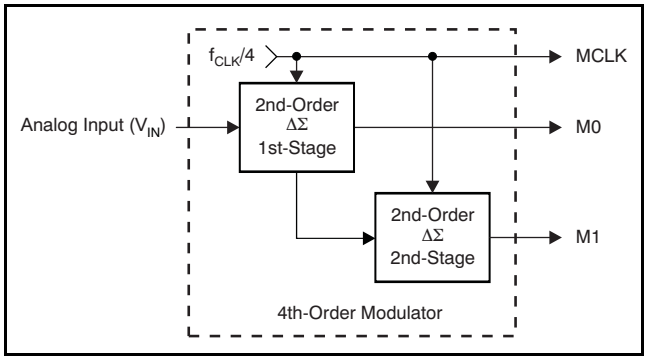


Figure 37. Fourth-Order Modulator

The modulator first stage converts the analog input voltage into a pulse-code modulated (PCM) stream. When the level of differential analog input (AINP – AINN) is near one-half the level of the reference voltage 1/2 × (VREFP – VREFN), the '1' density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM '0' and '1' densities are nearly equal. At the two extremes of the analog input levels (+FS and –FS), the '1' density of the PCM streams is approximately +90% and +10%, respectively.

The modulator second stage produces a '1' density data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are then combined before the digital filter stage, as shown in Equation 5.

$$Y[n] = 3M0[n-2] - 6M0[n-3] + 4M0[n-4] + 9(M1[n] - 2M1[n-1] + M1[n-2]) \quad (5)$$

M0[n] represents the most recent first-stage output while M0[n – 1] is the previous first-stage output. When the modulator output is enabled, the digital filter shuts down to save power.

The modulator is optimized for input signals within a 4-kHz passband. As Figure 38 shows, the noise shaping of the modulator results in a sharp increase in noise above 6 kHz. The modulator has a chopped input structure that further reduces noise within the passband. The noise moves out of the passband and appears at the chopping frequency (f_{CLK}/512 = 8 kHz). The component at 5.8 kHz is the tone frequency, shifted out of band by an external 20 mV/PGA offset. The frequency of the tone is proportional to the applied dc input and is given by PGA × V_{IN}/0.003 (in kHz).

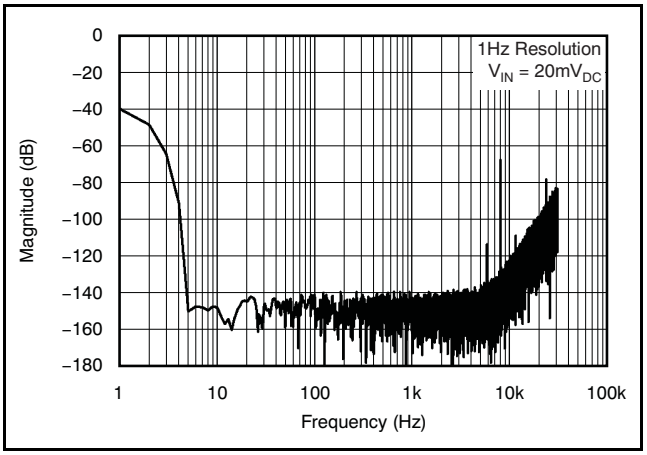


Figure 38. Modulator Output Spectrum

MODULATOR OVER-RANGE

The ADS1282 modulator is inherently stable, and therefore, has predictable recovery behavior resulting from an input overdrive condition. The modulator does not exhibit self-resetting behavior, which often results in an unstable output data stream.

The ADS1282 modulator outputs a 1s density data stream at 90% duty cycle with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but below 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input returns to the normal range from a long duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (31 readings for linear phase FIR). 31 additional readings (62 total) are required for completely settled data.

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle (that is, all 1 s, all 0 s, or ±110% FSR), the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small duration overdrive may not always clip the output code. When

the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires an additional 62 conversions for fully settled data (linear phase FIR).

In the extreme case of over-range, either input is overdriven, exceeding the voltage of either analog supply voltage plus an internal ESD diode drop. The internal diodes begin to conduct and the signal on the input is clipped. When the input overdrive is removed, the diodes recover quickly. Keep in mind that the input current must be limited to 100-mA peak or 10 mA continuous if an overvoltage condition is possible.

MODULATOR INPUT IMPEDANCE

The modulator samples the buffered input voltage with an internal capacitor to perform conversions. The charging of the input sampling capacitor draws a transient current from the PGA output. The average value of the current can be used to calculate an effective input impedance of $R_{EFF} = 1/(f_{MOD} \times C_S)$.

Where:

f_{MOD} = Modulator sample frequency
(High-resolution mode = CLK/4)
(Low-power mode = CLK/8)

C_S = Input sampling capacitor (17pF, typ)

The resulting modulator input impedance for CLK = 4.096 MHz is 55 kΩ (110 kΩ low-power mode). The modulator input impedance and the PGA output resistors result in a systematic gain error of –1% (–0.5% in low-power mode). C_S can vary ±20% or more over production lots, affecting the gain error.

MODULATOR OVER-RANGE DETECTION (MFLAG)

The ADS1282 has a fast-responding over-range detection that indicates when the differential input exceeds approximately 100% over-range. The threshold tolerance is ±2.5%.The MFLAG output asserts high when in an over-range condition. As Figure 39 and Figure 40 illustrate, the absolute differential input is compared to 100% of range. The output of the comparator is sampled at the rate of $f_{MOD}/2$, yielding the MFLAG output. The minimum MFLAG pulse width is $f_{MOD}/2$.

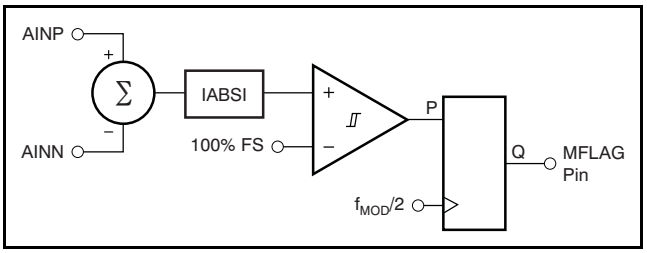


Figure 39. Modulator Over-Range Block Diagram

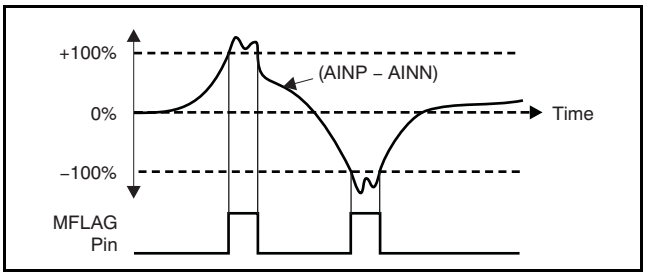


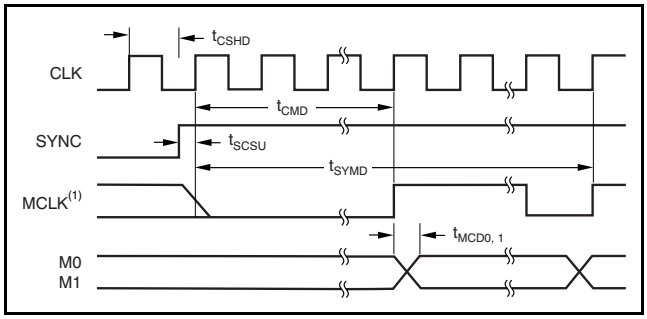
Figure 40. Modulator Over-Range Flag Operation

MODULATOR OUTPUT MODE

The modulator digital stream output is accessible directly, bypassing and disabling the internal digital filter. The modulator output mode is activated by setting the CONFIG0 register bits FILTR[1:0] = 00. Pins M0 and M1 then become the modulator data outputs and the MCLK becomes the modulator clock output. When not in the modulator mode, these pins are inputs and must be tied.

The modulator output is composed of three signals: one output for the modulator clock (MCLK) and two outputs for the modulator data (M0 and M1). The modulator clock output rate is f_{MOD} (f_{CLK}/4 for high-resolution mode, f_{CLK}/8 for low-power mode). The SYNC input resets the MCLK phase, as shown in Figure 41. The SYNC input is latched on the rising edge of CLK. The MCLK resets and the next rising edge of MCLK occurs five CLK periods later.

The modulator output data are two bits wide, which must be merged together before being filtered. Use the time domain equation of Equation 5 to merge the data outputs.



(1) High-resolution mode: MCLK = f_{CLK}/4; low-power mode: MCLK = f_{CLK}/8.

Figure 41. Modulator Mode Timing

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1282 is the differential voltage between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry of the reference inputs shown in Figure 42. The average load presented by the switched capacitor reference input can be modeled with an effective differential impedance of $R_{EFF} = t_{SAMPLE}/C_{IN}$ ($t_{SAMPLE} = 1/f_{MOD}$). Note that the effective impedance of the reference inputs loads the external reference.

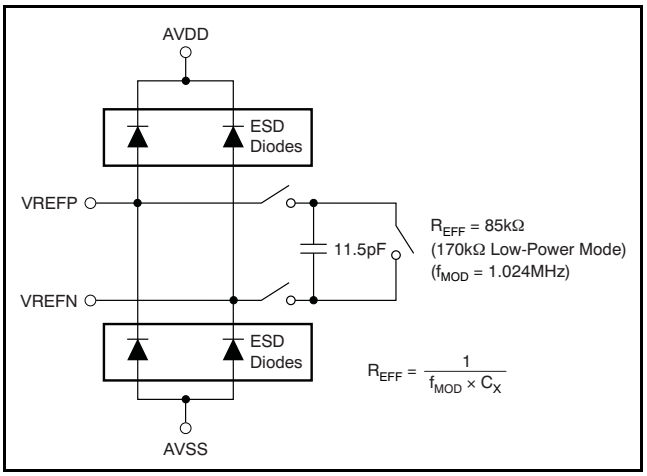


Figure 42. Simplified Reference Input Circuit

Table 6. Modulator Output Timing for Figure 41

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{MCD0, 1}$	MCLK rising edge to M0, M1 valid propagation delay(1)			100	ns
t_{CMD}	CLK rising edge (after SYNC rising edge) to MCLK rising edge reset time		5		$1/f_{CLK}$
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10			ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10			ns
t_{SYMD}	SYNC to stable bit stream			16	$1/f_{MOD}$

(1) Load on M0 and M1 = 20 pF || 100 kΩ.

The ADS1282 reference inputs are protected by ESD diodes. In order to prevent these diodes from turning on, the voltage on either input must stay within the range shown in Equation 6:

$$AVSS - 300mV < (VREFP \text{ or } VREFN) < AVDD + 300mV \quad (6)$$

Note that the minimum valid input for VREFN is AVSS – 0.1 V and maximum valid input for VREFP is AVDD + 0.1 V.

A high-quality +5 V reference voltage is necessary for achieving the best performance from the ADS1282. Noise and drift on the reference degrade overall system performance, and it is critical that special care be given to the circuitry generating the reference voltages in order to achieve full performance. See the *Application Information* section for reference recommendations.

DIGITAL FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter is comprised of three cascaded filter stages: a variable-decimation, fifth-order sinc filter; a fixed-decimation FIR, low-pass filter (LPF) with selectable phase; and a programmable, first-order, high-pass filter (HPF), as shown in Figure 43.

The output can be taken from one of the three filter blocks, as Figure 43 shows. To implement the digital filter completely off-chip, select the filter bypass setting (modulator output). For partial filtering by the ADS1282, select the sinc filter output. For complete on-chip filtering, activate both the sinc and FIR stages. The HPF can then be included to remove dc and low frequencies from the data. Table 7 shows the filter options.

Table 7. Digital Filter Selection

FILTR[1:0] BITS	DIGITAL FILTERS SELECTED
00	Bypass; modulator output mode
01	Sinc
10	Sinc + FIR
11	Sinc + FIR + HPF (low-pass and high-pass)

Sinc Filter Stage (sinx/x)

The sinc filter is a variable decimation rate, fifth-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} ($f_{CLK}/4$). The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter; it is set by the DR[2:0] register bits, as shown in Table 8.

Equation 7 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5 \quad (7)$$

Table 8. Sinc Filter Data Rates (CLK = 4.096MHz)

DR[2:0] REGISTER	DECIMATION RATIO (N)	SINC DATA RATE (SPS)
000	128	8,000
001	64	16,000
010	32	32,000
011	16	64,000
100	8	128,000

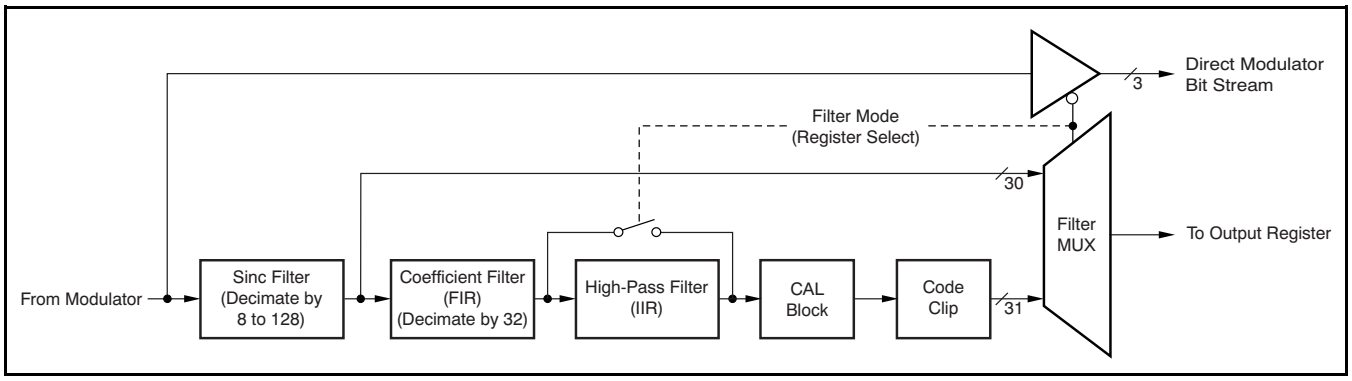


Figure 43. Digital Filter and Output Code Processing

Equation 8 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \quad (8)$$

where:

N = decimation ratio (see Table 8)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. Figure 44 shows the frequency response of the sinc filter and Figure 45 shows the roll-off of the sinc filter.

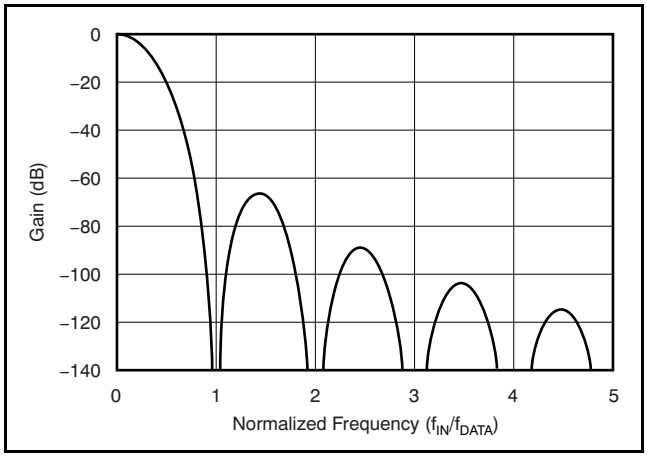


Figure 44. Sinc Filter Frequency Response

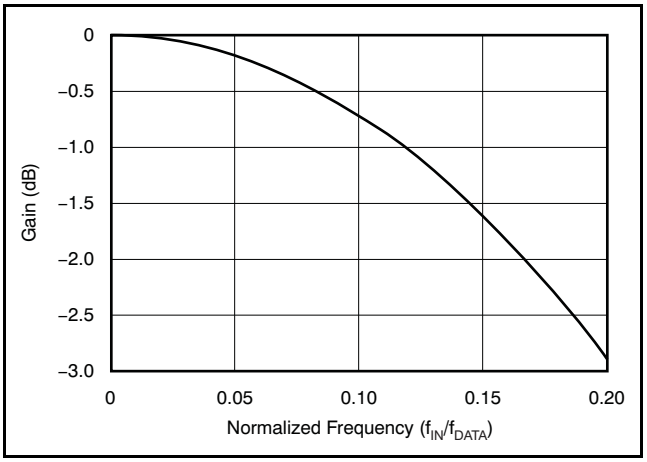


Figure 45. Sinc Filter Roll-Off

FIR Stage

The second stage of the ADS1282 digital filter is an FIR low-pass filter. Data are supplied to this stage from the sinc filter. The FIR stage is segmented into four sub-stages, as shown in Figure 46. The first two sub-stages are half-band filters with decimation ratios of 2. The third sub-stage decimates by 4 and the fourth sub-stage decimates by 2. The overall decimation of the FIR stage is 32. Note that two coefficient sets are used for the third and fourth sections, depending on the phase selection. Table 25 (in the Appendix section at the end of this document) lists the FIR stage coefficients. Table 9 lists the data rates and overall decimation ratio of the FIR stage.

Table 9. FIR Filter Data Rates

DR[2:0] REGISTER	DECIMATION RATIO (N)	FIR DATA RATE (SPS)
000	4096	250
001	2048	500
010	1024	1000
011	512	2000
100	256	4000

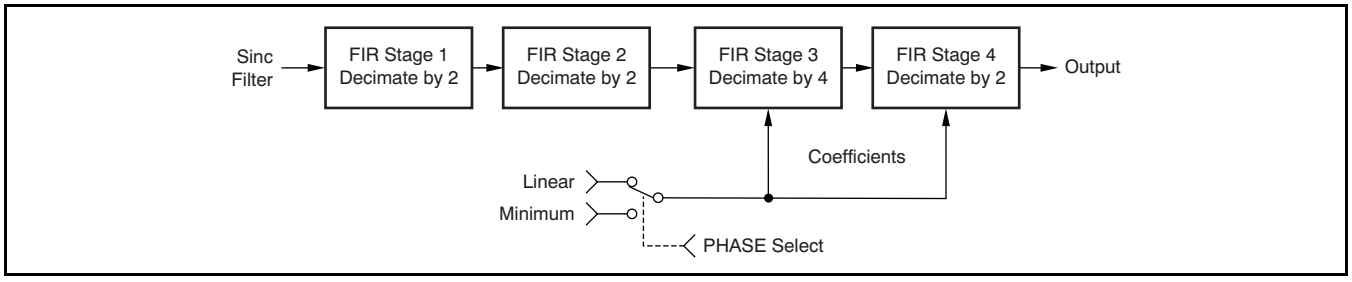


Figure 46. FIR Filter Sub-Stages

As shown in Figure 47, the FIR frequency response provides a flat passband to 0.375 of the data rate (±0.003 dB passband ripple). Figure 48 shows the transition from passband to stop band.

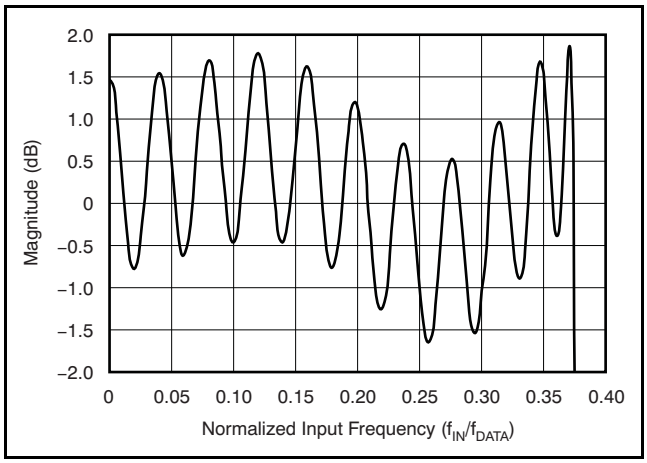


Figure 47. FIR Passband Magnitude Response (f_{DATA} = 500Hz)

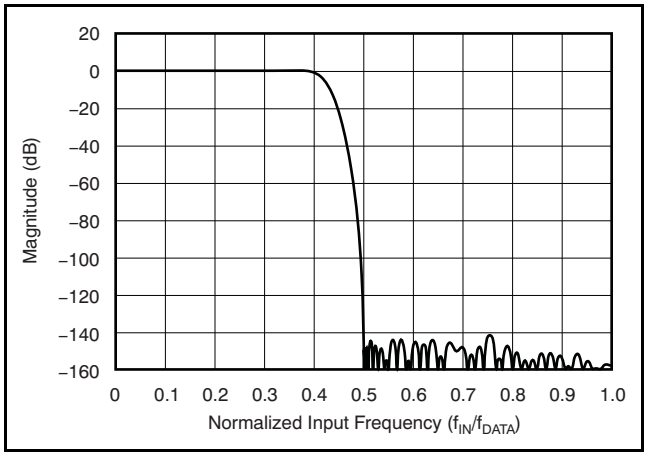


Figure 48. FIR Transition Band Magnitude Response

Although not shown in Figure 48, the passband response repeats at multiples of the modulator frequency ($Nf_{MOD} – f_0$ and $Nf_{MOD} + f_0$, where N = 1, 2, etc. and f_0 = passband). These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the passband and cause errors. A low-pass signal filter reduces the effect of aliasing. Often, the RC low-pass filter provided by the PGA output resistors and the external capacitor connected to CAPP and CAPN provides sufficient signal attenuation.

GROUP DELAY AND STEP RESPONSE

The FIR block is implemented as a multi-stage FIR structure with selectable linear or minimum phase response. The passband, transition band, and stop band responses of the filters are nearly identical but differ in the respective phase responses.

Linear Phase Response

Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Linear phase filters have the property that the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of the signal nature. This filter behavior results in essentially zero phase error when analyzing multi-tone signals. However, the group delay and settling time of the linear phase filter are somewhat larger than the minimum phase filter, as shown in Figure 49.

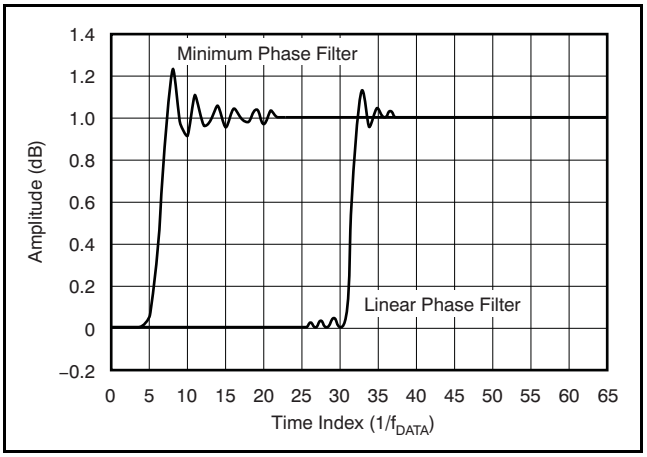


Figure 49. FIR Step Response

Minimum Phase Response

The minimum phase filter provides a short delay from the arrival of an input signal to the output, but the relationship (phase) is not constant versus frequency, as shown in Figure 50. The filter phase is selected by the PHS bit, as Table 10 shows.

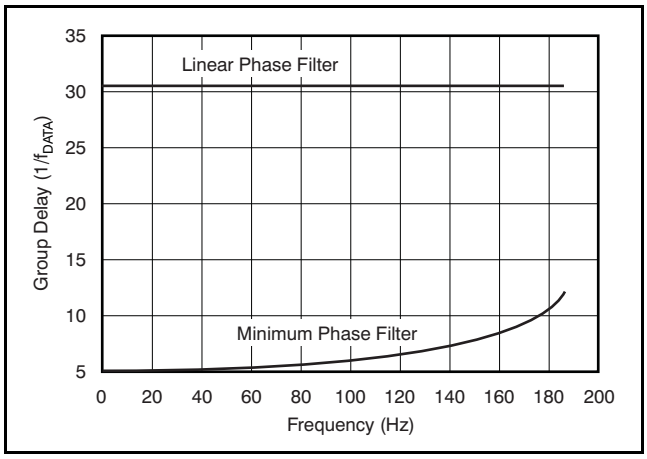


Figure 50. FIR Group Delay (f_{DATA} = 500Hz)

Table 10. FIR Phase Selection

PHS BIT	FILTER PHASE
0	Linear
1	Minimum

HPF Stage

The last stage of the ADS1282 filter block is a first-order HPF implemented as an IIR structure. This filter stage blocks dc signals and rolls off low-frequency components below the cut-off frequency. The transfer function for the filter is shown in Equation 9:

$$HPF(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \quad (9)$$

where *b* is calculated as shown in Equation 10:

$$b = \frac{\left(1 + (1 - a)^2\right)^2}{2} \quad (10)$$

The high-pass corner frequency is programmed by registers HPF[1:0], in hexadecimal. Equation 11 is used to set the high-pass corner frequency. Table 11 lists example values for the high-pass filter.

$$HPF[1:0] = 65{,}536 \left[1 - \sqrt{1 - 2\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}}\right] \quad (11)$$

Where:

HPF = High-pass filter register value (converted to hexadecimal)

$\omega_N = 2\pi f_{HP}/f_{DATA}$ (normalized frequency, radians)

f_{HP} = High-pass corner frequency (Hz)

f_{DATA} = Data rate (Hz)

Table 11. High-Pass Filter Value Examples

f_{HP} (Hz)	DATA RATE (SPS)	HPF[1:0]
0.5	250	0337h
1.0	500	0337h
1.0	1000	019Ah

The HPF causes a small gain error, in which case the magnitude of the error depends on the ratio of f_{HP}/f_{DATA}. For many common values of (f_{HP}/f_{DATA}), the gain error is negligible. Figure 51 shows the gain error of the HPF. The gain error factor is illustrated in Equation 15 (see the *Appendix* at the end of this document).

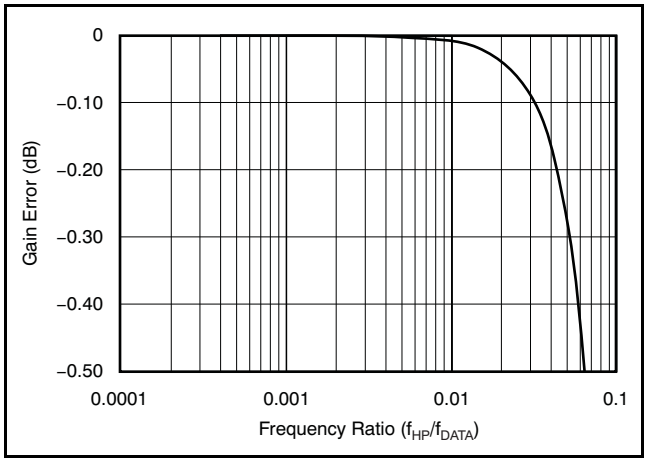


Figure 51. HPF Gain Error

Figure 52 shows the first-order amplitude and phase response of the HPF. Note that in the case of applying step inputs or synchronizing, the settling time of the filter should be taken into account.

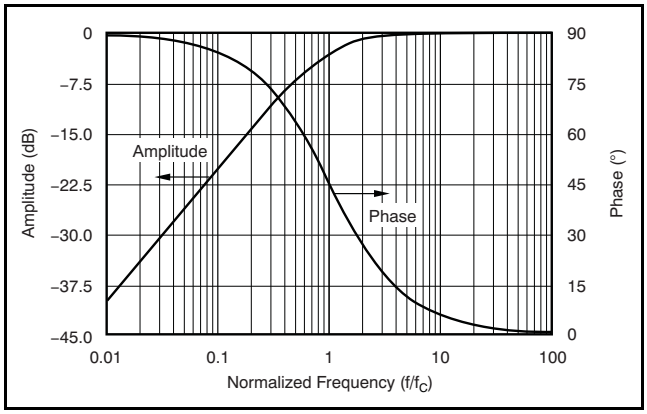


Figure 52. HPF Amplitude and Phase Response

MASTER CLOCK INPUT (CLK)

The ADS1282 requires a clock input for operation. The clock is applied to the CLK pin. The data conversion rate scales directly with the CLK frequency. Power consumption versus CLK frequency is relatively constant (see the *Typical Characteristics*).

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keep the clock trace as short as possible and use a 50-Ω series resistor close to the source.

SYNCHRONIZATION (SYNC PIN AND SYNC COMMAND)

The ADS1282 can be synchronized to an external event, as well as synchronized to other ADS1282 devices if the sync event is applied simultaneously.

The ADS1282 has two sources for synchronization: the SYNC input pin and the SYNC command. The ADS1282 also has two synchronizing modes: Pulse-sync and Continuous-sync. In Pulse-sync mode, the ADS1282 synchronizes to a single sync event. In Continuous-sync mode, either a single SYNC event is used to synchronize conversions or a continuous clock is applied to the pin with a period equal to integer multiples of the data rate. When the periods of the sync input and the $\overline{\text{DRDY}}$ output do not match, the ADS1282 re-synchronizes and conversions are restarted.

PULSE-SYNC MODE

In Pulse-sync mode, the ADS1282 stops and restarts the conversion process when a sync event occurs (by pin or command). When the sync event occurs, the device resets the internal memory; DRDY goes high (pulse SYNC mode) otherwise in Continuous SYNC mode, DRDY continues to toggle, and after the digital filter has settled, new conversion data are available, as shown in Figure 53 and Table 12.

Note that resynchronization occurs on the next rising CLK edge after the rising edge of the SYNC pin or after the eighth rising SCLK edge for opcode SYNC commands. To be effective, the SYNC opcode should be broadcast to all devices simultaneously.

CONTINUOUS-SYNC MODE

In Continuous-sync mode, either a single sync pulse or a continuous clock may be applied. When a single sync pulse is applied (rising edge), the device behaves similar to the Pulse-sync mode. However, in this mode, DRDY continues to toggle unaffected but the DOUT output is held low until data are ready, 63 DRDY periods later. When the conversion data are non-zero, new conversion data are ready (as shown in Figure 53).

When a continuous clock is applied to the SYNC pin, the period must be an integral multiple of the output data rate or the device re-synchronizes. When the sync input is first applied, the device re-synchronizes (under the condition $t_{SYNC} \neq N/f_{DATA}$). DRDY continues to output but DOUT is held low until the new data are ready. Then, if SYNC is applied again and the period matches an integral multiple of the output data rate, the device freely runs without re-synchronization. Note that the phase of the applied clock and output data rate (DRDY) are not matched because of the initial delay of DRDY after SYNC is first applied. Figure 54 shows the timing for Continuous-Sync mode.

Note that a SYNC clock input should be applied after the Continuous-Sync mode is set. The first rising edge of SYNC then causes a synchronization.

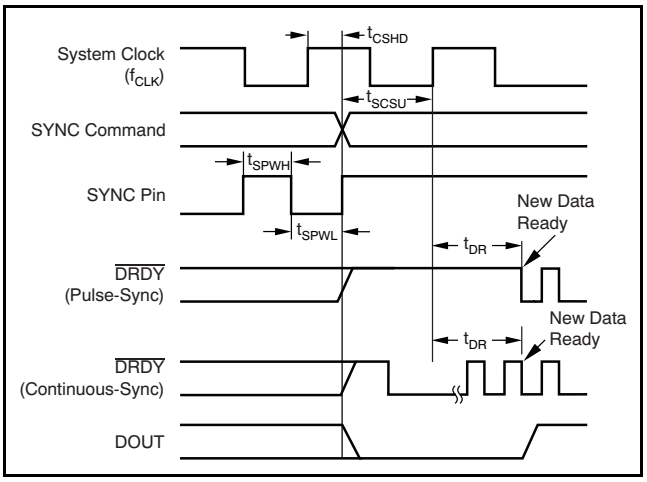


Figure 53. Pulse-Sync Timing, Continuous-Sync Timing with Single Sync

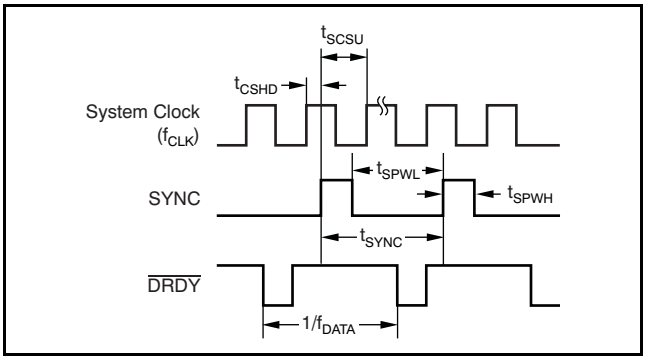


Figure 54. Continuous-Sync Timing with Sync Clock

Table 12. Pulse-Sync Timing for Figure 53 and Figure 54

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SYNC}	SYNC period(1)	1	Infinite	n/f_{DATA}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10		ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10		ns
$t_{SPWH, L}$	SYNC pulse width, high or low	2		$1/f_{CLK}$
t_{DR}	Time for data ready (SINC filter)	See Appendix, Table 26		
	Time for data ready (FIR filter)	$62.98046875/f_{DATA} + 466/f_{CLK}$		

(1) Continuous-Sync mode; a free-running SYNC clock input without causing re-synchronization.

RESET (RESET Pin and Reset Command)

The ADS1282 may be reset in two ways: toggle the RESET pin low or send a Reset command. When using the RESET pin, take it low and hold for at least $2/f_{CLK}$ to force a reset. The ADS1282 is held in reset until the pin is released. By command, RESET takes effect on the next rising edge of f_{CLK} after the eighth rising edge of SCLK of the command. Note that in order to ensure the Reset command can function, the SPI interface may require resetting itself; see the *Serial Interface* section.

In reset, registers are set to default and the conversions are synchronized on the next rising edge of CLK. New conversion data are available, as shown in Figure 55 and Table 13.

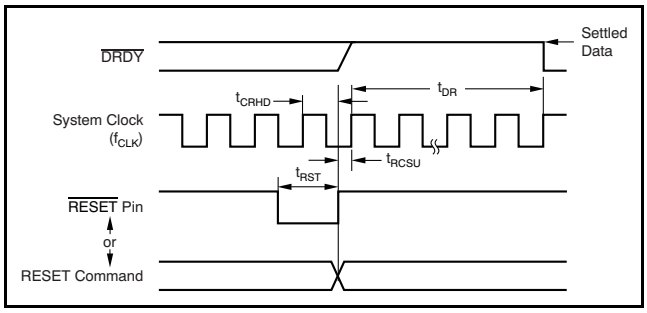


Figure 55. Reset Timing

Table 13. Reset Timing for Figure 55

PARAMETER	DESCRIPTION	MIN	UNITS
t_{CRHD}	CLK to RESET hold time	10	ns
t_{RCSU}	RESET to CLK setup time	10	ns
t_{RST}	RESET low	2	$1/f_{CLK}$
t_{DR}	Time for data ready	$62.98046875/f_{DATA} + 468/f_{CLK}$	

POWER-DOWN (PWDN Pin and Standby Command)

There are two ways to power-down the ADS1282: take the PWDN pin low or send a Standby command. When the PWDN pin is pulled low, the internal circuitry is disabled to minimize power and the contents of the register settings are reset.

In power-down, note that the device outputs remain active and the device inputs must not float. When the Standby command is sent, the SPI port and the configuration registers are kept active. Figure 56 and Table 14 show the timing.

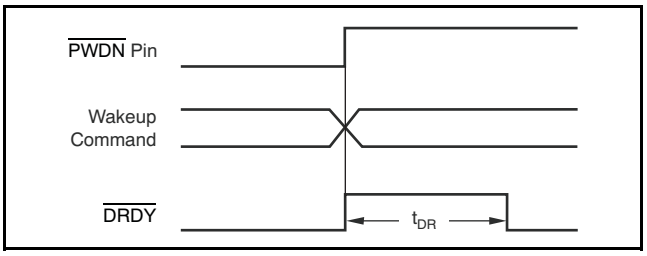


Figure 56. PWDN Pin and Wake-Up Command Timing (Table 14 shows t_{DR})

POWER-ON SEQUENCE

The ADS1282 has three power supplies: AVDD, AVSS, and DVDD. Figure 57 shows the power-on sequence of the ADS1282. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate an internal reset whose outputs are summed to generate a global internal reset. After the supplies have crossed the minimum thresholds, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, new conversion data are available, as shown in Figure 57 and Table 14.

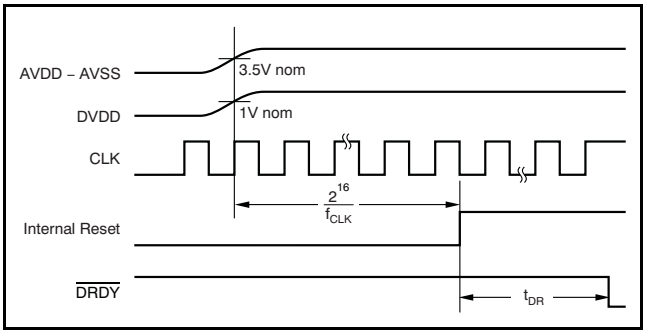


Figure 57. Power-On Sequence

Table 14. Power-On, PWDN Pin, and Wake-Up Command Timing for New Data

PARAMETER	DESCRIPTION		FILTER MODE
t_{DR}	Time for data ready 2^{16} CLK cycles after power-on; and new data ready after PWDN pin or Wake-Up command	See Appendix, Table 26	SINC (1)
		$62.98046875/f_{DATA} + 468/f_{CLK}$ (2)	FIR

(1) Supply power-on and PWDN pin default is 1000 SPS FIR.
(2) Subtract two CLK cycles for the Wake-Up command. The Wake-Up command is timed from the next rising edge of CLK to after the eighth rising edge of SCLK during command to DRDY falling.

DVDD POWER SUPPLY

The DVDD supply operates over the range of 1.75 V to 3.6 V. If DVDD is operated at less than 2.25 V, connect the DVDD pin to the BYPAS pin. If DVDD is greater than or equal to 2.25 V, do not connect DVDD to the BYPAS pin. Figure 58 shows this connection.

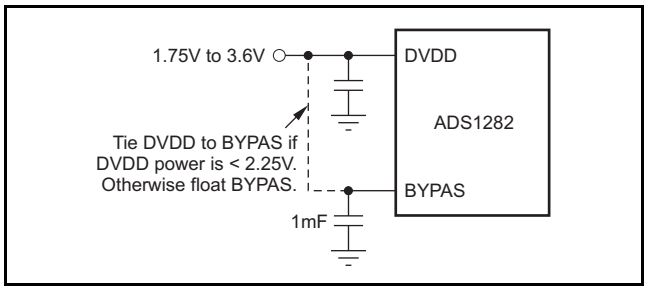


Figure 58. DVDD Power

SERIAL INTERFACE

A serial interface is used to read the conversion data and access the configuration registers. The interface consists of three basic signals: SCLK, DIN, and DOUT. An additional output, $\overline{\text{DRDY}}$, transitions low in Read Data Continuous mode when data are ready for retrieval. Figure 59 shows the connection when multiple converters are used.

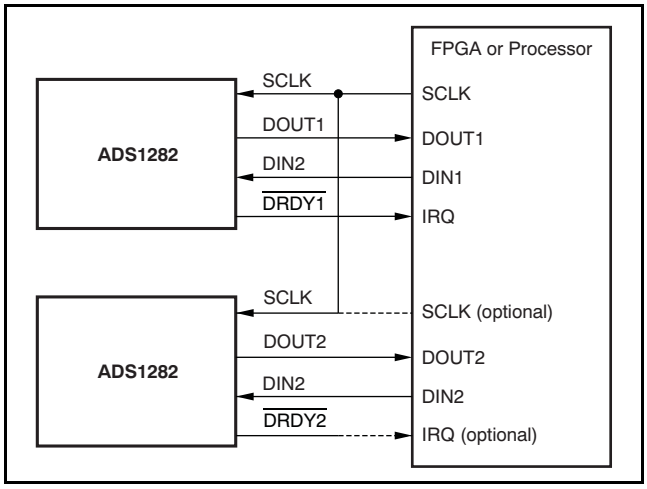


Figure 59. Interface for Multiple Devices

Serial Clock (SCLK)

The serial clock (SCLK) is an input that is used to clock data into (DIN) and out of (DOUT) the ADS1282. This input is a Schmitt-trigger input that has a high degree of noise immunity. However, it is recommended to keep SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. If SCLK is held low for 64 $\overline{\text{DRDY}}$ cycles, data transfer or commands in progress terminate and the SPI interface resets. The next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover the interface when a transmission is interrupted or SCLK inadvertently glitches. SCLK should remain low when not active.

Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADS1282. Keep DIN low when reading conversion data in the Read Data Continuous mode (except when issuing a STOP Read Data Continuous command). Data on DIN are shifted into the converter on the rising edge of SCLK. In Pin mode, DIN is not used.

Data Output (DOUT)

The data output pin (DOUT) is used to output data from the ADS1282. Data are shifted out on DOUT on the falling edge of SCLK.

Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output; when it transitions low, this transition indicates new conversion data are ready, as shown in Figure 60. When reading data by the continuous mode, the data must be read within four CLK periods before $\overline{\text{DRDY}}$ goes low again or the data are overwritten with new conversion data. When reading data by the command mode, the read operation can overlap the occurrence of the next $\overline{\text{DRDY}}$ without data corruption.

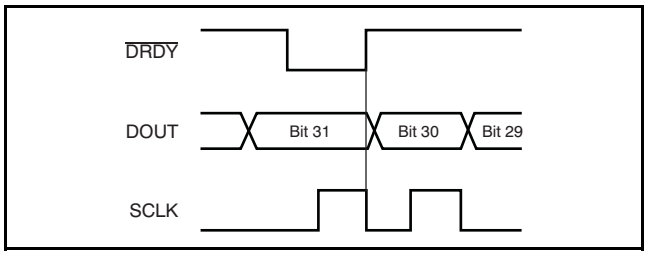


Figure 60. $\overline{\text{DRDY}}$ with Data Retrieval

$\overline{\text{DRDY}}$ resets high on the first falling edge of SCLK. Figure 60 and Figure 61 show the function of $\overline{\text{DRDY}}$ with and without data readback, respectively.

If data are not retrieved (no SCLK provided), $\overline{\text{DRDY}}$ pulses high for four f_{CLK} periods during the update time, as shown in Figure 61.

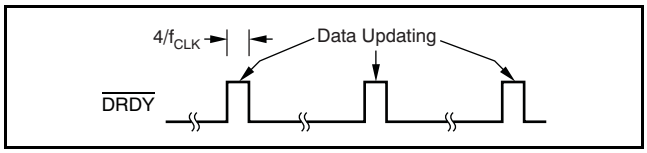


Figure 61. $\overline{\text{DRDY}}$ With No Data Retrieval

DATA FORMAT

The ADS1282 provides 32 bits of conversion data in binary twos complement format, as shown in Table 15. The LSB of the data is a redundant sign bit: '0' for positive numbers and '1' for negative numbers. However, when the output is clipped to +FS, the LSB = 1; when the output is clipped to –FS, the LSB = 0. If desired, the data readback may be stopped at 24 bits. Note that in sinc filter mode, the output data are scaled by 1/2.

Table 15. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	32-BIT IDEAL OUTPUT CODE(1)	
	FIR FILTER	SINC FILTER
$> \frac{V_{REF}}{2 \times PGA}$	7FFFFFFFh	(2)
$\frac{V_{REF}}{2 \times PGA}$	7FFFFFFEh	3FFFFFFFh
$\frac{V_{REF}}{2PGA \times (2^{30} - 1)}$	00000002h	00000001h
0	00000000h	00000000h
$\frac{-V_{REF}}{2PGA \times (2^{30} - 1)}$	FFFFFFFFh	FFFFFFFFh
$\frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000000h	(2)

(1) Excludes effects of noise, linearity, offset, and gain errors.

(2) In sinc filter mode, the output does not clip at half-scale code when the full-scale range is exceeded.

READING DATA

The ADS1282 has two ways to read conversion data: Read Data Continuous and Read Data By Command.

Read Data Continuous

In the Read Data Continuous mode, the conversion data are shifted out directly from the device without the need for sending a read command. This mode is the default mode at power-on. This mode is also enabled by the RDATAC command. When DRDY goes low, indicating that new data are available, the MSB of data appears on DOUT, as shown in Figure 62. The data are normally read on the rising edge of SCLK, at the occurrence of the first falling edge of SCLK, DRDY returns high. After 32 bits of data have been shifted out, further SCLK transitions cause DOUT to go low. If desired, the read operation may be stopped at 24 bits. The data shift operation must be completed within four CLK periods before DRDY falls again or the data may be corrupted.

When a Stop Read Data Continuous command is issued, the DRDY output is blocked but the ADS1282 continues conversions. In stop continuous mode, the data can only be read by command.

Read Data By Command

The Read Data Continuous mode is stopped by the SDATAC command. In this mode, conversion data are read by command. In the Read Data By Command mode, a read data command must be sent to the device for each data conversion (as shown in Figure 63). When the read data command is received (on the eighth SCLK rising edge), data are available to read only when DRDY goes low (t_{DR}). When DRDY goes low, conversion data appear on DOUT. The data may be read on the rising edge of SCLK.

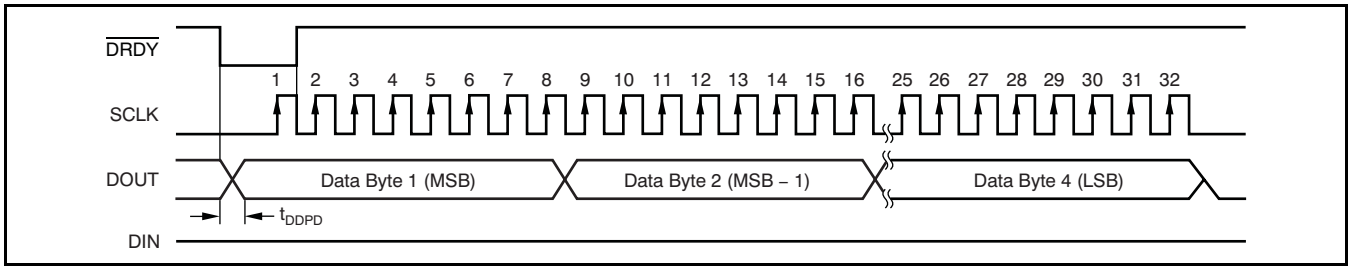


Figure 62. Read Data Continuous

Table 16. Timing Data for Figure 62

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DDPD}	DRDY to valid MSB on DOUT propagation delay(1)			100	ns

(1) Load on DOUT = 20 pF || 100 kΩ.

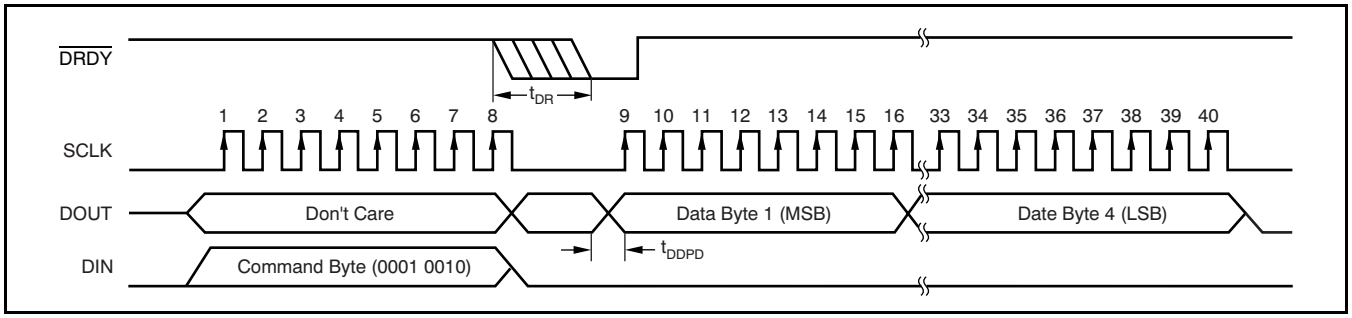


Figure 63. Read Data By Command, RDATA (t_{DDPD} timing is given in Table 16)

Table 17. Read Data Timing for Figure 63

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DR}	Time for new data after data read command	0		1	f_{DATA}

ONE-SHOT OPERATION

The ADS1282 can perform very power-efficient, one-shot conversions using the STANDBY command while under software control. Figure 64 shows this sequence. First, issue the STANDBY command to set the Standby mode.

When ready to make a measurement, issue the WAKEUP command. Monitor $\overline{\text{DRDY}}$; when it goes low, the fully settled conversion data are ready and may be read directly in Read Data Continuous mode. Afterwards, issue another STANDBY command. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

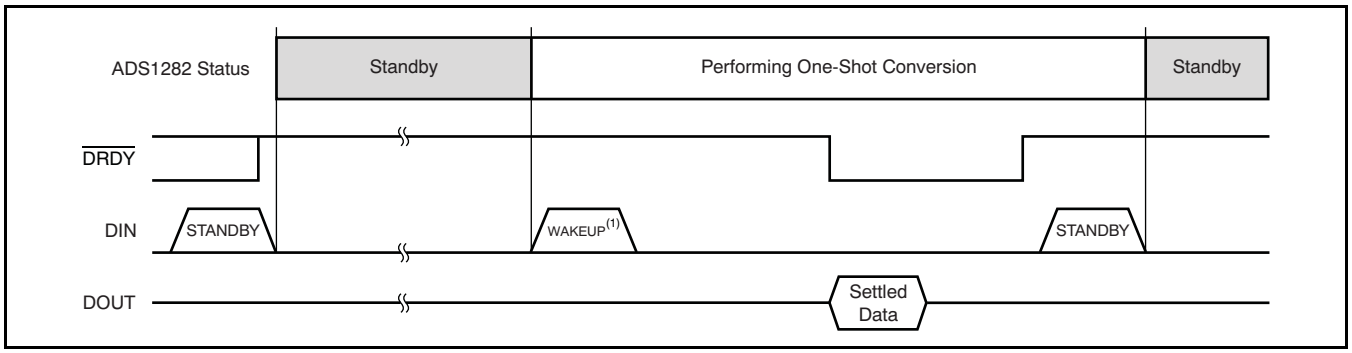
OFFSET AND FULL-SCALE CALIBRATION REGISTERS

The conversion data can be scaled for offset and gain before yielding the final output code. As shown in Figure 65, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 12 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (12)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

Note that the offset and full-scale calibrations apply to specific PGA settings. When the PGA changes, the contents of these registers may have to be recalculated. Calibration is bypassed in the sinc filter mode.



(1) See Figure 56 and Table 14 for time to new data.

Figure 64. One-Shot Conversions Using the STANDBY Command

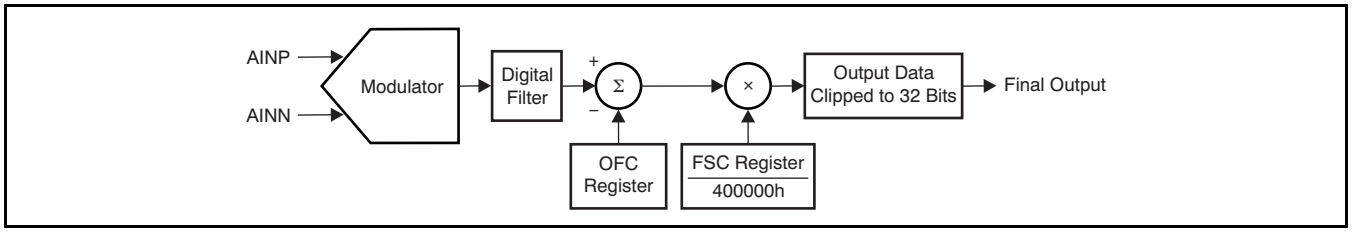


Figure 65. Calibration Block Diagram

OFC[2:0] Registers

The offset calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 20. The offset register is left-justified to align with the 32-bits of conversion data. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value). Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 18), to avoid input overload, the analog inputs cannot exceed the full-scale range.

Table 18. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	80000000h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
800000h	7FFFFF00h

(1) Full 32-bit final output code with zero code input.

FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 21. The full-scale calibration value is 24-bit, straight offset binary, normalized to 1.0 at code 400000h. Table 19 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). Note that while the gain calibration register value corrects gain errors above 1 (gain correction < 1), the full-scale range of the analog inputs cannot be exceeded to avoid input overload.

Table 19. Full-Scale Calibration Register Values

FSC REGISTER	GAIN CORRECTION
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

Table 20. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
OFC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 21. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
FSC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

CALIBRATION COMMANDS

Calibration commands may be sent to the ADS1282 to calibrate the conversion data. The values of the offset and gain calibration registers are internally written to perform calibration. The appropriate input signals must be applied to the ADS1282 inputs before sending the commands. Use slower data rates to achieve more consistent calibration results; this effect is a byproduct of the lower noise that these data rates provide. Also, if calibrating at power-on, be sure the reference voltage is fully settled.

Figure 66 shows the calibration command sequence. After the analog input voltage (and reference) have stabilized, send the Stop Data Continuous command followed by the SYNC and Read Data Continuous commands. 64 data periods later, $\overline{\text{DRDY}}$ goes low. After $\overline{\text{DRDY}}$ goes low, send the Stop Data Continuous, then the Calibrate command followed by the Read Data Continuous command. After 16 data periods, calibration is complete and conversion data may be read at this time. The SYNC input must remain high during the calibration sequence.

Note that the calibration commands apply to specific PGA settings. If the PGA is changed, recalibration is necessary. Calibration is bypassed in the sinc filter mode.

OFSCAL Command

The OFSCAL command performs an offset calibration. Before sending the offset calibration command, a *zero* input signal must be applied to the ADS1282 and the inputs allowed to stabilize. When the command is sent, the ADS1282 averages 16 readings and then writes this value to the OFC register. The contents of the OFC register may be subsequently read or written. During offset calibration, the full-scale correction is bypassed.

GANCAL Command

The GANCAL command performs a gain calibration. Before sending the GANCAL command, a dc input signal must be applied that is in the range of, but not exceeding, positive or negative full-scale. After the signal has stabilized, the command can be sent. The ADS1282 averages 16 readings, then computes the value that compensates for the gain error. The gain correction value is then written to the FSC register. The contents of the GANCAL register may be subsequently read or written. Note that while the gain calibration command corrects for gain errors above 1 (gain correction < 1), to avoid input overload, the analog inputs cannot exceed full-scale range. The gain calibration should be performed after the offset calibration.

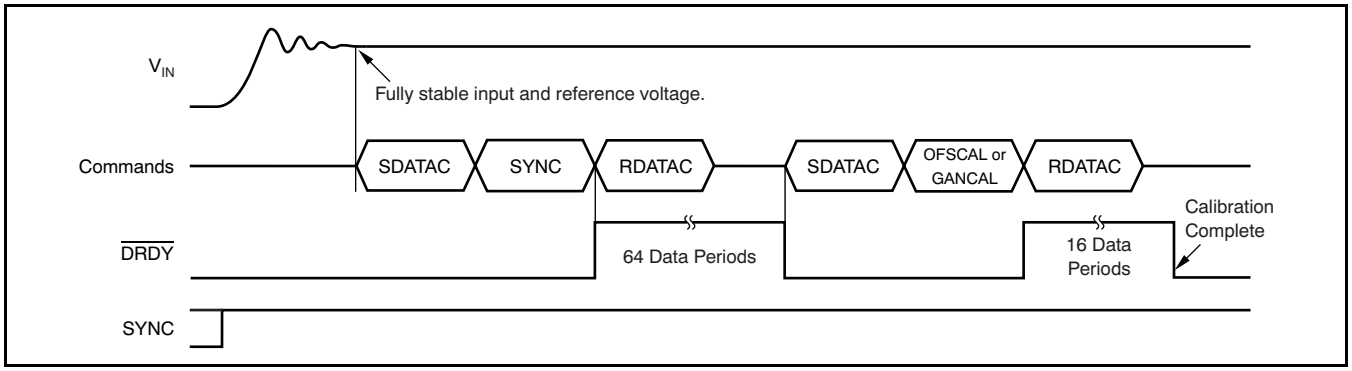


Figure 66. Offset/Gain Calibration Timing

USER CALIBRATION

System calibration of the ADS1282 can be performed without using the calibration commands. This procedure requires the calibration values to be externally calculated and then written to the calibration registers. The steps for this procedure are:

1. Set the OFSCAL[2:0] register = 0h and GANCAL[2:0] = 400000h. These values set the offset and gain registers to 0 and 1, respectively.
2. Apply a *zero* differential input to the input of the system. Wait for the system to settle and then average *n* output readings. Higher numbers of averaged readings result in more consistent calibration. Write the averaged value to the OFC register.
3. Apply a differential positive or negative dc signal, or an ac signal, less than the *full-scale* input to the system. Wait for the system to settle and then average the *n* output readings.

The value written to the FSC registers is calculated by Equation 13.

DC signal calibration is shown in Equation 13. The expected output code is based on 31-bit output data.

$$\text{FSC}[2:0] = 400000\text{h} \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \quad (13)$$

For ac signal calibration, use an RMS value of collected data (as shown in Equation 14).

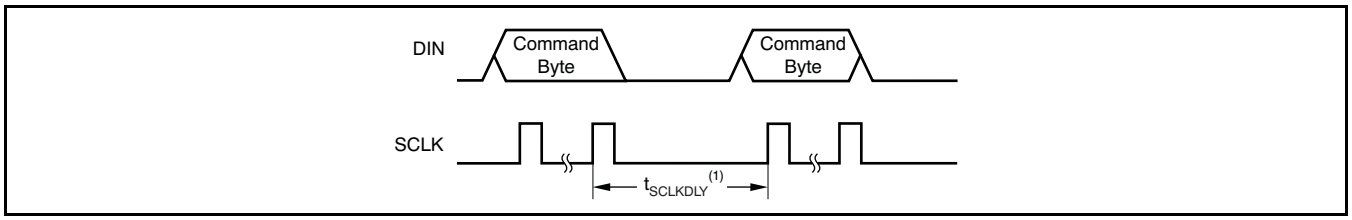
$$\text{FSC}[2:0] = 400000\text{h} \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \quad (14)$$

COMMANDS

The commands listed in Table 22 control the operation of the ADS1282. Most commands are stand-alone (that is, 1 byte in length); the register reads and writes require a second command byte in addition to the actual data bytes.

A delay of 24 f_{CLK} cycles between commands and between bytes within a command is required, starting from the last SCLK rising edge of one command to the first SCLK rising edge of the following command. This delay is shown in Figure 67.

In Read Data Continuous mode, the ADS1282 places conversion data on the DOUT pin as SCLK is applied. As a consequence of the potential conflict of conversion data on DOUT and data placed on DOUT resulting from a register or Read Data By Command operation, it is necessary to send a STOP Read Data Continuous command before Register or Data Read By Command. The STOP Read Data Continuous command disables the direct output of conversion data on the DOUT pin.



(1) $t_{SCLKDLY} = 24/f_{CLK}$ (min).

Figure 67. Consecutive Commands

Table 22. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1st COMMAND BYTE(1) (2)	2nd COMMAND BYTE(3)
WAKEUP	Control	Wake-up from Standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter Standby mode	0000 001X (0 h or 03h)	
SYNC	Control	Synchronize the A/D conversion	0000 010X (04h or 5h)	
$\overline{\text{RESET}}$	Control	Reset registers to default values	0000 011X (06h or 07h)	
RDATAC	Control	Read data continuous	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* register(s) at address *rrrrr* (4)	00r rrrr (20h + 000r rrrr)	000n nnnn (00h + n nnnn)
WREG	Register	Write *nnnnn* register(s) at address *rrrrr*	010r rrrr (40h + 000r rrrr)	000n nnnn (00h + n nnnn)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = don't care.
(2) rrrrr = starting address for register read and write commands.
(3) nnnnn = number of registers to be read/written – 1. For example, to read/write three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel Read Data Continuous mode before sending a command.

WAKEUP: Wake-Up From Standby Mode

Description: This command is used to exit the standby mode. Upon sending the command, the time for the first data to be ready is illustrated in Figure 56 and Table 15. Sending this command during normal operation has no effect; for example, reading data by the Read Data Continuous method with DIN held low.

STANDBY: Standby Mode

Description: This command places the ADS1282 into Standby mode. In Standby, the device enters a reduced power state where a low quiescent current remains to keep the register settings and SPI interface active. For complete device shutdown, take the PWDN pin low (register settings are not saved). To exit Standby mode, issue the WAKEUP command. The operation of Standby mode is shown in Figure 68.

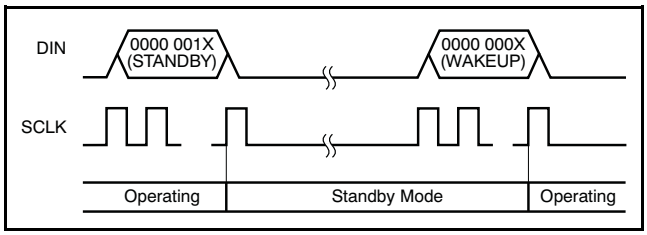


Figure 68. STANDBY Command Sequence

SYNC: Synchronize the A/D Conversion

Description: This command synchronizes the A/D conversion. Upon receipt of the command, the reading in progress is cancelled and the conversion process is re-started. In order to synchronize multiple ADS1282s, the command must be sent simultaneously to all devices. Note that the SYNC pin must be high for this command.

RESET: Reset the Device

Description: The RESET command resets the registers to default values, enables the Read Data Continuous mode, and restarts the conversion process; the RESET command is functionally the same as the RESET pin. See Figure 55 for the RESET command timing.

RDATAC: Read Data Continuous

Description: This command enables the Read Data Continuous mode (default mode). In this mode, conversion data can be read from the device directly without the need to supply a data read command. Each time DRDY falls low, new data are available to read. See the *Read Data Continuous* section for more details.

SDATAC: Stop Read Data Continuous

Description: This command stops the Read Data Continuous mode. Exiting the Read Data Continuous mode is required before sending Register and Data read commands. This command suppresses the DRDY output, but the ADS1282 continues conversions.

RDATA: Read Data By Command

Description: This command reads the conversion data. See the *Read Data By Command* section for more details.

RREG: Read Register Data

Description: This command is used to read single or multiple register data. The command consists of a two-byte op-code argument followed by the output of register data. The first byte of the op-code includes the starting address, and the second byte specifies the number of registers to read – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to read.

Starting with the 16th falling edge of SCLK, the register data appear on DOUT.

The RREG command is illustrated in Figure 69. Note that a delay of 24 f_{CLK} cycles is required between each byte transaction.

WREG: Write to Register

Description: This command writes single or multiple register data. The command consists of a two-byte op-code argument followed by the input of register data. The first byte of the op-code contains the starting address and the second byte specifies the number of registers to write – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to write.

Data byte(s): one or more register data bytes, depending on the number of registers specified.

Figure 70 illustrates the WREG command.

Note that a delay of 24 f_{CLK} cycles is required between each byte transaction.

OFSCAL: Offset Calibration

Description: This command performs an offset calibration. The inputs to the converter (or the inputs to the external pre-amplifier) should be zeroed and allowed to stabilize before sending this command. The offset calibration register updates after this operation. See the *Calibration Commands* section for more details.

GANCAL: Gain Calibration

Description: This command performs a gain calibration. The inputs to the converter should have a stable dc input, preferably close to (but not exceeding) positive full-scale. The gain calibration register updates after this operation. See the *Calibration Commands* section for more details.

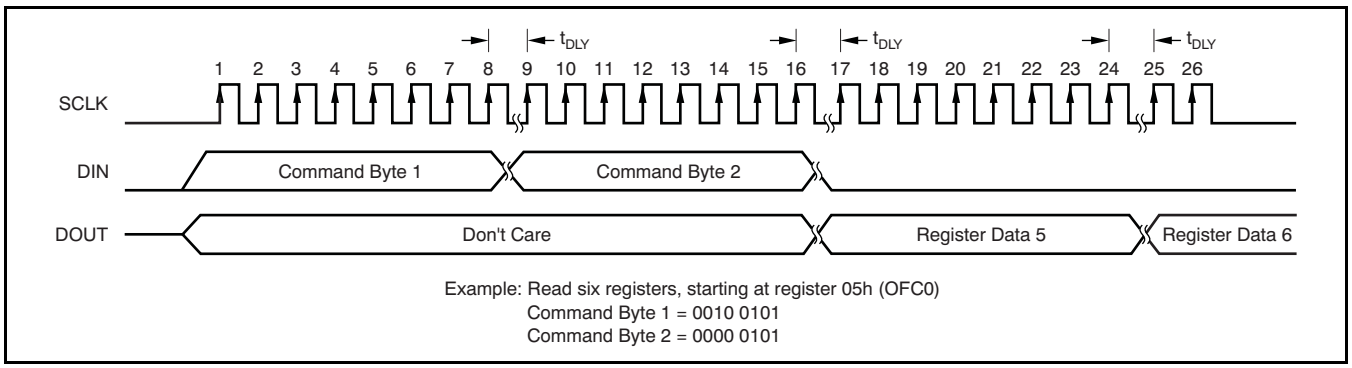


Figure 69. Read Register Data (Table 23 shows t_{DLY})

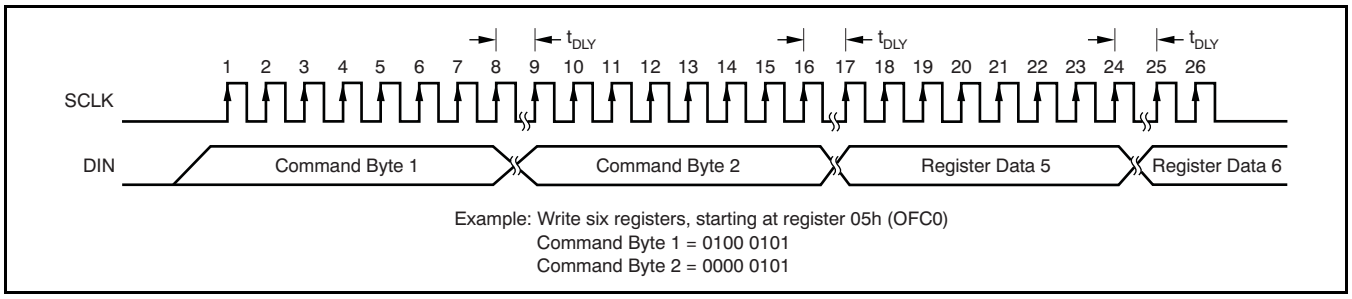


Figure 70. Write Register Data (Table 23 shows t_{DLY})

Table 23. t_{DRY} Value

PARAMETER	MIN
t_{DLY}	$24/f_{CLK}$

REGISTER MAP

Collectively, the registers contain all the information needed to configure the part, such as data rate, filter selection, calibration, etc. The registers are accessed by the RREG and WREG commands. The registers can be accessed individually or as a block of registers by sending or receiving consecutive bytes.

Table 24. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	X0h	ID3	ID2	ID1	ID0	0	0	0	0
01h	CONFIG0	52h	SYNC	MODE	DR2	DR1	DR0	PHS	FILTR1	FILTR0
02h	CONFIG1	08h	0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

ID : ID REGISTER (ADDRESS 00h)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	0	0	0	0

Reset value = X0h.

Bit[7:4] **ID[3:0]**

Factory-programmed identification bits (read-only)

Bit[3:0] **Reserved**

Always write '0'

CONFIG0 : CONFIGURATION REGISTER 0 (ADDRESS 01h)

7	6	5	4	3	2	1	0
SYNC	MODE	DR2	DR1	DR0	PHASE	FILTR1	FILTR0

Reset value = 52h.

Bit[7] **SYNC**

Synchronization mode
0: Pulse SYNC mode (default)
1: Continuous SYNC mode

Bit[6] **MODE**

0: Low-power mode
1: High-resolution mode (default)

Bit[5:3] **Data Rate Select**

DR[2:0]

000: 250SPS
001: 500SPS
010: 1000SPS (default)
011: 2000SPS
100: 4000SPS

Bit[2] **FIR Phase Response**

PHASE

0: Linear phase (default)
1: Minimum phase

Bit[1:0] **Digital Filter Select**

FILTR[1:0]

Digital filter configuration
00: On-chip filter bypassed, modulator output mode
01: Sinc filter block only
10: Sinc + LPF filter blocks (default)
11: Sinc + LPF + HPF filter blocks

CONFIG1 : CONFIGURATION REGISTER 1 (ADDRESS 02h)

7	6	5	4	3	2	1	0
0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0

Reset value = 08h.

Bit[7] **Reserved**

Always write '0'

Bit[6:4] **MUX Select**

MUX[2:0]

000: AINP1 and AINN1 (default)
001: AINP2 and AINN2
010: Internal short via 400Ω
011:AINP1 and AINN1 connected to AINP2 and AINN2
100: External short to AINN2

Bit[3] **PGA Chopping Enable**

CHOP

0: PGA chopping disabled
1: PGA chopping enabled (default)

Bit[2:0] **PGA Gain Select**

PGA[2:0]

000: G = 1 (default)
001: G = 2
010: G = 4
011: G = 8
100: G = 16
101: G = 32
110: G = 64

HPF1 and HPF0

These two bytes (high-byte and low-byte, respectively) set the corner frequency of the high-pass filter.

HPF0: High-Pass Filter Corner Frequency, Low Byte (Address 03h)

7	6	5	4	3	2	1	0
HP07	HP06	HP05	HP04	HP03	HP02	HP01	HP00

Reset value = 32h.

HPF1: High-Pass Filter Corner Frequency, High Byte (Address 04h)

7	6	5	4	3	2	1	0
HP15	HP14	HP13	HP12	HP11	HP10	HP09	HP08

Reset value = 03h.

OFC2, OFC1, OFC0

These three bytes set the offset calibration value.

OFC0: Offset Calibration, Low Byte (Address 05h)

7	6	5	4	3	2	1	0
OC07	OC06	OC05	OC04	OC03	OC02	OC01	OC00

Reset value = 00h.

OFC1: Offset Calibration, Mid Byte (Address 06h)

7	6	5	4	3	2	1	0
OC15	OC14	OC13	OC12	OC11	OC10	OC09	OC08

Reset value = 00h.

OFC2: Offset Calibration, High Byte (Address 07h)

7	6	5	4	3	2	1	0
OC23	OC22	OC21	OC20	OC19	OC18	OC17	OC16

Reset value = 00h.

FSC2, FSC1, FSC0

These three bytes set the full-scale calibration value.

FSC0: Full-Scale Calibration, Low Byte (Address 08h)

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

Reset value = 00h.

FSC1: Full-Scale Calibration, Mid Byte (Address 09h)

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

Reset value = 00h.

FSC2: Full-Scale Calibration, High Byte (Address 0Ah)

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

Reset value = 40h.

CONFIGURATION GUIDE

After RESET or power-on, the registers can be configured using the following procedure:

1. **Reset the serial interface.** Before using the serial interface, it may be necessary to recover the serial interface (undefined I/O power-up sequencing may cause false SCLK detection). To reset the SPI interface, toggle the $\overline{\text{RESET}}$ pin or, when in Read Data Continuous mode, hold SCLK low for 64 $\overline{\text{DRDY}}$ periods.
2. **Configure the registers.** The registers are configured by either writing to them individually or as a group. Software may be configured in either mode. The SDATAC command must be sent before register read/write operations to cancel the Read Data Continuous mode.
3. **Verify register data.** The register may be read back for verification of device communications.
4. **Set the data mode.** After register configuration, the device may be configured for Read Data Continuous mode, either by the Read Data Continuous command or configured in Read Data By Register mode using SDATAC command.
5. **Synchronize readings.** Whenever SYNC is high, the ADS1282 freely runs the data conversions. To stop and re-sync the conversions, take SYNC low and then high.
6. **Read data.** If the Read Data Continuous mode is active, the data are read directly after $\overline{\text{DRDY}}$ falls by applying SCLK pulses. If the Read Data Continuous mode is inactive, the data can only be read by Read Data By Command. The Read Data opcode command must be sent in this mode to read each conversion result (note that $\overline{\text{DRDY}}$ only asserts after each read data command is sent).

APPLICATION INFORMATION

The ADS1282 is a very high-resolution ADC. Optimal performance requires giving special attention to the support circuitry and printed circuit board (PCB) design. Locate noisy digital components, such as microcontrollers, oscillators, etc, in an area of the PCB away from the converter or front-end components. Locating the digital components close to the power-entry point keeps the digital current path short and separate from sensitive analog components.

A typical geophone front-end application is shown in Figure 71. The application shows the ADS1282 operation with dual ±2.5-V analog supplies. The ADS1282 can also operate with a single 5-V analog supply.

The geophone input signal is filtered both differentially, by components C_4 and R_1 to R_4 and filtered independently by components C_2, C_3 and R_1, R_2. The differential filter removes high-frequency normal mode components from the input signal. The independent filters remove high-frequency components that are common to both input signals leads (common-mode filter). The recommended input filters may not be required for all applications depending on the system requirements.

Resistors R_5 and R_6 bias the signals inputs to midsupply (ground), and also provide the bias current return path for the ADS1282 inputs. For single-supply operation, set the bias to a low impedance 2.5 V (AVDD/2). Resistors R_5 and R_6 can also influence common-mode attenuation. To maintain good CMR performance, resistors R_5 and R_6 may require matching.

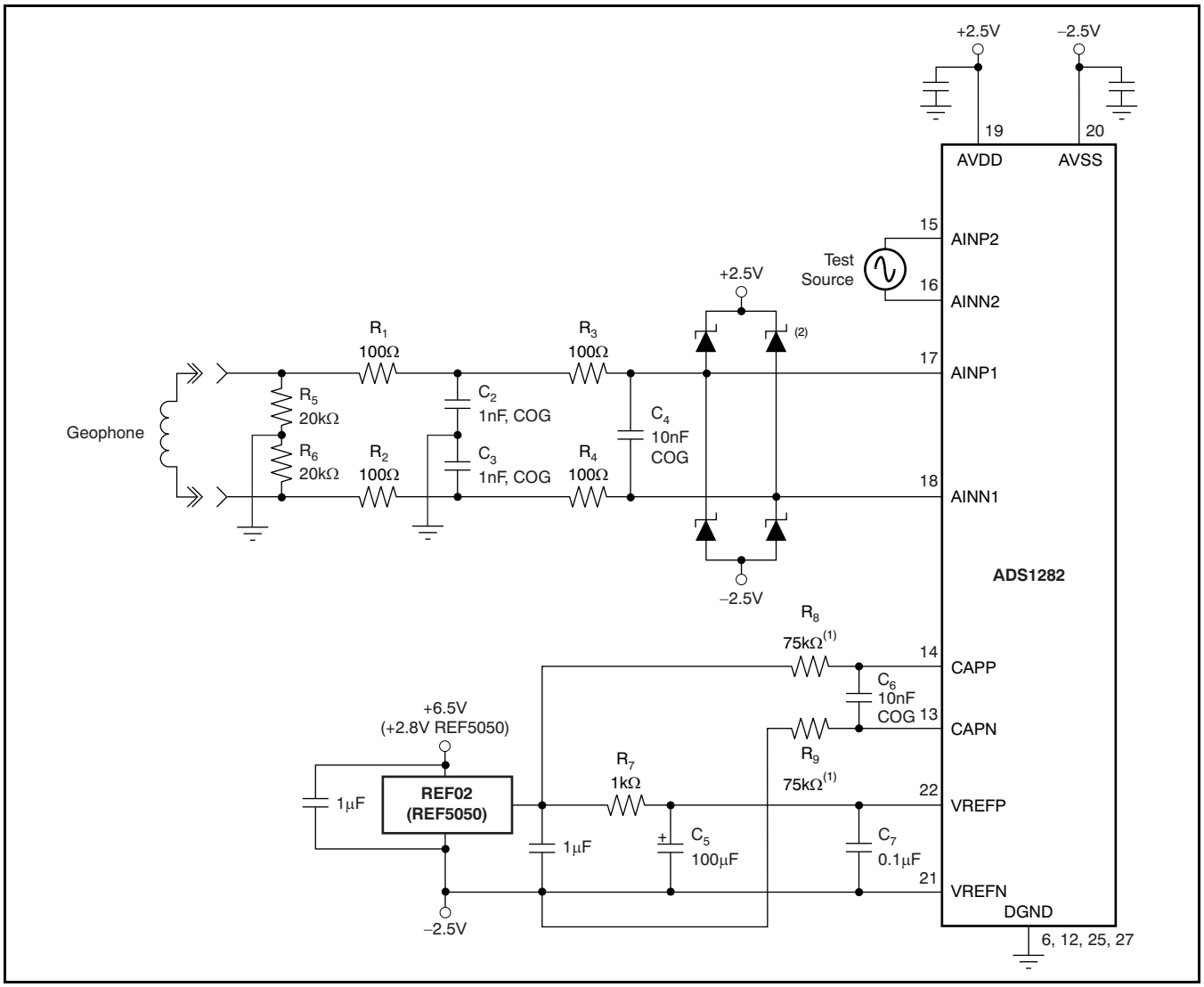
Diode clamps protect the ADS1282 inputs from voltage transients and overloads.

The REF02 +5-V reference provides the reference to the ADS1282. The reference output is filtered by R_7 and C_5. The filter requires several seconds to settle after power-on. Capacitor C_7 provides high-frequency bypassing of the reference inputs and should be placed close to the ADS1282 pins. Note that R_7 (1kΩ) results in a systematic gain error (–1.2% in high-resolution mode, and –0.6% in low-power mode).

Alternatively, the REF5050 (5V) or REF5045 (4.5V) reference can be used. The REF5045 reference has the advantage of operating from the +5V power supply. The REF5050 requires 5.2-V minimum power supply. The noise filter is also required on these references.

Optional components R_8, and R_9 provides a 20mV offset to the ADS1282. The internal 300-Ω resistors form a voltage divider with the external resistors to provide the offset. The offset moves the low level idle tones out of the passsband. Note that the offset is independent of the PGA setting. To maintain good CMR performance, R_{10} and R_{11} should be matched to 0.1%, and the traces routed back directly to the reference.

Capacitor C_6 (10 nF) filters the PGA output glitches caused by sampling of the modulator. The capacitor also forms a low-pass filter on the input signal with a cut-off frequency 25 kHz.



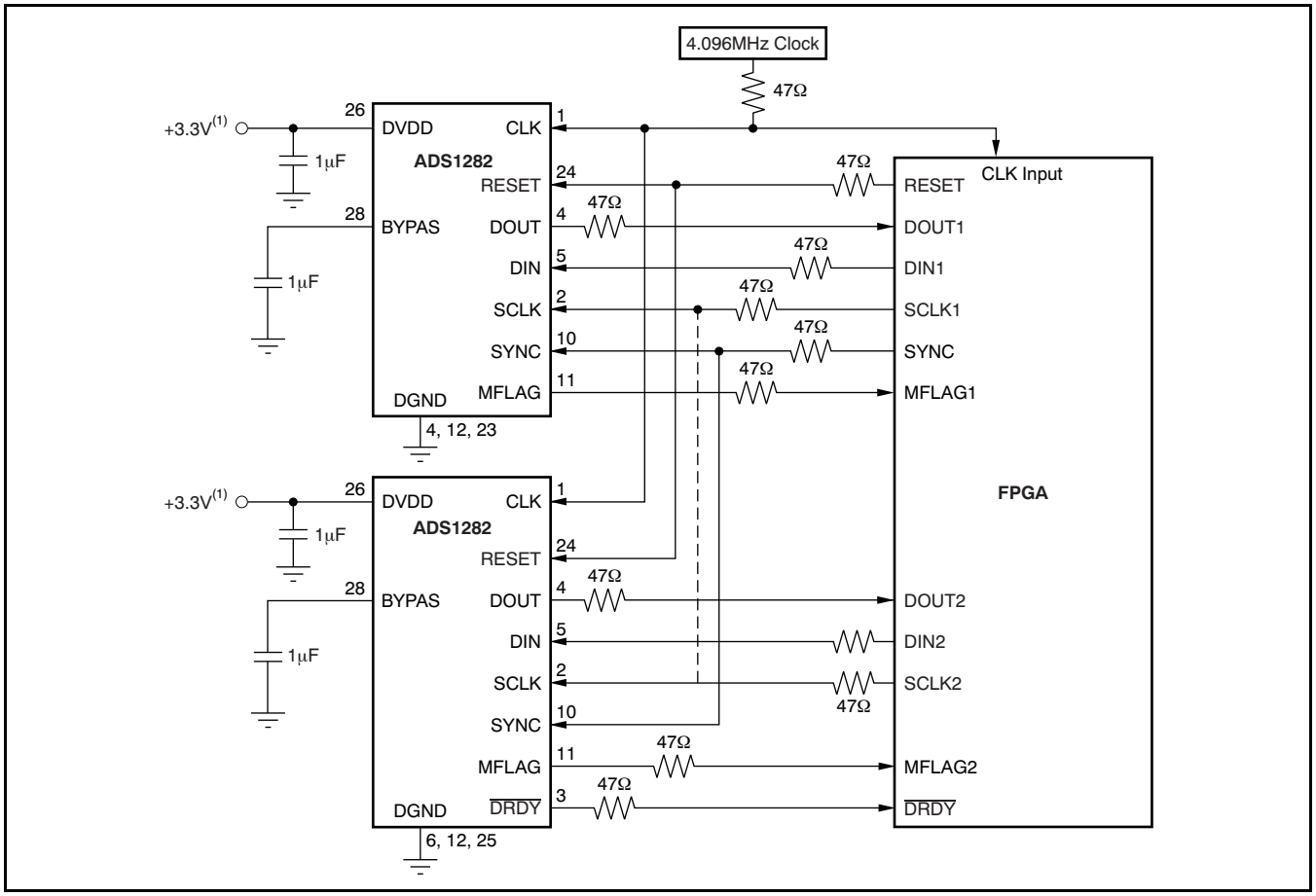
(1) Optional 20 mV offset. Match to 0.1% to maintain CMR.

Figure 71. Geophone Interface Application

Figure 72 shows the digital connection to a field programmable gate array (FPGA) device. In this example, two ADS1282s are shown connected. The DRDY output from each ADS1282 can be used; however, when the devices are synchronized, the DRDY output from only one device is sufficient. A shared SCLK line between the devices is optional.

The modulator over-range flag (MFLAG) from each device ties to the FPGA. For synchronization, one SYNC control line connects all ADS1282 devices. The RESET line also connects to all ADS1282 devices.

For best performance, the FPGA and the ADS1282s should operate from the same clock. Avoid ringing on the digital inputs. 47-Ω resistors in series with the digital traces can help to reduce ringing by controlling impedances. Place the resistors at the source (driver) end of the trace. Unused digital inputs should not float; tie them to DVDD or GND. This includes the modulator data pins, M0, M1, and MCLK.



NOTE: Dashed line is optional.

(1) For DVDD < 2.25 V, see the *DVDD Power Supply* section.

Figure 72. Microcontroller Interface with Dual ADS1282s

APPENDIX

Table 25. FIR Stage Coefficients

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
			Scaling = 134217728		Scaling = 134217728	
	Scaling = 1/8388608		LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_0	–10944	–774	–73	819	–132	11767
b_1	0	0	–874	8211	–432	133882
b_2	103807	8994	–4648	44880	–75	769961
b_3	0	0	–16147	174712	2481	2940447
b_4	–507903	–51663	–41280	536821	6692	8262605
b_5	0	0	–80934	1372637	7419	17902757
b_6	2512192	199523	–120064	3012996	–266	30428735
b_7	4194304	0	–118690	5788605	–10663	40215494
b_8	2512192	–629120	–18203	9852286	–8280	39260213
b_9	0	0	224751	14957445	10620	23325925
b_{10}	–507903	2570188	580196	20301435	22008	–1757787
b_{11}	0	4194304	893263	24569234	348	–21028126
b_{12}	103807	2570188	891396	26260385	–34123	–21293602
b_{13}	0	0	293598	24247577	–25549	–3886901
b_{14}	–10944	–629120	–987253	18356231	33460	14396783
b_{15}		0	–2635779	9668991	61387	16314388
b_{16}		199523	–3860322	327749	–7546	1518875
b_{17}		0	–3572512	–7171917	–94192	–12979500
b_{18}		–51663	–822573	–10926627	–50629	–11506007
b_{19}		0	4669054	–10379094	101135	2769794
b_{20}		8994	12153698	–6505618	134826	12195551
b_{21}		0	19911100	–1333678	–56626	6103823
b_{22}		–774	25779390	2972773	–220104	–6709466
b_{23}			27966862	5006366	–56082	–9882714
b_{24}			Only half shown; symmetric starting with b_{22}.	4566808	263758	–353347
b_{25}				2505652	231231	8629331
b_{26}				126331	–215231	5597927
b_{27}				–1496514	–430178	–4389168
b_{28}				–1933830	34715	–7594158
b_{29}				–1410695	580424	–428064
b_{30}				–502731	283878	6566217
b_{31}				245330	–588382	4024593
b_{32}				565174	–693209	–3679749
b_{33}				492084	366118	–5572954
b_{34}				231656	1084786	332589
b_{35}				–9196	132893	5136333
b_{36}				–125456	–1300087	2351253
b_{37}				–122207	–878642	–3357202
b_{38}				–61813	1162189	–3767666
b_{39}				–4445	1741565	1087392
b_{40}				22484	–522533	3847821
b_{41}				22245	–2490395	919792
b_{42}				10775	–688945	–2918303

Table 25. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	Scaling = 1/8388608		Scaling = 134217728		Scaling = 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{43}				940	2811738	–2193542
b_{44}				–2953	2425494	1493873
b_{45}				–2599	–2338095	2595051
b_{46}				–1052	–4511116	–79991
b_{47}				–43	641555	–2260106
b_{48}				214	6661730	–963855
b_{49}				132	2950811	1482337
b_{50}				33	–8538057	1480417
b_{51}					–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					Only half shown; symmetric starting with b_{53}.	644405
b_{56}						–675082
b_{57}						–806095
b_{58}						211391
b_{59}						740896
b_{60}						141976
b_{61}						–527673
b_{62}						–327618
b_{63}						278227
b_{64}						363809
b_{65}						–70646
b_{66}						–304819
b_{67}						–63159
b_{68}						205798
b_{69}						124363
b_{70}						–107173
b_{71}						–131357
b_{72}						31104
b_{73}						107182
b_{74}						15644
b_{75}						–71728
b_{76}						–36319
b_{77}						38331
b_{78}						38783
b_{79}						–13557
b_{80}						–31453
b_{81}						–1230
b_{82}						20983
b_{83}						7729
b_{84}						–11463
b_{85}						–8791
b_{86}						4659

Table 25. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	Scaling = 1/8388608		Scaling = 134217728		Scaling = 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{87}						7126
b_{88}						–732
b_{89}						–4687
b_{90}						–976
b_{91}						2551
b_{92}						1339
b_{93}						–1103
b_{94}						–1085
b_{95}						314
b_{96}						681
b_{97}						16
b_{98}						–349
b_{99}						–96
b_{100}						144
b_{101}						78
b_{102}						–46
b_{103}						–42
b_{104}						9
b_{105}						16
b_{106}						0
b_{107}						–4

$$\text{HPF Gain Error Factor} = \frac{1 - \sqrt{1 - 2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}}{2 - \left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)} \quad (15)$$

See the *HPF Stage* section for an example of how to use this equation.

Table 26. t_{DR} Time for Data Ready (Sinc Filter)

f_{DATA}	f_{CLK} (1)
128k	440
64k	616
32k	968
16k	1672
8k	2824

(1) For SYNC and Wake-Up commands, f_{CLK} = number of CLK cycles from next rising CLK edge directly after eighth rising SCLK edge to DRDY falling edge. For Wake-Up command only, subtract two f_{CLK} cycles.

Table 26 is referenced by Table 12 and Table 14.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS1282SJT	PREVIEW	CDIP	JT	28		TBD	Call TI	Call TI
ADS1282SKGDA	PREVIEW	XCEPT	KGD	0	400	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

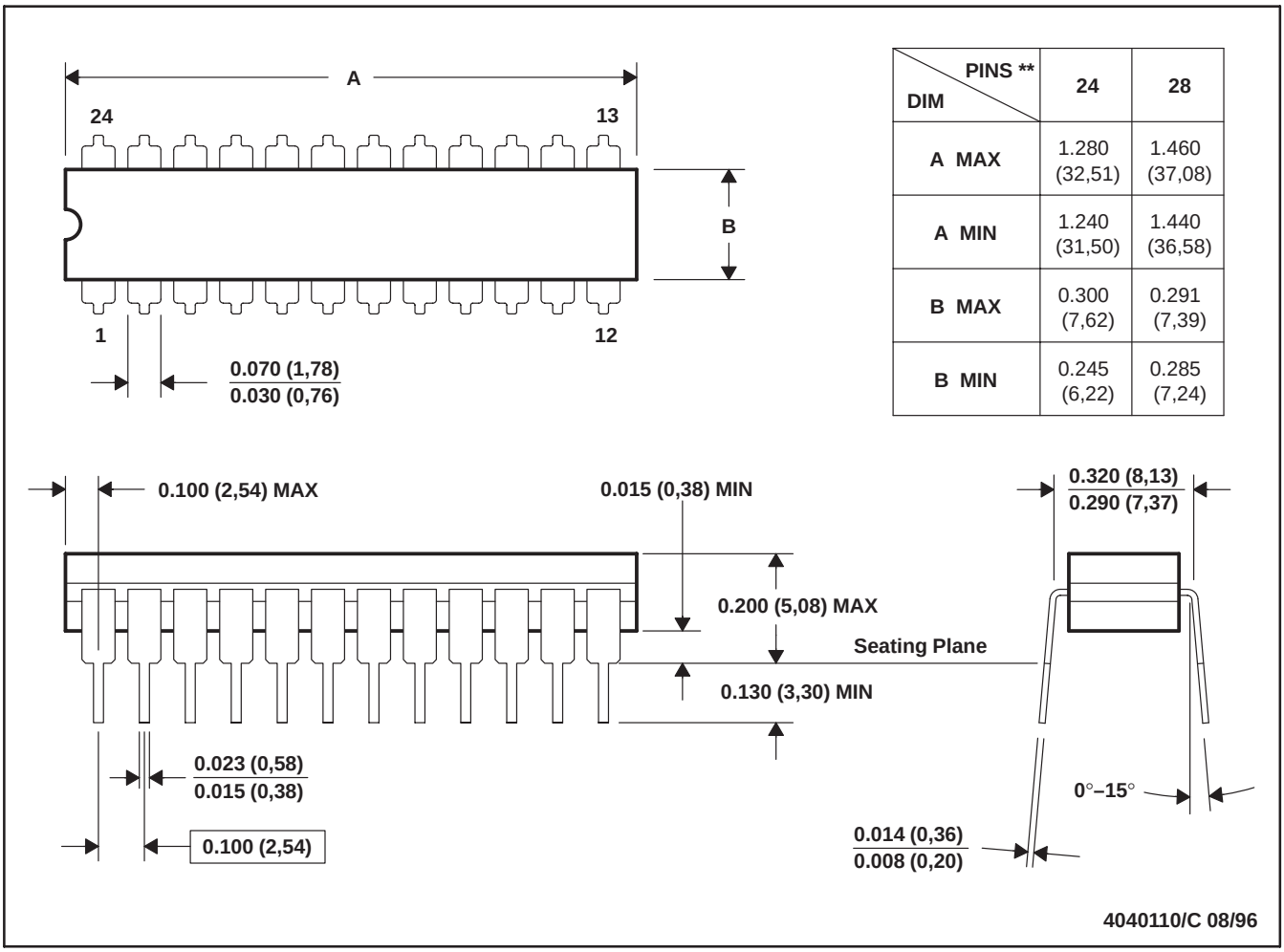
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN



DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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