OCTAL SIMULTANEOUS-SAMPLING 24-BIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Simultaneously Measure Eight Channels**
- **Up to 128-kSPS Data Rate**
- **AC Performance:**
  62-kHz Bandwidth
  111-dB SNR (High-Resolution Mode)
  –108-dB THD
- **DC Accuracy:**
  0.8-µV/°C Offset Drift
  1.3-ppm/°C Gain Drift
- **Selectable Operating Modes:**
  High-Speed: 128 kSPS, 106 dB SNR
  High-Resolution: 52 kSPS, 111 dB SNR
  Low-Power: 52 kSPS, 31 mW/ch
  Low-Speed: 10 kSPS, 7 mW/ch
- **Linear Phase Digital Filter**
- **SPI™ or Frame-Sync Serial Interface**
- **Low Sampling Aperture Error**
- **Modulator Output Option (digital filter bypass)**
- **Analog Supply: 5 V**
- **Digital Core: 1.8 V**
- **I/O Supply: 1.8 V to 3.3 V**
- **Currently available in KGD chiptray option**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range**[1]
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**
- **Vibration/Modal Analysis**
- **Multi-Channel Data Acquisition**
- **Acoustics/Dynamic Strain Gauges**
- **Pressure Sensors**

DESCRIPTION

Based on the single-channel ADS1271, the ADS1278 (octal) is a 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with data rates up to 128 k samples per second (SPS), allowing simultaneous sampling of eight channels.

Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, they have limited signal bandwidth and are mostly suited for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1278 combines these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. These ADCs provide a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005 dB of ripple.

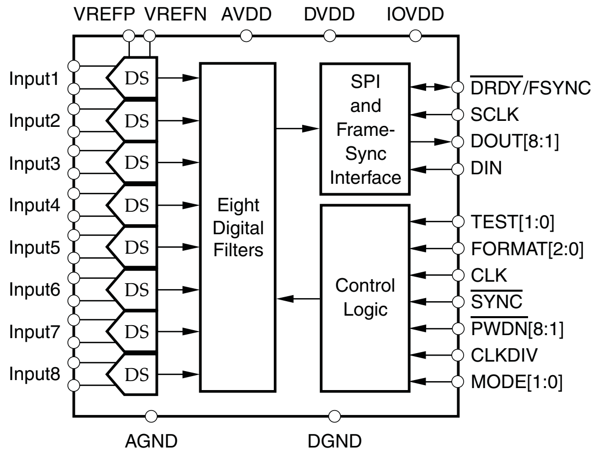
Four operating modes allow for optimization of speed, resolution, and power. All operations are controlled directly by pins; there are no registers to program. The device is fully specified over the extended industrial range (–55°C to 210°C) and is available in KGD Chiptray option.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009, Texas Instruments Incorporated



ADS1278

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE (BARE DIE)(2)	ORDERABLE PART NUMBER
–55°C to 210°C	CHIPTRAY	ADS1278SKGDA

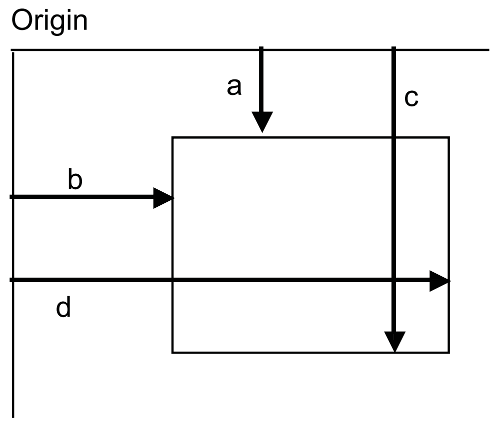
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

 Copyright © 2009, Texas Instruments Incorporated

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon with backgrind	GND	AlCu



Bond Pad Coordinates in Microns - Rev A[(1)]

DISCRIPTION	PAD NUMBER	a	b	c	d
Do not connect	1	5.00	4455.65	70.00	4520.65
AINP2	2	5.00	4355.65	70.00	4420.65
AINN2	3	5.00	4255.65	70.00	4320.65
Do not connect	4	5.00	4155.65	70.00	4220.65
Do not connect	5	5.00	4038.30	70.00	4103.30
AINP1	6	5.00	3938.30	70.00	4003.30
AINN1	7	5.00	3838.30	70.00	3903.30
Do not connect	8	5.00	3738.30	70.00	3803.30
AVDD	9	5.00	3373.30	70.00	3678.30
AGND	10	5.00	3033.30	70.00	3338.30
Do not connect	11	5.00	2853.30	70.00	2998.30
DGND	12	5.00	1911.65	70.00	1976.65
TEST0	13	5.00	1760.45	70.00	1825.45
Do not connect	14	5.00	1648.95	70.00	1713.95
TEST1	15	5.00	1536.60	70.00	1601.60
CLKDIV	16	5.00	1385.40	70.00	1450.40
$\overline{\text{SYNC}}$	17	5.00	1234.20	70.00	1299.20
DIN	18	5.00	1083.00	70.00	1148.00
DOUT8	19	5.00	780.60	70.00	845.60
DOUT7	20	5.00	629.40	70.00	694.40
DOUT6	21	5.00	478.20	70.00	543.20
DOUT5	22	5.00	275.80	70.00	340.80
DOUT4	23	275.80	5.00	340.80	70.00
DOUT3	24	745.40	5.00	810.40	70.00
DOUT2	25	1099.30	5.00	1164.30	70.00
DOUT1	26	1250.50	5.00	1315.50	70.00
DGND	27	1525.25	5.00	1590.25	70.00
IOVDD	28	1691.00	5.00	1756.00	70.00

(1) For singal descriptions see the Pin Descriptions table.

Copyright © 2009, Texas Instruments Incorporated

Bond Pad Coordinates in Microns - Rev A (continued)

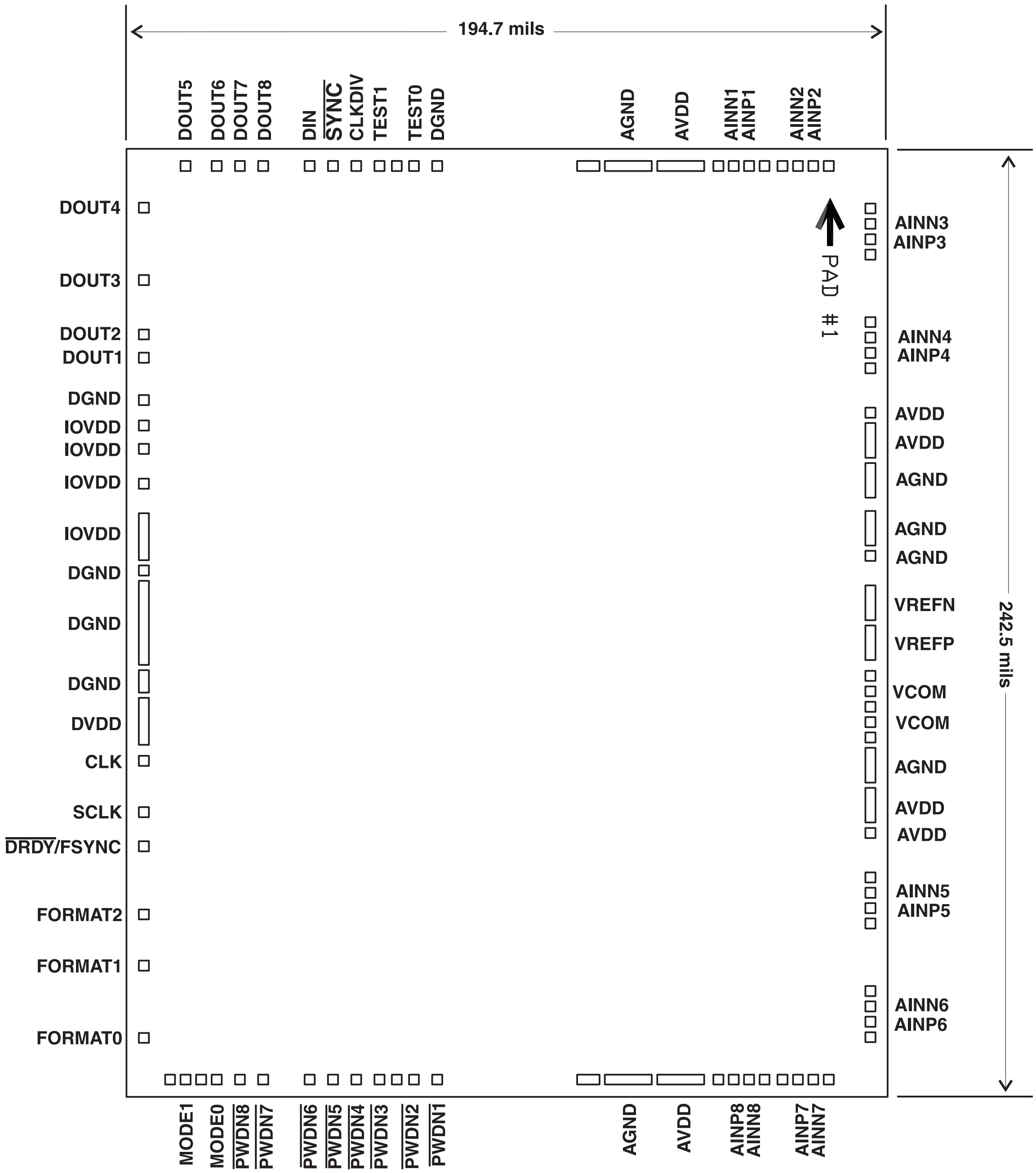
DISCRIPTION	PAD NUMBER	a	b	c	d
IOVDD	29	1842.20	5.00	1907.20	70.00
IOVDD	30	2068.10	5.00	2133.10	70.00
IOVDD	31	2292.45	5.00	2597.45	70.00
DGND	32	2632.45	5.00	2697.45	70.00
DGND	33	2732.45	5.00	3277.45	70.00
DGND	34	3312.45	5.00	3457.45	70.00
DVDD	35	3492.45	5.00	3797.45	70.00
CLK	36	3869.40	5.00	3934.40	70.00
SCLK	37	4201.90	5.00	4266.90	70.00
$\overline{\text{DRDY}}$/FSYNC	38	4423.90	5.00	4488.90	70.00
FORMAT2	39	4866.90	5.00	4931.90	70.00
FORMAT1	40	5199.40	5.00	5264.40	70.00
FORMAT0	41	5669.00	5.00	5734.00	70.00
MODE1	42	5939.80	275.80	6004.80	340.80
MODE0	43	5939.80	478.20	6004.80	543.20
$\overline{\text{PWDN8}}$	44	5939.80	629.40	6004.80	694.40
$\overline{\text{PWDN7}}$	45	5939.80	780.60	6004.80	845.60
$\overline{\text{PWDN6}}$	46	5939.80	1083.00	6004.80	1148.00
$\overline{\text{PWDN5}}$	47	5939.80	1234.20	6004.80	1299.20
$\overline{\text{PWDN4}}$	48	5939.80	1385.40	6004.80	1450.40
$\overline{\text{PWDN3}}$	49	5939.80	1536.60	6004.80	1601.60
Do not connect	50	5939.80	1648.95	6004.80	1713.95
$\overline{\text{PWDN2}}$	51	5939.80	1760.45	6004.80	1825.45
$\overline{\text{PWDN1}}$	52	5939.80	1911.65	6004.80	1976.65
Do not connect	53	5939.80	2853.30	6004.80	2998.30
AGND	54	5939.80	3033.30	6004.80	3338.30
AVDD	55	5939.80	3373.30	6004.80	3678.30
Do not connect	56	5939.80	3738.30	6004.80	3803.30
AINP8	57	5939.80	3838.30	6004.80	3903.30
AINN8	58	5939.80	3938.30	6004.80	4003.30
Do not connect	59	5939.80	4038.30	6004.80	4103.30
Do not connect	60	5939.80	4155.65	6004.80	4220.65
AINP7	61	5939.80	4255.65	6004.80	4320.65
AINN7	62	5939.80	4355.65	6004.80	4420.65
Do not connect	63	5939.80	4455.65	6004.80	4520.65
Do not connect	64	5664.20	4726.45	5729.20	4791.45
AINP6	65	5564.20	4726.45	5629.20	4791.45
AINN6	66	5464.20	4726.45	5529.20	4791.45
Do not connect	67	5364.20	4726.45	5429.20	4791.45
Do not connect	68	4925.95	4726.45	4990.95	4791.45
AINP5	69	4825.95	4726.45	4890.95	4791.45
AINN5	70	4725.95	4726.45	4790.95	4791.45
Do not connect	71	4625.95	4726.45	4690.95	4791.45
AVDD	72	4337.40	4726.45	4402.40	4791.45
AVDD	73	4077.40	4726.45	4302.40	4791.45
AGND	74	3817.40	4726.45	4042.40	4791.45
Do not connect	75	3717.40	4726.45	3782.40	4791.45

Copyright © 2009, Texas Instruments Incorporated

Bond Pad Coordinates in Microns - Rev A (continued)

DISCRIPTION	PAD NUMBER	a	b	c	d
VCOM	76	3617.40	4726.45	3682.40	4791.45
Do not connect	77	3517.40	4726.45	3582.40	4791.45
VCOM	78	3417.40	4726.45	3482.40	4791.45
Do not connect	79	3317.40	4726.45	3382.40	4791.45
VREFP	80	3022.40	4726.45	3247.40	4791.45
VREFN	81	2762.40	4726.45	2987.40	4791.45
AGND	82	2537.40	4726.45	2602.40	4791.45
AGND	83	2277.40	4726.45	2502.40	4791.45
AGND	84	1967.40	4726.45	2192.40	4791.45
AVDD	85	1707.40	4726.45	1932.40	4791.45
AVDD	86	1607.40	4726.45	1672.40	4791.45
Do not connect	87	1318.85	4726.45	1383.85	4791.45
AINP4	88	1218.85	4726.45	1283.85	4791.45
AINN4	89	1118.85	4726.45	1183.85	4791.45
Do not connect	90	1018.85	4726.45	1083.85	4791.45
Do not connect	91	580.60	4726.45	645.60	4791.45
AINP3	92	480.60	4726.45	545.60	4791.45
AINN3	93	380.60	4726.45	445.60	4791.45
Do not connect	94	280.60	4726.45	345.60	4791.45
Do not connect	95	5939.80	377.00	6004.80	442.00
Do not connect	96	5939.80	175.80	6004.80	240.80

Copyright © 2009, Texas Instruments Incorporated



Copyright © 2009, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted(1)

			UNIT
AVDD to AGND		–0.3 to 6.0	V
DVDD, IOVDD to DGND		–0.3 to 3.6	V
AGND to DGND		–0.3 to 0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog input to AGND		–0.3 to AVDD + 0.3	V
Digital input or output to DGND		–0.3 to DVDD + 0.3	V
Operating temperature range		–55 to 210	°C
Storage temperature range		–60 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –55°C to 210°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C MIN	TYP	MAX	T_A = 210°C(1) MIN	TYP	MAX	UNIT
Analog Inputs									
Full-scale input voltage (FSR(2))		V_{IN} = (AINP – AINN)		$\pm V_{REF}$			$\pm V_{REF}$		V
Absolute input voltage		AINP or AINN to AGND	AGND – 0.1		AVDD + 0.1	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage (V_{CM})		V_{CM} = (AINP + AINN)/2		2.5			2.5		V
Differential input impedance	High-Speed mode			14			14		kΩ
	High-Resolution mode			14			14		kΩ
	Low-Power mode			28			28		kΩ
	Low-Speed mode			140			140		kΩ
DC Performance									
Resolution		No missing codes	24						Bits
Data rate (f_{DATA})	High-Speed mode	f_{CLK} = 32.768MHz(3)		128,000			128,000		SPS
		f_{CLK} = 27MHz		105,469			105,469		SPS(4)
	High-Resolution mode			52,734			52,734		SPS
	Low-Power mode			52,734			52,734		SPS
	Low-Speed mode			10,547			10,547		SPS
Integral nonlinearity (INL)(5)		Differential input, V_{CM} = 2.5V		±0.0003	±0.0012			±0.0014	% FSR(2)
Offset error				0.25	2			2	mV
Offset drift				0.8					µV/°C
Gain error				0.1	0.5			0.5	% FSR
Gain drift				1.3					ppm/°C
Noise	High-Speed mode	Shorted input		8.5	21			21	µV, rms
	High-Resolution mode	Shorted input		5.5	13			13	µV, rms
	Low-Power mode	Shorted input		8.5	21			21	µV, rms
	Low-Speed mode	Shorted input		8.0	21			21	µV, rms

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) FSR = full-scale range = $2V_{REF}$.
(3) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes. When f_{CLK} > 27MHz, operation is limited to Frame-Sync mode and $V_{REF} \leq 2.6V$.
(4) SPS = samples per second.
(5) Best fit method.

Copyright © 2009, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –55°C to 210°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C MIN	TYP	MAX	T_A = 210°C(1) MIN	TYP	MAX	UNIT
Common-mode rejection		f_{CM} = 60Hz	90	108		90			dB
Power-supply rejection	AVDD	f_{PS} = 60Hz		80			80		dB
	DVDD			85			85		dB
	IOVDD			105			102		dB
V_{COM} output voltage		No load		AVDD/2			AVDD/2		V
AC Performance									
Crosstalk		f = 1kHz, –0.5dBFS(6)		–107					dB
Signal-to-noise ratio (SNR)(7) (unweighted)	High-Speed mode		98	106		96			dB
	High-Resolution mode	V_{REF} = 2.5V	101	110		101			dB
		V_{REF} = 3V		111					dB
	Low-Power mode		98	106		97			dB
	Low-Speed mode		98	107		98			dB
Total harmonic distortion (THD)(8)		V_{IN} = 1kHz, –0.5dBFS		–108	–96			-96	dB
Spurious-free dynamic range				109					dB
Passband ripple				±0.005					dB
Passband				0.453 f_{DATA}					Hz
–3dB Bandwidth				0.49 f_{DATA}					Hz
Stop band attenuation	High-Resolution mode		95						dB
	All other modes		100						
Stop band	High-Resolution mode		0.547 f_{DATA}		127.453 f_{DATA}				Hz
	All other modes		0.547 f_{DATA}		63.453 f_{DATA}				Hz
Group delay	High-Resolution mode			39/f_{DATA}					s
	All other modes			38/f_{DATA}					s
Settling time (latency)	High-Resolution mode	Complete settling		78/f_{DATA}					s
	All other modes	Complete settling		76/f_{DATA}					s
Voltage Reference Inputs									
Reference input voltage (V_{REF}) (V_{REF} = VREFP – VREFN)		f_{CLK} = 27MHz	0.5	2.5	3.1	0.5	2.5	3.1	V
		f_{CLK} = 32.768MHz(9)	0.5	2.5	2.6	0.5	2.5	2.6	V
Negative reference input (VREFN)			AGND – 0.1		AGND + 0.1	AGND – 0.1		AGND + 0.1	V
Positive reference input (VREFP)			VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
Reference Input impedance	High-Speed mode			0.65			0.65		kΩ
	High-Resolution mode			0.65			0.65		kΩ
	Low-Power mode			1.3			1.3		kΩ
	Low-Speed mode			6.5			6.5		kΩ
Digital Input/Output (IOVDD = 1.8V to 3.6V)									
V_{IH}			0.7 IOVDD		IOVDD	0.7 IOVDD		IOVDD	V
V_{IL}			DGND		0.3 IOVDD	DGND		0.3 IOVDD	V
V_{OH}		I_{OH} = 4mA	0.8 IOVDD		IOVDD	0.8 IOVDD		IOVDD	V

(6) Worst-case channel crosstalk between one or more channels.
(7) Minimum SNR is ensured by the limit of the *DC noise* specification.
(8) THD includes the first nine harmonics of the input signal; Low-Speed mode includes the first five harmonics.
(9) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes. When f_{CLK} > 27MHz, operation is limited to Frame-Sync mode and V_{REF} ≤ 2.6V.

 Copyright © 2009, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –55°C to 210°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}		I_{OL} = 4mA	DGND		0.2 IOVDD	DGND		0.2 IOVDD	V
Input leakage		0 < $V_{IN\ DIGITAL}$ < IOVDD			±10				µA
Master clock rate (f_{CLK})		High-Speed mode[9]	0.1		32.768	0.1		32.768	MHz
		Other modes	0.1		27	0.1		27	MHz
Power Supply									
AVDD			4.75	5	5.25	4.75	5	5.25	V
DVDD			1.65	1.8	1.95	1.65	1.8	1.95	V
IOVDD			1.65		3.6	1.65		3.6	V
Power-down current	AVDD			1	10		65		µA
	DVDD			1	50		200		µA
	IOVDD			1	11		25		µA
AVDD current	High-Speed mode			97	145		135	185	mA
	High-Resolution mode			97	145		135	185	mA
	Low-Power mode			44	64		60	84	mA
	Low-Speed mode			9	14		12	22	mA
DVDD current	High-Speed mode			23	30		24	31	mA
	High-Resolution mode			16	20		17	20	mA
	Low-Power mode			12	17		13	17	mA
	Low-Speed mode			2.5	4.5		3	5	mA
IOVDD current	High-Speed mode			0.25	1		0.3	1.15	mA
	High-Resolution mode			0.125	0.6		0.2	0.75	mA
	Low-Power mode			0.125	0.6		0.2	0.75	mA
	Low-Speed mode			0.035	0.3		0.1	0.45	mA
Power dissipation	High-Speed mode			530	785			985	mW
	High-Resolution mode			515	765			985	mW
	Low-Power mode			245	355			455	mW
	Low-Speed mode			50	80			120	mW

PIN DESCRIPTIONS

PIN NAME	FUNCTION	DESCRIPTION
AGND	Analog ground	Analog ground; connect to DGND using a single plane.
AINP1	Analog input	AINP[8:1] Positive analog input, channels 8 through 1.
AINP2	Analog input	
AINP3	Analog input	
AINP4	Analog input	
AINP5	Analog input	
AINP6	Analog input	
AINP7	Analog input	
AINP8	Analog input	

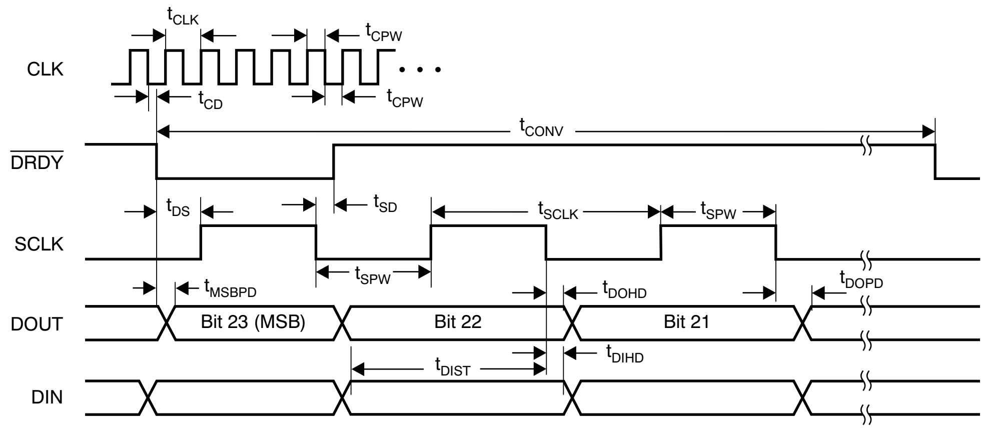
Copyright © 2009, Texas Instruments Incorporated

PIN DESCRIPTIONS (continued)

PIN NAME	FUNCTION	DESCRIPTION
AINN1	Analog input	AINN[8:1] Negative analog input, channels 8 through 1.
AINN2	Analog input	
AINN3	Analog input	
AINN4	Analog input	
AINN5	Analog input	
AINN6	Analog input	
AINN7	Analog input	
AINN8	Analog input	
AVDD	Analog power supply	Analog power supply (4.75V to 5.25V).
VCOM	Analog output	AVDD/2 Unbuffered voltage output.
VREFN	Analog input	Negative reference input.
VREFP	Analog input	Positive reference input.
CLK	Digital input	Master clock input.
CLKDIV	Digital input	CLK input divider control: 1 = 32.768MHz (High-Speed mode only) / 27MHz 0 = 13.5MHz (low-power) / 5.4MHz (low-speed)
DGND	Digital ground	Digital ground power supply.
DIN	Digital input	Daisy-chain data input.
DOUT1	Digital output	DOUT1 is TDM data output (TDM mode). DOUT[8:1] Data output for channels 8 through 1.
DOUT2	Digital output	
DOUT3	Digital output	
DOUT4	Digital output	
DOUT5	Digital output	
DOUT6	Digital output	
DOUT7	Digital output	
DOUT8	Digital output	
$\overline{\text{DRDY}}$/ FSYNC	Digital input/output	Frame-Sync protocol: frame clock input; SPI protocol: data ready output.
DVDD	Digital power supply	Digital core power supply (+1.65V to +1.95V).
FORMAT0	Digital input	FORMAT[2:0] Selects Frame-Sync/SPI protocol, TDM/discrete data outputs, fixed/dynamic position TDM data, and modulator mode/normal operating mode.
FORMAT1	Digital input	
FORMAT2	Digital input	
IOVDD	Digital power supply	I/O power supply (+1.65V to +3.6V).
MODE0	Digital input	MODE[1:0] Selects High-Speed, High-Resolution, Low-Power, or Low-Speed mode operation.
MODE1	Digital input	
$\overline{\text{PWDN1}}$	Digital input	$\overline{\text{PWDN}}$[8:1] Power-down control for channels 8 through 1.
$\overline{\text{PWDN2}}$	Digital input	
$\overline{\text{PWDN3}}$	Digital input	
$\overline{\text{PWDN4}}$	Digital input	
$\overline{\text{PWDN5}}$	Digital input	
$\overline{\text{PWDN6}}$	Digital input	
$\overline{\text{PWDN7}}$	Digital input	
$\overline{\text{PWDN8}}$	Digital input	
SCLK	Digital input/output	Serial clock input, Modulator clock output.
$\overline{\text{SYNC}}$	Digital input	Synchronize input (all channels).
TEST0	Digital input	TEST[1:0] Test mode select: 00 = Normal operation, 01 = Do not use 11 = Test mode, 10 = Do not use
TEST1	Digital input	

Copyright © 2009, Texas Instruments Incorporated

TIMING CHARACTERISTICS: SPI FORMAT



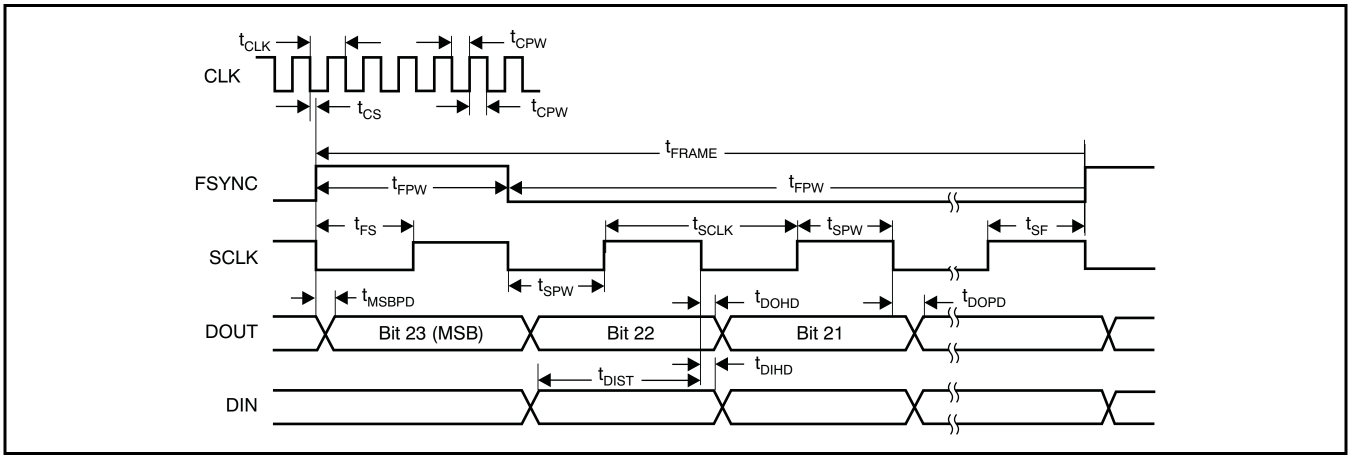
TIMING REQUIREMENTS: SPI FORMAT(1)

For T_A = –40°C to 105°C, IOVDD = 1.65 V to 3.6 V, and DVDD = 1.65 V to 1.95 V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)(2)	37		10,000	ns
t_{CPW}	CLK positive or negative pulse width	15			ns
t_{CONV}	Conversion period ($1/f_{DATA}$)(3)	256		2560	t_{CLK}
t_{CD}(4)	Falling edge of CLK to falling edge of DRDY		22		ns
t_{DS}(4)	Falling edge of DRDY to rising edge of first SCLK to retrieve data	1			t_{CLK}
t_{MSBPD}	DRDY falling edge to DOUT MSB valid (propagation delay)			16	ns
t_{SD}(4)	Falling edge of SCLK to rising edge of DRDY		18		ns
t_{SCLK}(5)	SCLK period	1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width	0.4			t_{CLK}
t_{DOHD}(4)(6)	SCLK falling edge to new DOUT invalid (hold time)	10			ns
t_{DOPD}(4)	SCLK falling edge to new DOUT valid (propagation delay)			32	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)	6			ns
t_{DIHD}(6)	Old DIN valid to falling edge of SCLK (hold time)	6			ns

(1) Timing parameters are characerized or guranteed by design for specified temperature but not production tested.
(2) f_{CLK} = 27MHz maximum.
(3) Depends on MODE[1:0] and CLKDIV selection. See Table 6 (f_{CLK}/f_{DATA}).
(4) Load on DRDY and DOUT = 20pF.
(5) For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc.
(6) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4ns.

TIMING CHARACTERISTICS: FRAME-SYNC FORMAT



TIMING REQUIREMENTS: FRAME-SYNC FORMAT[1]

For T_A = –40°C to 105°C, IOVDD = 1.65 V to 3.6 V, and DVDD = 1.65 V to 1.95 V.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	All modes	37		10,000	ns
		High-Speed mode only	30.5			ns
t_{CPW}	CLK positive or negative pulse width		12			ns
t_{CS}	Falling edge of CLK to falling edge of SCLK		–0.25		0.25	t_{CLK}
t_{FRAME}	Frame period ($1/f_{DATA}$)[2]		256		2560	t_{CLK}
t_{FPW}	FSYNC positive or negative pulse width		1			t_{SCLK}
t_{FS}	Rising edge of FSYNC to rising edge of SCLK		5			ns
t_{SF}	Rising edge of SCLK to rising edge of FSYNC		5			ns
t_{SCLK}	SCLK period[3]		1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width		0.4			t_{CLK}
t_{DOHD}[4][5]	SCLK falling edge to old DOUT invalid (hold time)		10			ns
t_{DOPD}[5]	SCLK falling edge to new DOUT valid (propagation delay)				31	ns
t_{MSBPD}	FSYNC rising edge to DOUT MSB valid (propagation delay)				31	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD}[4]	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) Timing parameters are characerized or guranteed by design for specified temperature but not production tested.
(2) Depends on MODE[1:0] and CLKDIV selection. See Table 6 (f_{CLK}/f_{DATA}).
(3) SCLK must be continuously running and limited to ratios of 1, 1/2, 1/4, and 1/8 of f_{CLK}.
(4) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4 ns.
(5) Load on DOUT = 20 pF.

Copyright © 2009, Texas Instruments Incorporated

ADS1278 Operating Life Derating Chart

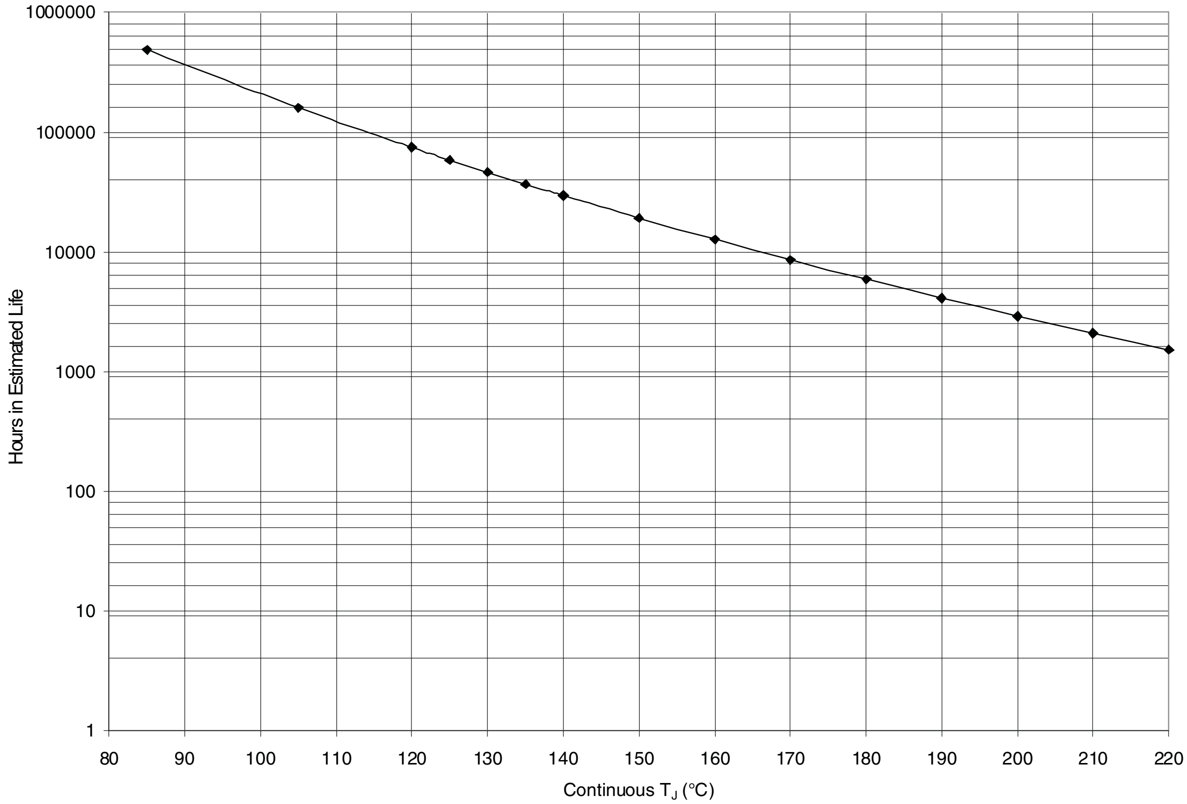


Figure 1.

Notes:

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Sillicon operating life design goal is 10 years at 110°C junction temperature.

TYPICAL CHARACTERISTICS

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

OUTPUT SPECTRUM

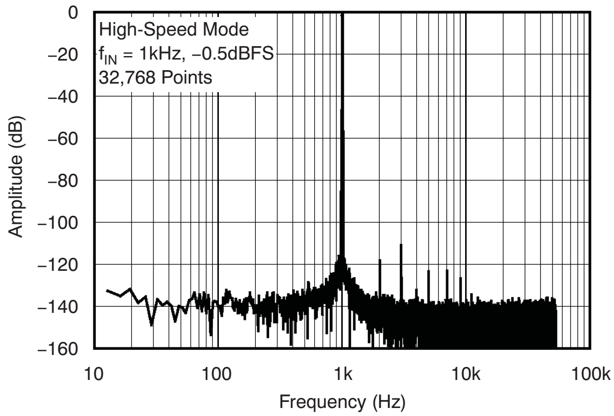


Figure 2.

OUTPUT SPECTRUM

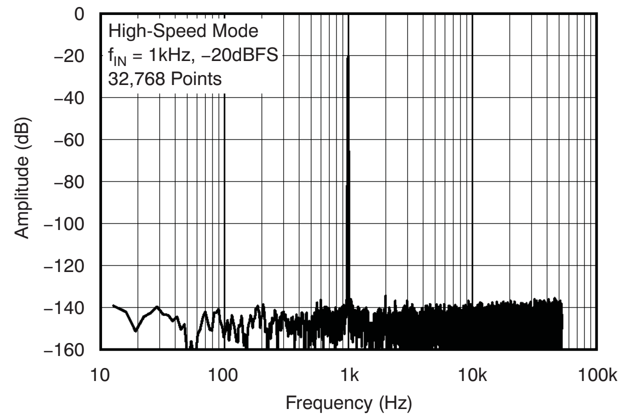


Figure 3.

OUTPUT SPECTRUM

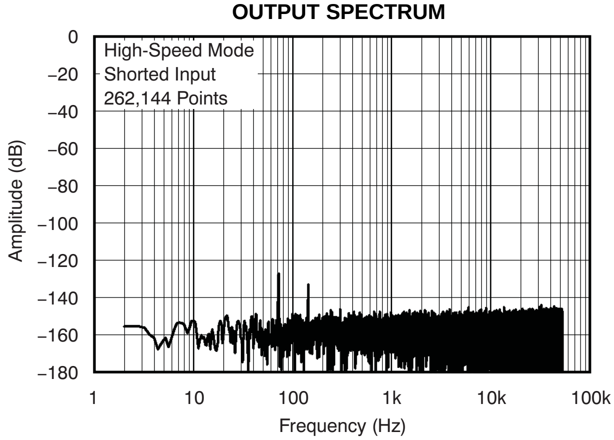


Figure 4.

NOISE HISTOGRAM

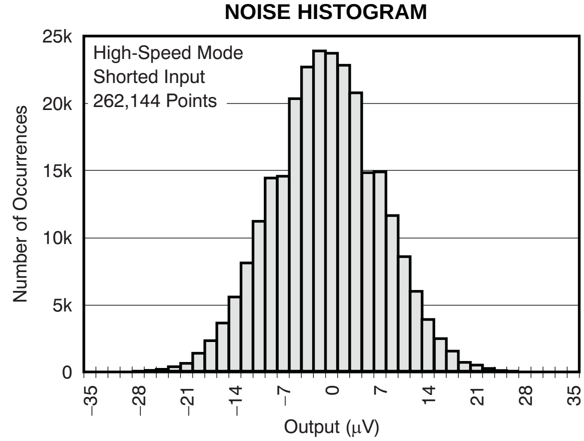


Figure 5.

OUTPUT SPECTRUM

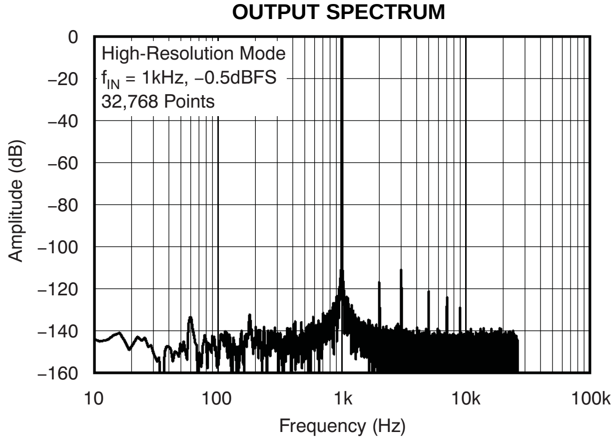


Figure 6.

OUTPUT SPECTRUM

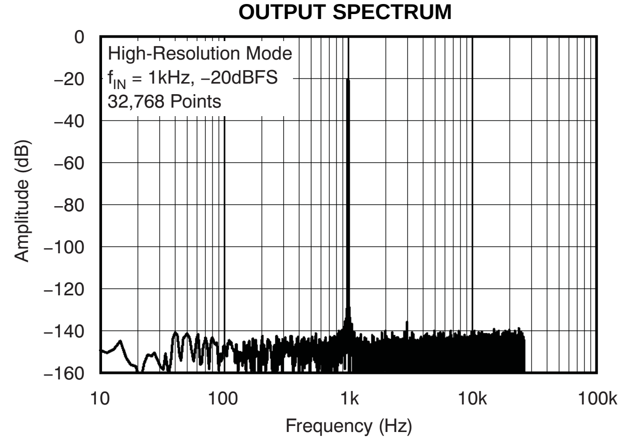


Figure 7.

 Copyright © 2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

OUTPUT SPECTRUM

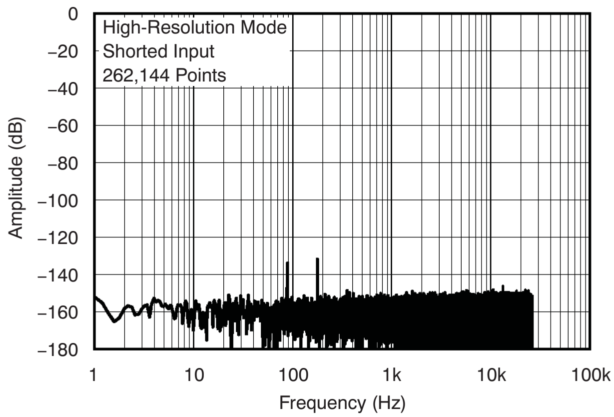


Figure 8.

NOISE HISTOGRAM

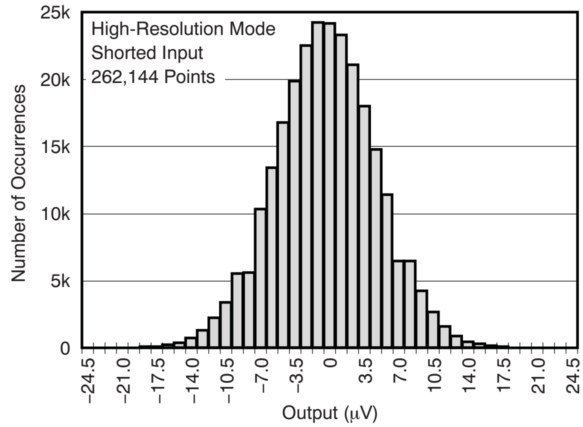


Figure 9.

OUTPUT SPECTRUM

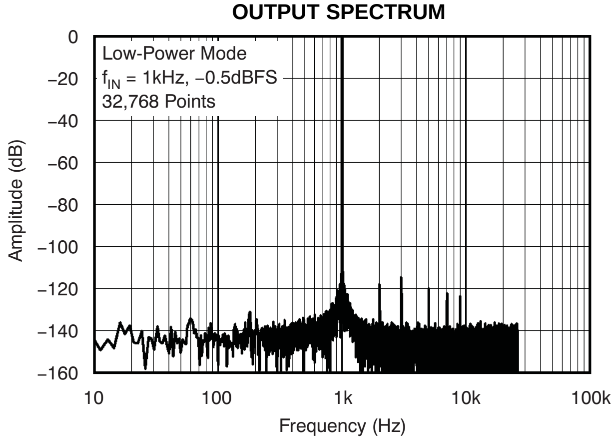


Figure 10.

OUTPUT SPECTRUM

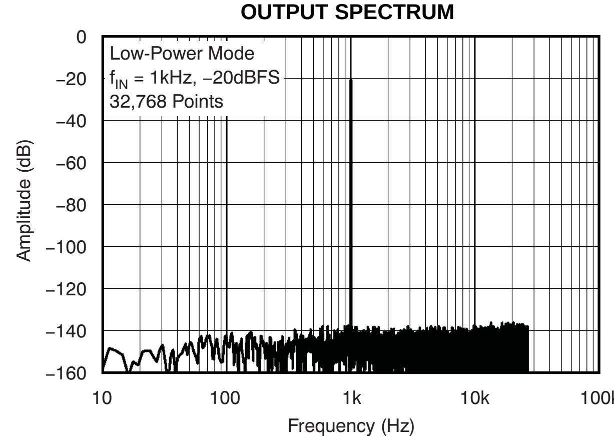


Figure 11.

OUTPUT SPECTRUM

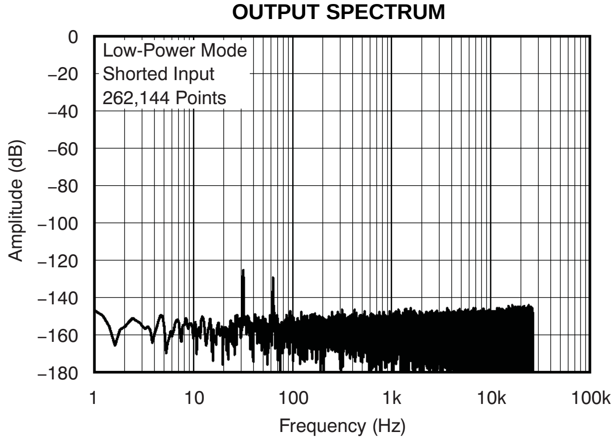


Figure 12.

NOISE HISTOGRAM

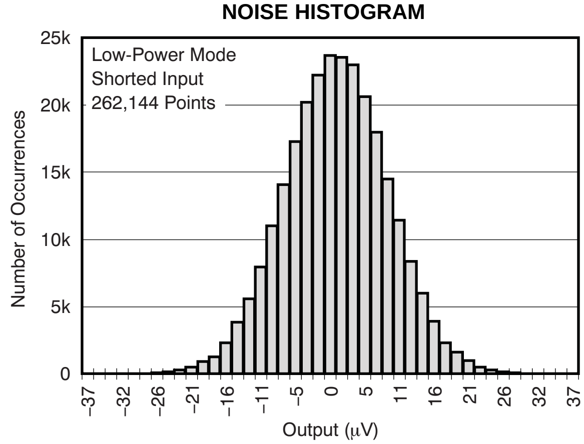


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

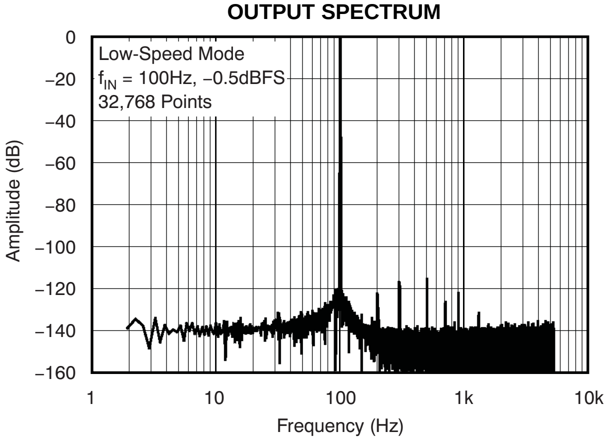


Figure 14.

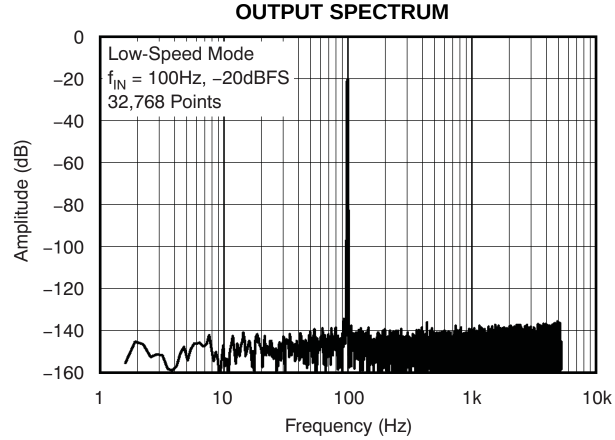


Figure 15.

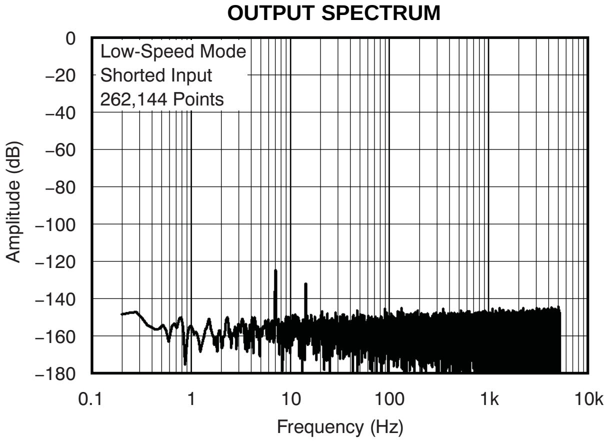


Figure 16.

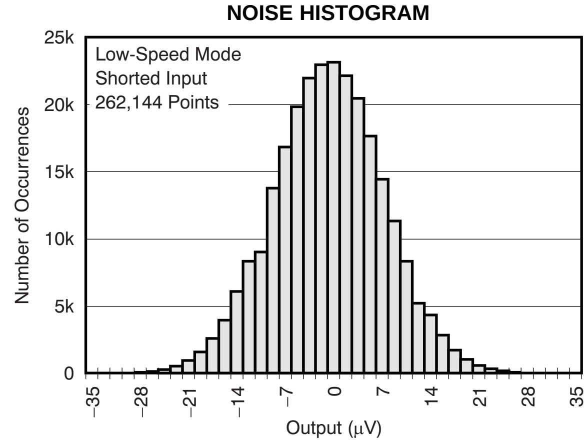


Figure 17.

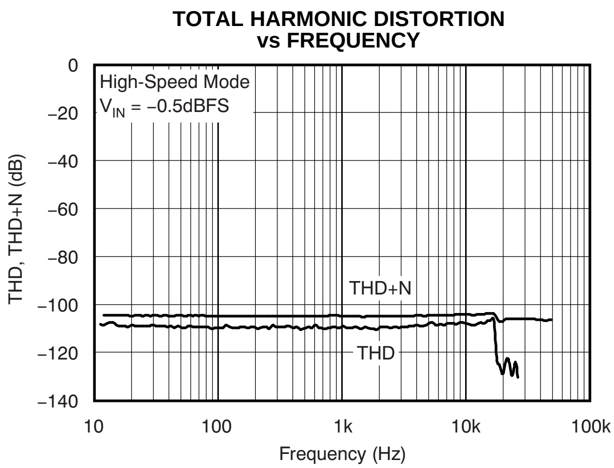


Figure 18.

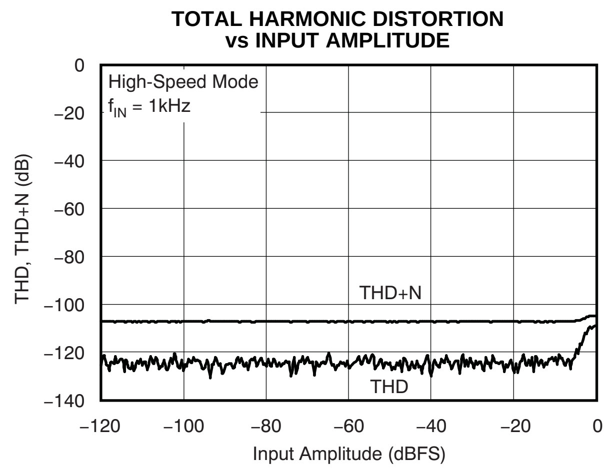


Figure 19.

 Copyright © 2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs FREQUENCY

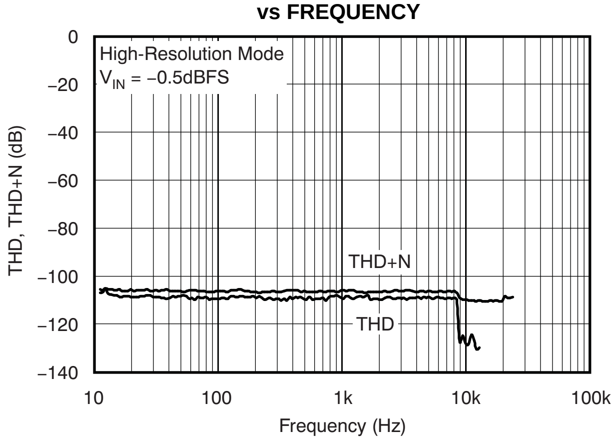


Figure 20.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

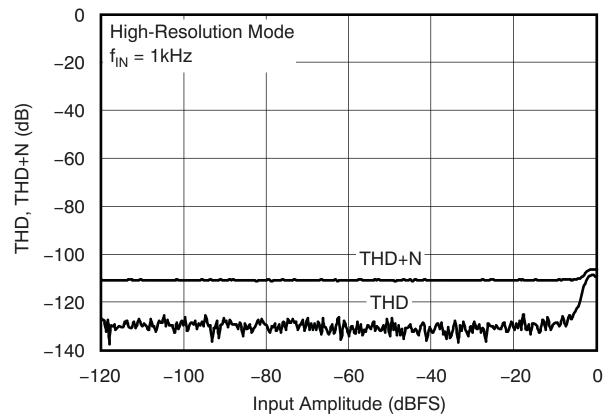


Figure 21.

TOTAL HARMONIC DISTORTION vs FREQUENCY

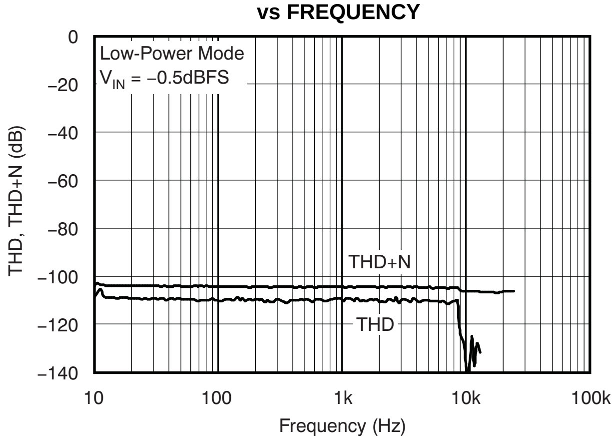


Figure 22.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

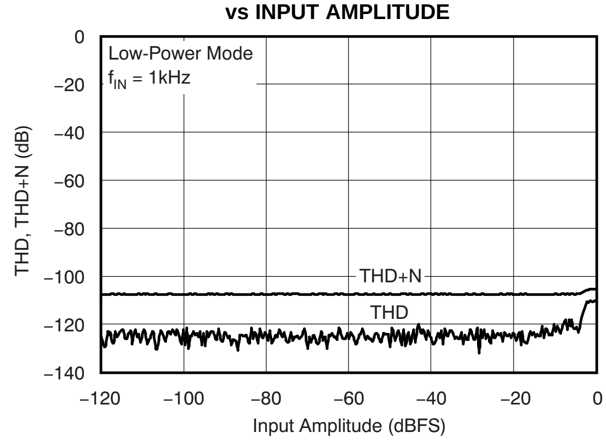


Figure 23.

TOTAL HARMONIC DISTORTION vs FREQUENCY

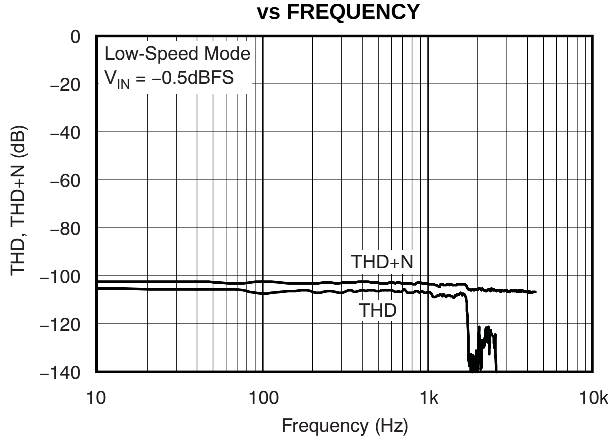


Figure 24.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

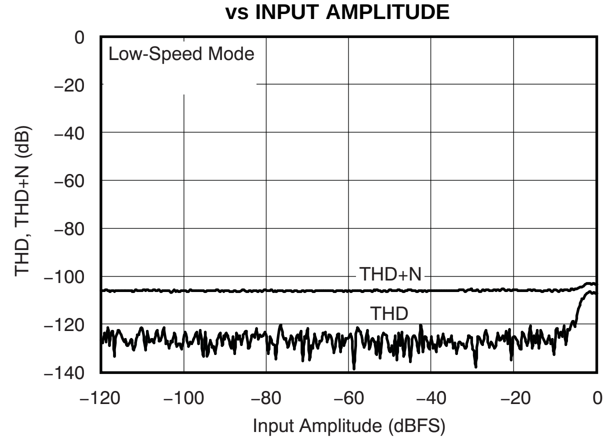


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

OFFSET DRIFT HISTOGRAM

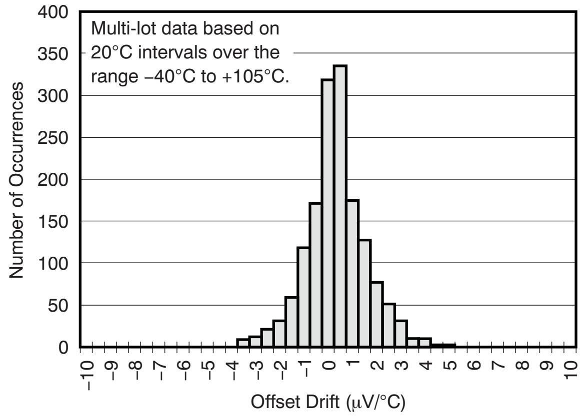


Figure 26.

GAIN DRIFT HISTOGRAM

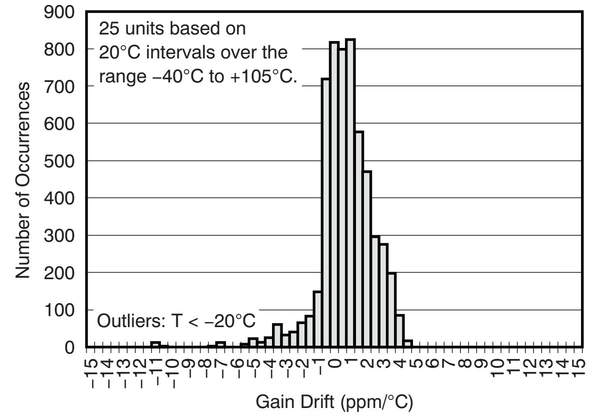


Figure 27.

OFFSET WARMUP DRIFT RESPONSE BAND

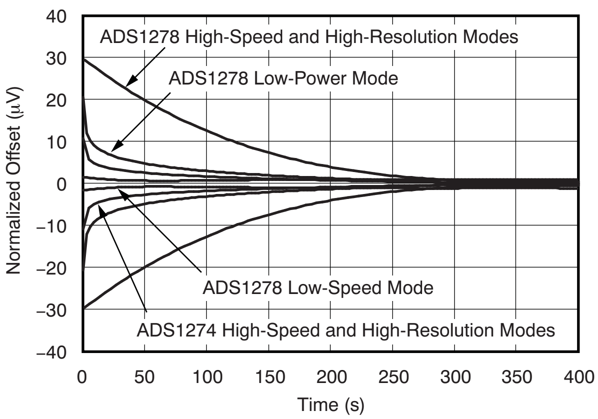


Figure 28.

GAIN WARMUP DRIFT RESPONSE BAND

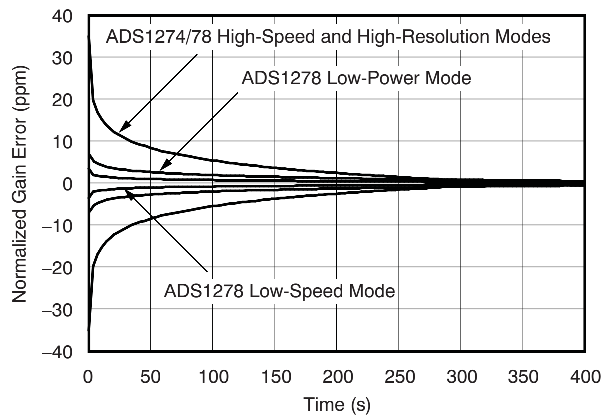


Figure 29.

OFFSET ERROR HISTOGRAM

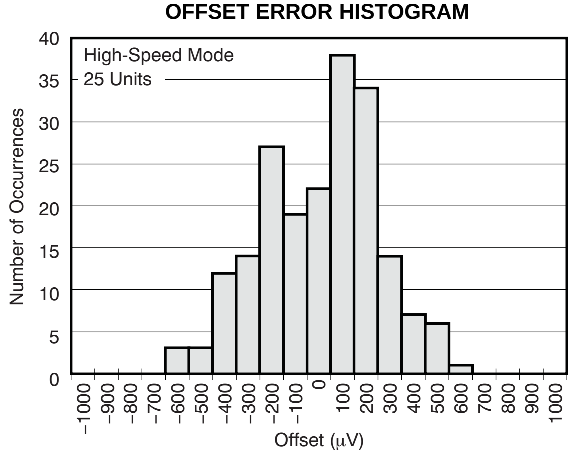


Figure 30.

GAIN ERROR HISTOGRAM

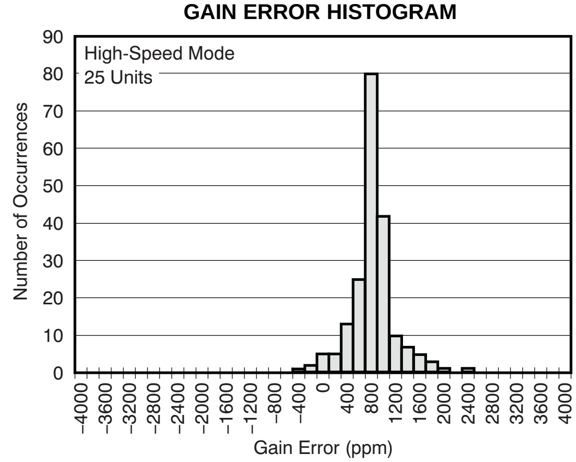


Figure 31.

 Copyright © 2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

CHANNEL GAIN MATCH HISTOGRAM

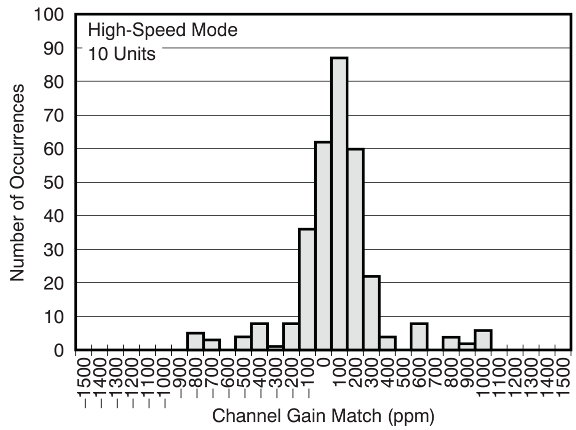


Figure 32.

CHANNEL OFFSET MATCH HISTOGRAM

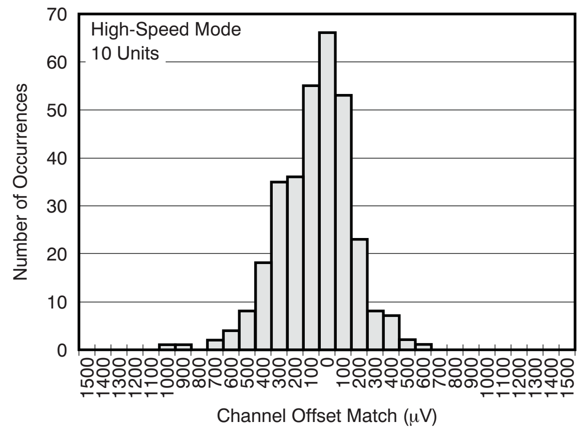


Figure 33.

OFFSET AND GAIN vs TEMPERATURE

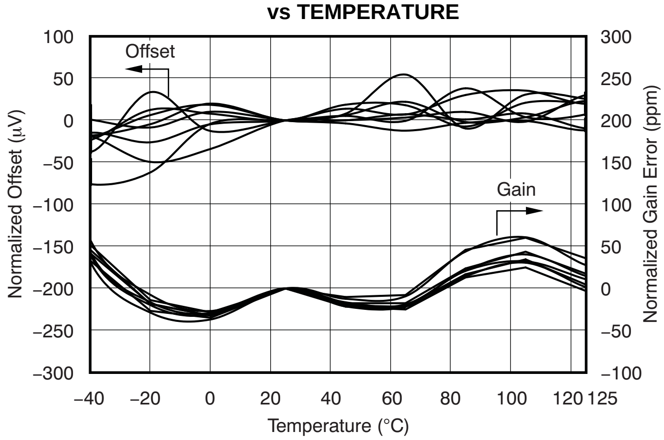


Figure 34.

VCOM VOLTAGE OUTPUT HISTOGRAM

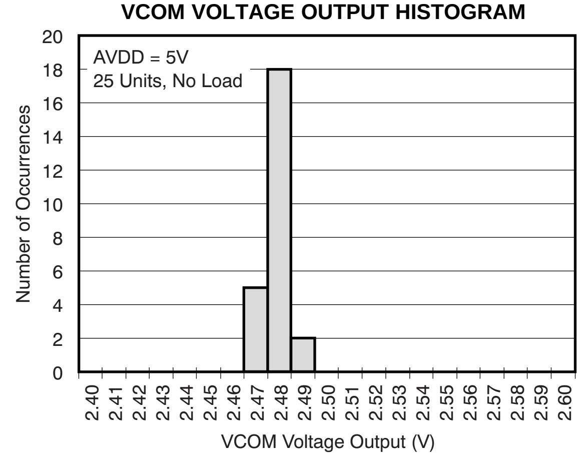


Figure 35.

SAMPLING MATCH ERROR HISTOGRAM

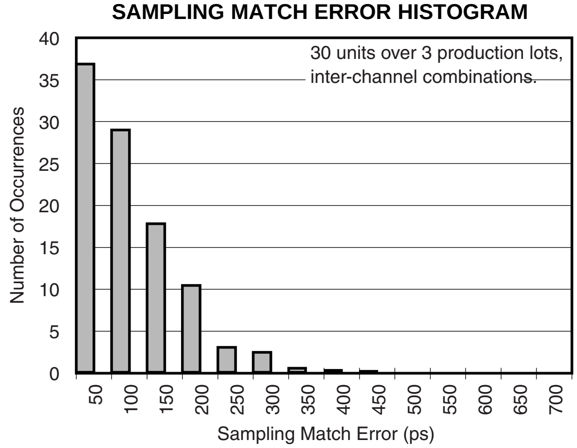


Figure 36.

REFERENCE INPUT DIFFERENTIAL IMPEDANCE vs TEMPERATURE

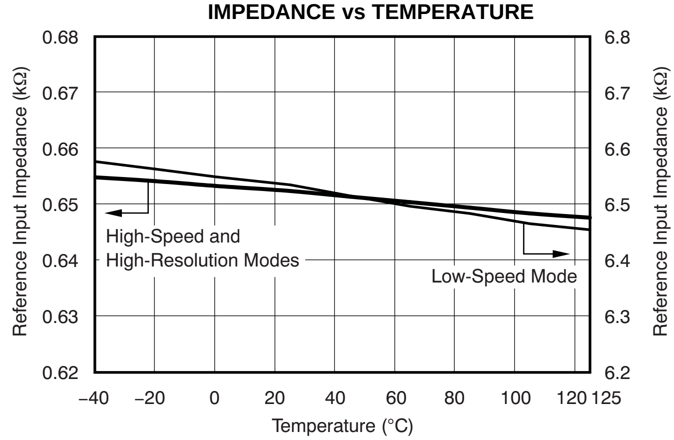


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

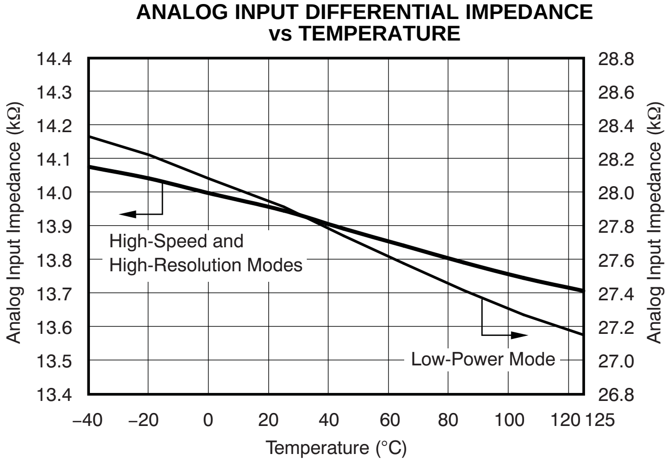


Figure 38.

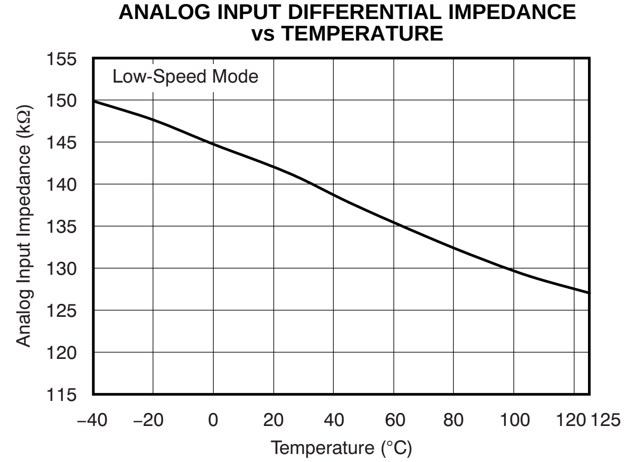


Figure 39.

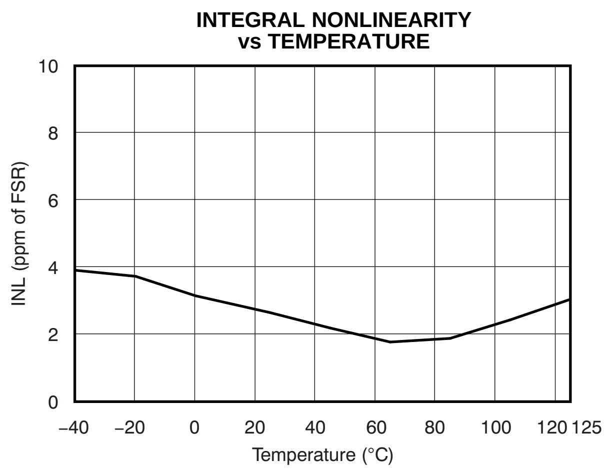


Figure 40.

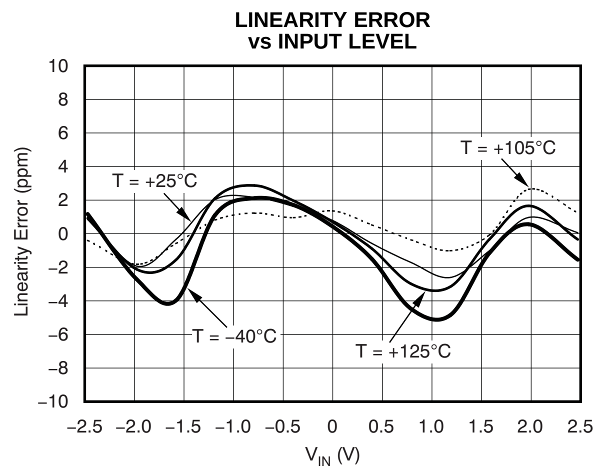


Figure 41.

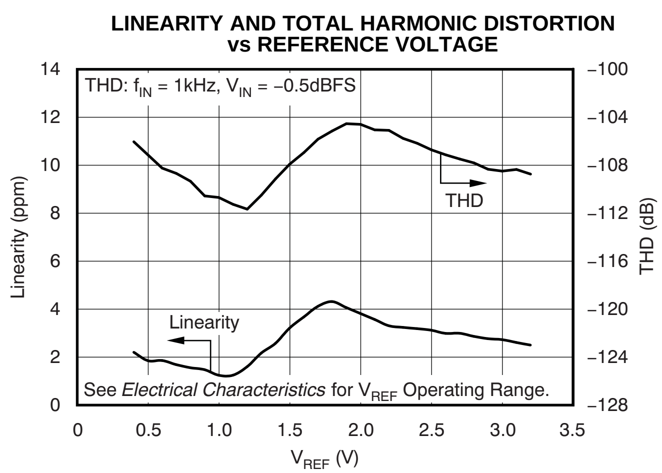


Figure 42.

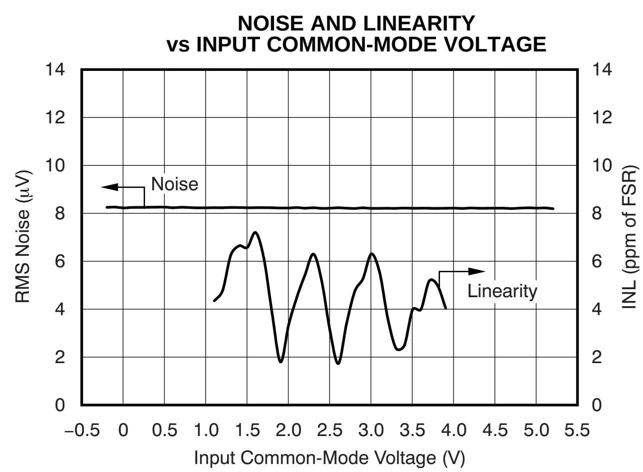


Figure 43.

Copyright © 2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

NOISE vs TEMPERATURE

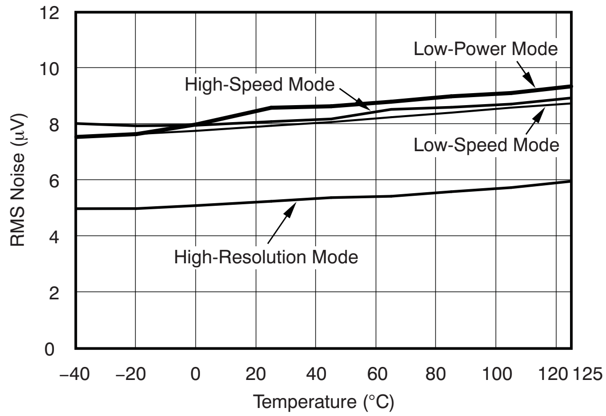


Figure 44.

NOISE vs REFERENCE VOLTAGE

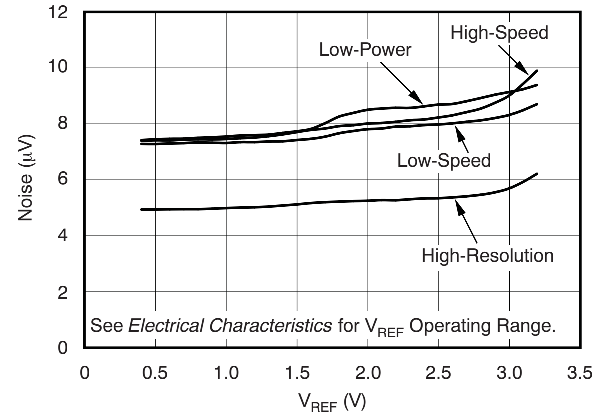


Figure 45.

TOTAL HARMONIC DISTORTION AND NOISE vs CLK

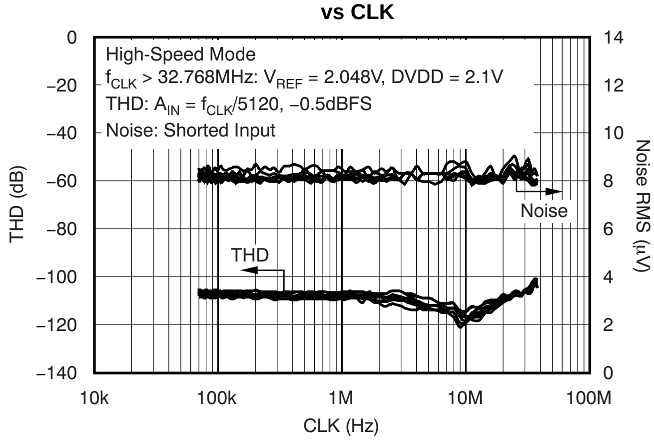


Figure 46.

COMMON-MODE REJECTION vs INPUT FREQUENCY

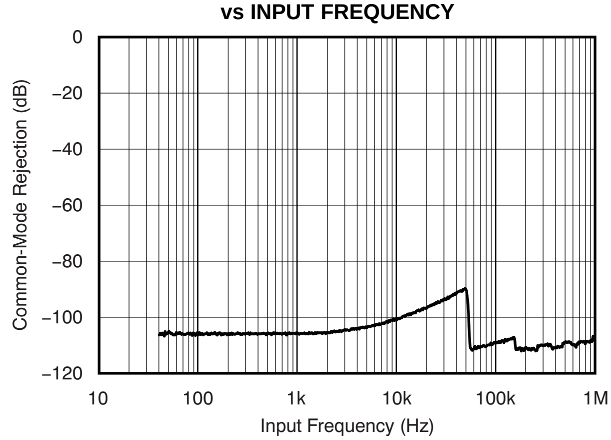


Figure 47.

POWER-SUPPLY REJECTION vs POWER-SUPPLY FREQUENCY

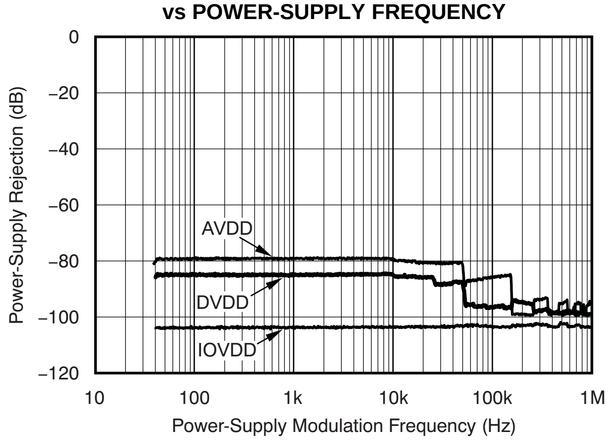


Figure 48.

AVDD CURRENT vs TEMPERATURE

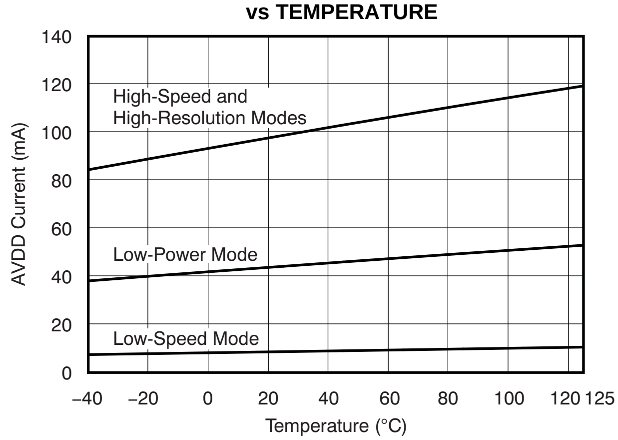


Figure 49.

Copyright © 2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

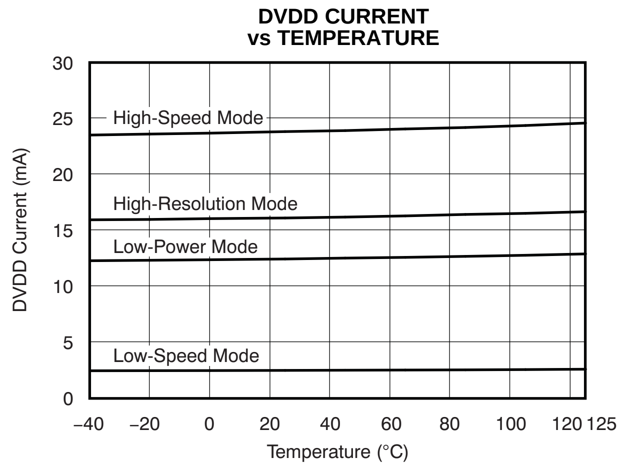


Figure 50.

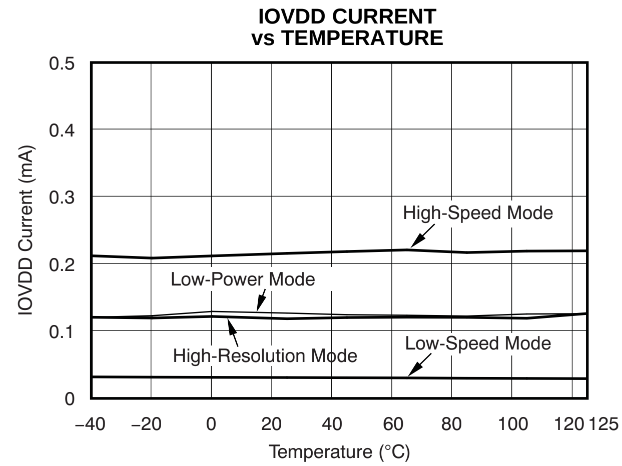


Figure 51.

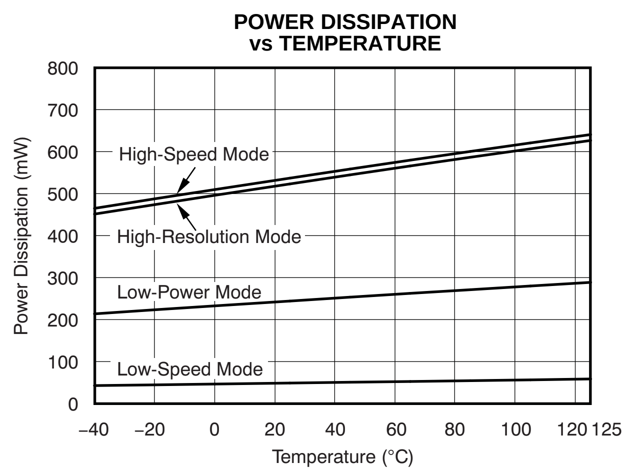


Figure 52.

 Copyright © 2009, Texas Instruments Incorporated

OVERVIEW

The ADS1278 is an octal 24-bit, delta-sigma ADC based on the single-channel ADS1271. It offers the combination of outstanding dc accuracy and superior ac performance. Figure 53 shows the block diagram. The converter is comprised of eight advanced, 6th-order, chopper-stabilized, delta-sigma modulators followed by low-ripple, linear phase FIR filters. The modulators measure the differential input signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output. To allow tradeoffs among speed, resolution, and power, four operating modes are supported: High-Speed, High-Resolution, Low-Power, and Low-Speed. Table 1 summarizes the performance of each mode.

In High-Speed mode, the maximum data rate is 128 kSPS (when operating at 128 kSPS, Frame-Sync format must be used). In High-Resolution mode, the SNR = 111dB (V_{REF} = 3.0 V); in Low-Power mode, the power dissipation is 31 mW/channel; and in Low-Speed mode, the power dissipation is only 7 mW/channel at 10.5 kSPS. The digital filters can be bypassed, enabling direct access to the modulator output.

The ADS1278 is configured by simply setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that supports both SPI and Frame-Sync formats. The ADS1278 has a daisy-chainable output and the ability to synchronize externally, so it can be used conveniently in systems requiring more than eight channels.

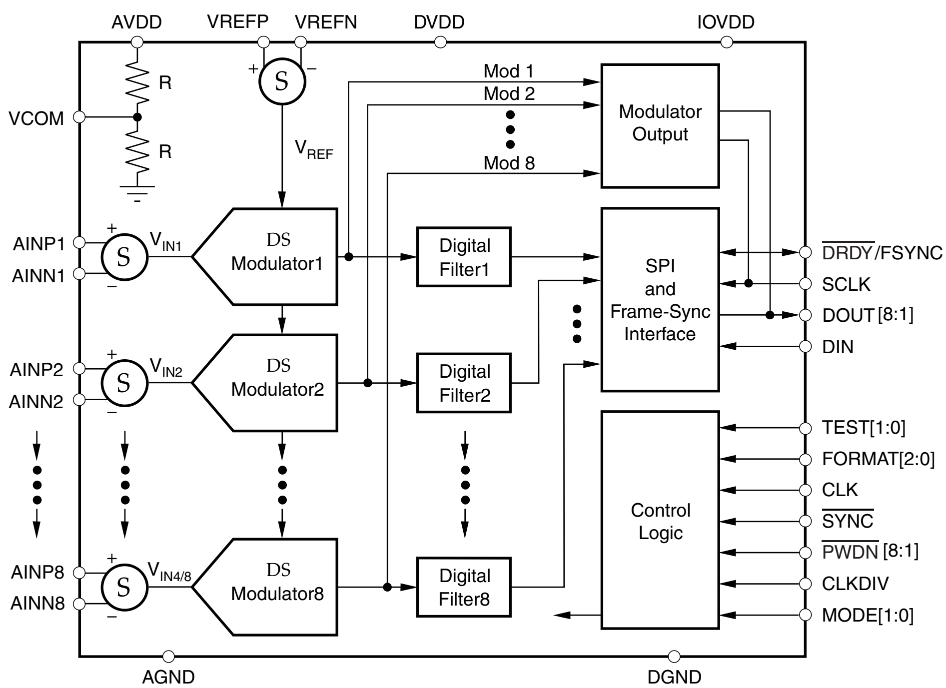


Figure 53. Block Diagram

Table 1. Operating Mode Performance Summary

MODE	MAX DATA RATE (SPS)	PASSBAND (kHz)	SNR (dB)	NOISE (μV_{RMS})	POWER/CHANNEL (mW)
High-Speed	128,000	57,984	106	8.5	70
High-Resolution	52,734	23,889	110	5.5	64
Low-Power	52,734	23,889	106	8.5	31
Low-Speed	10,547	4,798	107	8.0	7

FUNCTIONAL DESCRIPTION

The ADS1278 is a delta-sigma ADC consisting of eight independent converters that digitize eight input signals in parallel.

The converter is composed of two main functional blocks to perform the ADC conversions: the modulator and the digital filter. The modulator samples the input signal together with sampling the reference voltage to produce a 1s density output stream. The density of the output stream is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by the internal digital filter where the output conversion result is produced.

In operation, the input signal is sampled by the modulator at a high rate (typically 64x higher than the final output data rate). The quantization noise of the modulator is moved to a higher frequency range where the internal digital filter removes it. Oversampling results in very low levels of noise within the signal passband.

Since the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency is at the modulator sampling rate. This architecture greatly relaxes the requirement of external antialiasing filters because of the high modulator sampling rate.

SAMPLING APERTURE MATCHING

The ADS1278 converter operates from the same CLK input. The CLK input controls the timing of the modulator sampling instant. The converter is designed such that the sampling skew, or modulator sampling aperture match between channels, is controlled. Furthermore, the digital filters are synchronized to start the convolution phase at the same modulator clock cycle. This design results in excellent phase match among the ADS1278 channels.

Figure 36 shows the inter-device channel sample matching for the ADS1278.

FREQUENCY RESPONSE

The digital filter sets the overall frequency response. The filter uses a multi-stage FIR topology to provide linear phase with minimal passband ripple and high stop band attenuation. The filter coefficients are identical to the coefficients used in the ADS1271. The oversampling ratio of the digital filter (that is, the ratio of the modulator sampling to the output data rate, or f_{MOD}/f_{DATA}) is a function of the selected mode, as shown in Table 2.

Table 2. Oversampling Ratio versus Mode

MODE SELECTION	OVERSAMPLING RATIO (f_{MOD}/f_{DATA})
High-Speed	64
High-Resolution	128
Low-Power	64
Low-Speed	64

Copyright © 2009, Texas Instruments Incorporated

High-Speed, Low-Power, and Low-Speed Modes

The digital filter configuration is the same in High-Speed, Low-Power, and Low-Speed modes with the oversampling ratio set to 64. Figure 54 shows the frequency response in High-Speed, Low-Power, and Low-Speed modes normalized to f_{DATA}. Figure 55 shows the passband ripple. The transition from passband to stop band is shown in Figure 56. The overall frequency response repeats at 64x multiples of the modulator frequency f_{MOD}, as shown in Figure 57.

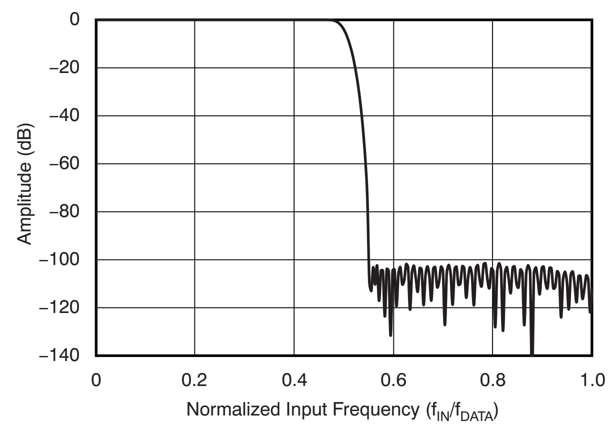


Figure 54. Frequency Response for High-Speed, Low-Power, and Low-Speed Modes

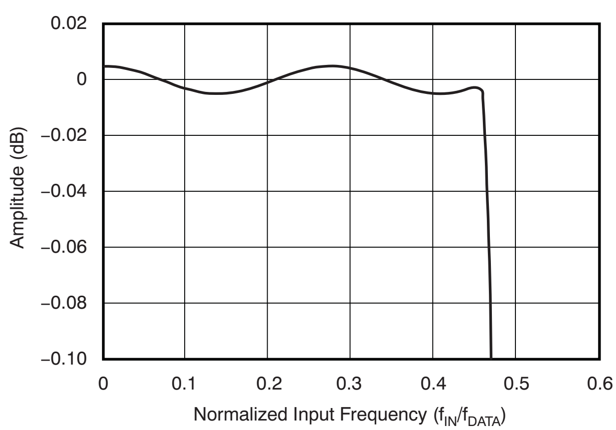


Figure 55. Passband Response for High-Speed, Low-Power, and Low-Speed Modes

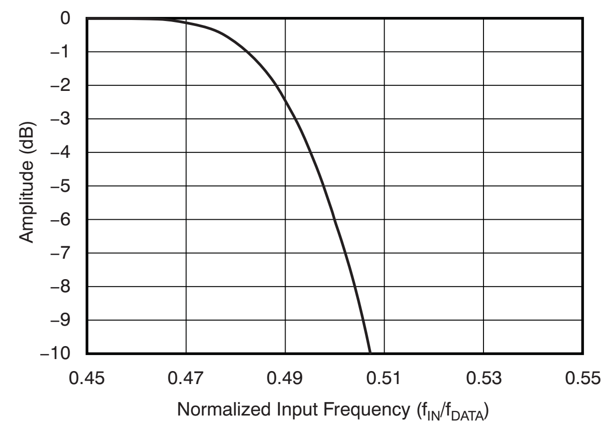


Figure 56. Transition Band Response for High-Speed, Low-Power, and Low-Speed Modes

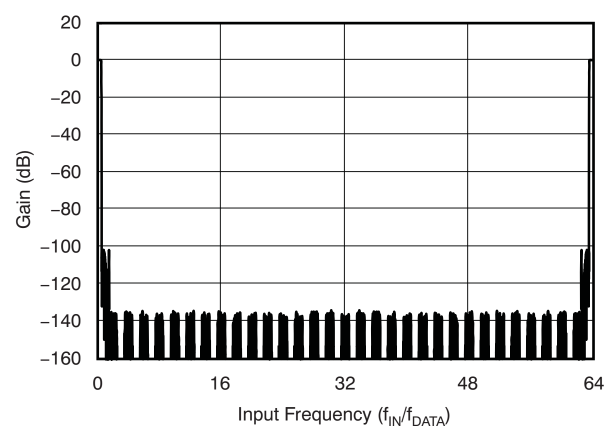


Figure 57. Frequency Response Out to f_{MOD} for High-Speed, Low-Power, and Low-Speed Modes

These image frequencies, if present in the signal and not externally filtered, will fold back (or alias) into the passband, causing errors. The stop band of the ADS1278 provides 100 dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1278 inputs is recommended to limit possible high-amplitude, out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 3 lists the image rejection versus external filter order.

Table 3. Antialiasing Filter Order Image Rejection

ANTIALIASING FILTER ORDER	IMAGE REJECTION (dB) (f_{-3dB} at f_{DATA})	
	HS, LP, LS	HR
1	39	45
2	75	87
3	111	129

High-Resolution Mode

The oversampling ratio is 128 in High-Resolution mode. Figure 58 shows the frequency response in High-Resolution mode normalized to f_{DATA}. Figure 59 shows the passband ripple, and the transition from passband to stop band is shown in Figure 60. The overall frequency response repeats at multiples of the modulator frequency f_{MOD} (128 × f_{DATA}), as shown in Figure 61. The stop band of the ADS1278 provides 100 dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1278 inputs is recommended to limit possible high-amplitude out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 3 lists the image rejection versus external filter order.

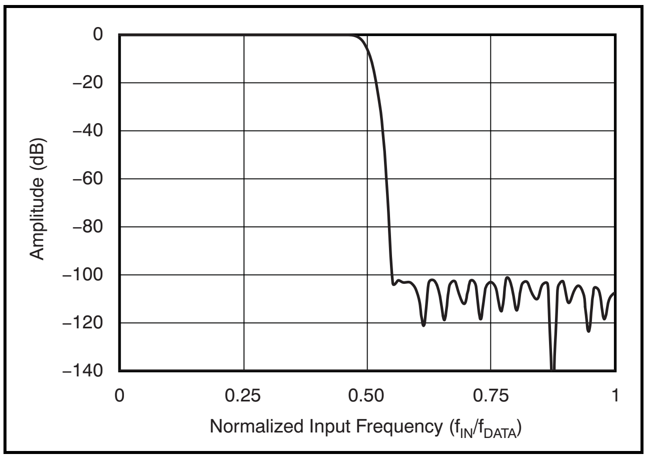


Figure 58. Frequency Response for High-Resolution Mode

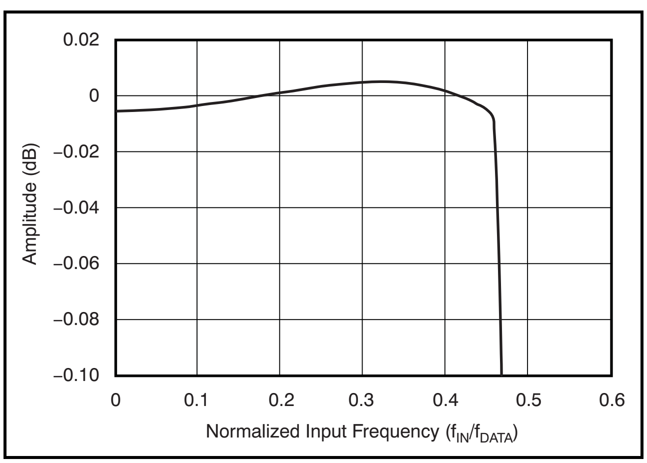


Figure 59. Passband Response for High-Resolution Mode

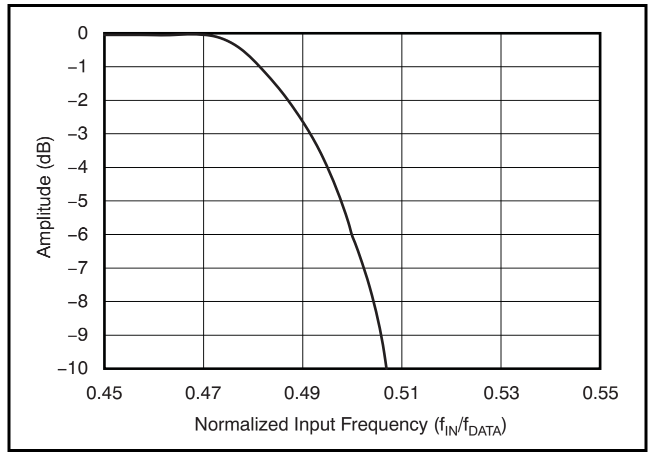


Figure 60. Transition Band Response for High-Resolution mode

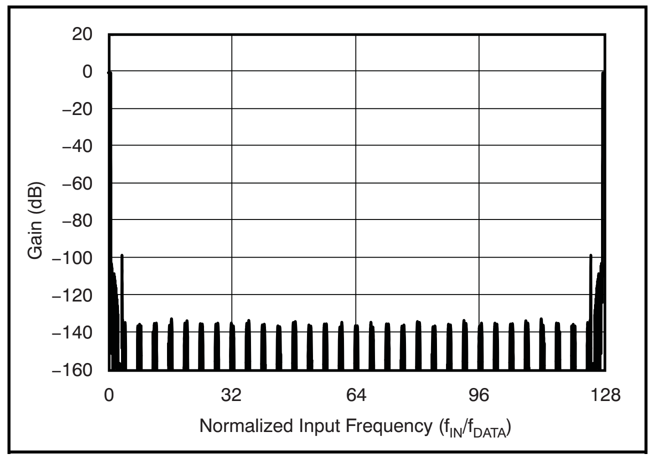


Figure 61. Frequency Response Out to f_{MOD} for High-Resolution Mode

Copyright © 2009, Texas Instruments Incorporated

PHASE RESPONSE

The ADS1278 incorporates a multiple stage, linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (constant group delay). This characteristic means the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of input signal frequency. This behavior results in essentially zero phase errors when analyzing multi-tone signals.

SETTLING TIME

As with frequency and phase response, the digital filter also determines settling time. Figure 62 shows the output settling behavior after a step change on the analog inputs normalized to conversion periods. The X-axis is given in units of conversion. Note that after the step change on the input occurs, the output data change very little prior to 30 conversion periods. The output data are fully settled after 76 conversion periods for High-Speed and Low-Power modes, and 78 conversion periods for High-Resolution mode.

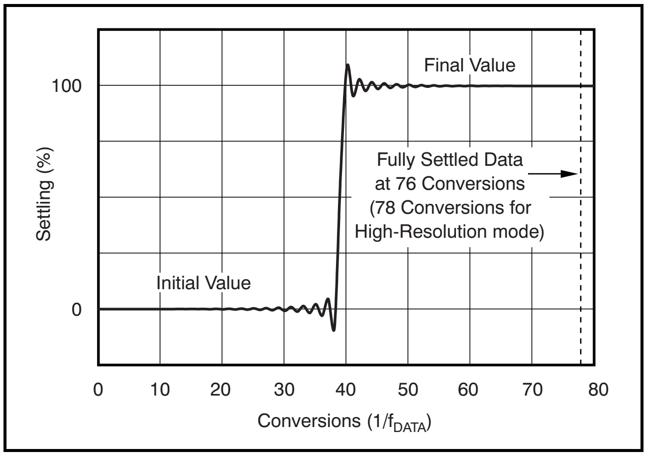


Figure 62. Step Response

DATA FORMAT

The ADS1278 outputs 24 bits of data in twos complement format.

A positive full-scale input produces an ideal output code of 7FFFFFh, and the negative full-scale input produces an ideal output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 4 summarizes the ideal output codes for different input signals.

Table 4. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
$\geq +V_{REF}$	7FFFFFh
$\frac{+V_{REF}}{2^{23}-1}$	000001h
0	000000h
$\frac{-V_{REF}}{2^{23}-1}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

ANALOG INPUTS (AINP, AINN)

The ADS1278 measures each differential input signal V_{IN} = (AINP – AINN) against the common differential reference V_{REF} = (VREFP – VREFN). The most positive measurable differential input is $+V_{REF}$, which produces the most positive digital output code of 7FFFFFh. Likewise, the most negative measurable differential input is $–V_{REF}$, which produces the most negative digital output code of 800000h.

For optimum performance, the inputs of the ADS1278 are intended to be driven differentially. For single-ended applications, one of the inputs (AINP or AINN) can be driven while the other input is fixed (typically to AGND or 2.5 V). Fixing the input to 2.5 V permits bipolar operation, thereby allowing full use of the entire converter range.

While the ADS1278 measures the differential input signal, the absolute input voltage is also important. This value is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

–0.1 V < (AINN or AINP) < AVDD + 0.1 V

If either input is taken below –0.4 V or above (AVDD + 0.4 V), ESD protection diodes on the inputs may turn on. If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

The ADS1278 is a very high-performance ADC. For optimum performance, it is critical that the appropriate circuitry be used to drive the ADS1278 inputs. See the *Application Information* section for several recommended circuits.

The ADS1278 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged. Figure 63 shows a conceptual diagram of these circuits. Switch S_2 represents the net effect of the modulator circuitry in discharging the sampling capacitor; the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 64. The sampling time (t_{SAMPLE}) is the inverse of modulator sampling frequency (f_{MOD}) and is a function of the mode, the CLKDIV input, and CLK frequency, as shown in Table 5.

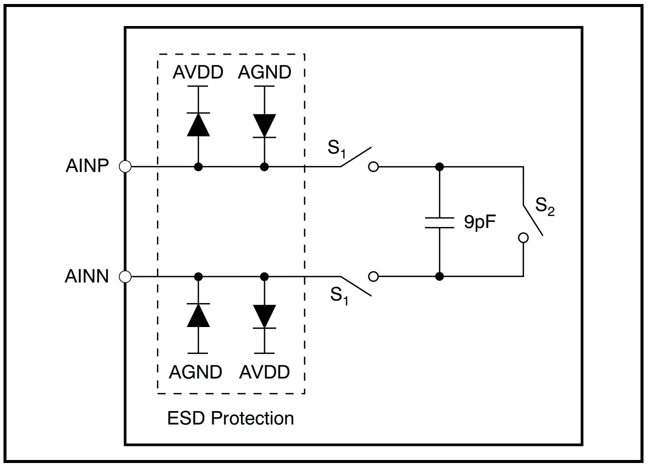


Figure 63. Equivalent Analog Input Circuitry

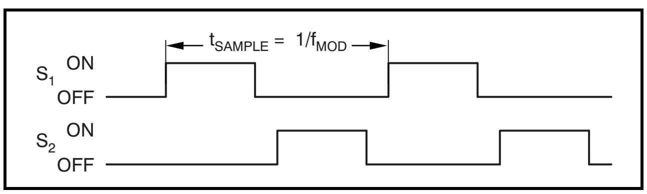


Figure 64. S_1 and S_2 Switch Timing for Figure 63

Table 5. Modulator Frequency (f_{MOD}) Mode Selection

MODE SELECTION	CLKDIV	f_{MOD}
High-Speed	1	$f_{CLK}/4$
High-Resolution	1	$f_{CLK}/4$
Low-Power	1	$f_{CLK}/8$
	0	$f_{CLK}/4$
Low-Speed	1	$f_{CLK}/40$
	0	$f_{CLK}/8$

The average load presented by the switched capacitor input can be modeled with an effective differential impedance, as shown in Figure 65. Note that the effective impedance is a function of f_{MOD}.

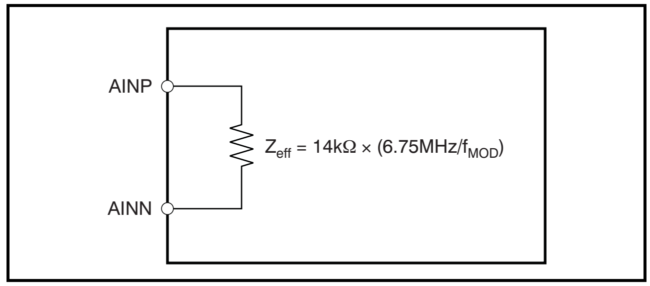


Figure 65. Effective Input Impedances

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1278 ADC is the differential voltage between VREFP and VREFN: V_{REF} = (VREFP – VREFN). The voltage reference is common to all channels. The reference inputs use a structure similar to that of the analog inputs with the equivalent circuitry on the reference inputs shown in Figure 66. As with the analog inputs, the load presented by the switched capacitor can be modeled with an effective impedance, as shown in Figure 67. However, the reference input impedance depends on the number of active (enabled) channels in addition to f_{MOD}. As a result of the change of reference input impedance caused by enabling and disabling channels, the regulation and setting time of the external reference should be noted, so as not to affect the readings.

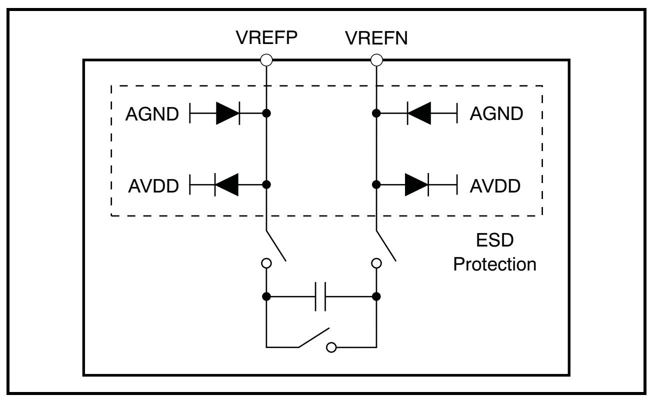


Figure 66. Equivalent Reference Input Circuitry

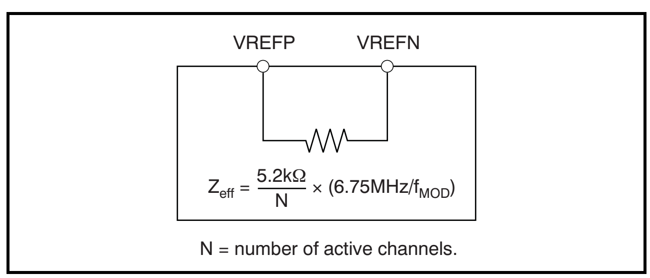


Figure 67. Effective Reference Impedance

Copyright © 2009, Texas Instruments Incorporated

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.4 V, and likewise do not exceed AVDD by 0.4 V. If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Note that the valid operating range of the reference inputs is limited to the following parameters:

–0.1 V ≤ VREFN ≤ +0.1 V

VREFN + 0.5 V ≤ VREFP ≤ AVDD + 0.1 V

CLOCK INPUT (CLK)

The ADS1278 requires a clock input for operation. The individual converters of the ADS1278 operate from the same clock input. At the maximum data rate, the clock input can be either 27 MHz or 13.5 MHz for Low-Power mode, or 2 7MHz or 5.4 MHz for Low-Speed mode, determined by the setting of the CLKDIV input. For High-Speed mode, the maximum CLK input frequency is 32.768 MHz. For High-Resolution mode, the maximum CLK input frequency is 27 MHz. The selection of the external clock frequency (f_{CLK}) does not affect the resolution of the ADS1278. Use of a slower f_{CLK} can reduce the power consumption of an external clock buffer. The output data rate scales with clock frequency, down to a minimum clock frequency of f_{CLK} = 100 kHz. Table 6 summarizes the ratio of the clock input frequency (f_{CLK}) to data rate (f_{DATA}), maximum data rate and corresponding maximum clock input for the four operating modes.

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keeping the clock trace as short as possible, and using a 50-Ω series resistor placed close to the source end, often helps.

Table 6. Clock Input Options

MODE SELECTION	MAX f_{CLK} (MHz)	CLKDIV	f_{CLK}/f_{DATA}	DATA RATE (SPS)
High-Speed	32.768	1	256	128,000
High-Resolution	27	1	512	52,734
Low-Power	27	1	512	52,734
	13.5	0	256	
Low-Speed	27	1	2,560	10,547
	5.4	0	512	

MODE SELECTION (MODE)

The ADS1278 supports four modes of operation: High-Speed, High-Resolution, Low-Power, and Low-Speed. The modes offer optimization of speed, resolution, and power. Mode selection is determined by the status of the digital input MODE[1:0] pins, as shown in Table 7. The ADS1278 continually monitors the status of the MODE pin during operation.

Table 7. Mode Selection

MODE[1:0]	MODE SELECTION	MAX f_{DATA} (1)
00	High-Speed	128,000
01	High-Resolution	52,734
10	Low-Power	52,734
11	Low-Speed	10,547

(1) f_{CLK} = 27 MHz max (32.768MHz max in High-Speed mode).

When using the SPI protocol, $\overline{DRDY}$ is held high after a mode change occurs until settled (or valid) data are ready; see Figure 68 and Table 8.

In Frame-Sync protocol, the DOUT pins are held low after a mode change occurs until settled data are ready; see Figure 68 and Table 8. Data can be read from the device to detect when DOUT changes to logic 1, indicating that the data are valid.

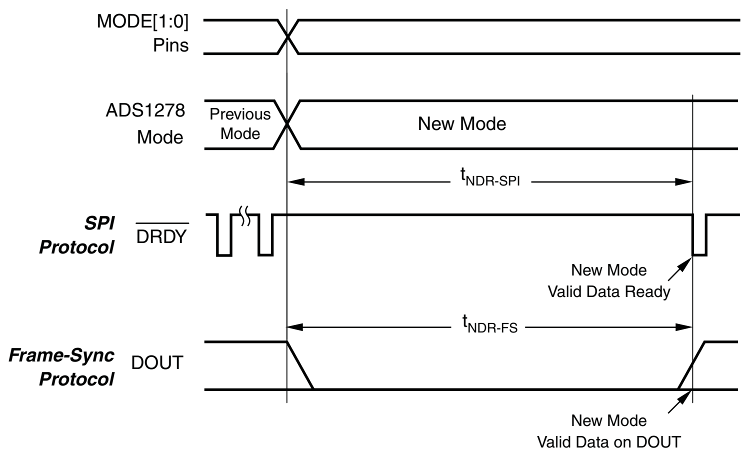


Figure 68. Mode Change Timing

Table 8. New Data After Mode Change

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{NDR-SPI}$	Time for new data to be ready (SPI)			129	Conversions ($1/f_{DATA}$)
t_{NDR-FS}	Time for new data to be ready (Frame-Sync)	127		128	Conversions ($1/f_{DATA}$)

SYNCHRONIZATION (SYNC)

The ADS1278 can be synchronized by pulsing the SYNC pin low and then returning the pin high. When the pin goes low, the conversion process stops, and the internal counters used by the digital filter are reset. When the SYNC pin returns high, the conversion process restarts. Synchronization allows the conversion to be aligned with an external event, such as the changing of an external multiplexer on the analog inputs, or by a reference timing pulse.

Because the ADS1278 converters operate in parallel from the same master clock and use the same SYNC input control, they are always in synchronization with each other. The aperture match among internal channels is typically less than 500 ps. However, the synchronization of multiple devices is somewhat different. At device power-on, variations in internal reset thresholds from device to device may result in uncertainty in conversion timing.

The SYNC pin can be used to synchronize multiple devices to within the same CLK cycle. Figure 69 illustrates the timing requirement of SYNC and CLK in SPI format.

See Figure 70 for the Frame-Sync format timing requirement.

After synchronization, indication of valid data depends on whether SPI or Frame-Sync format was used.

In the SPI format, DRDY goes high as soon as SYNC is taken low; see Figure 69. After SYNC is returned high, DRDY stays high while the digital filter is settling. Once valid data are ready for retrieval, DRDY goes low.

In the Frame-Sync format, DOUT goes low as soon as SYNC is taken low; see Figure 70. After SYNC is returned high, DOUT stays low while the digital filter is settling. Once valid data are ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking SYNC high, and must then remain running. If the clock inputs (CLK, FSYNC or SCLK) are subsequently interrupted or reset, re-assert the SYNC pin.

For consistent performance, re-assert SYNC after device power-on when data first appear.

 Copyright © 2009, Texas Instruments Incorporated

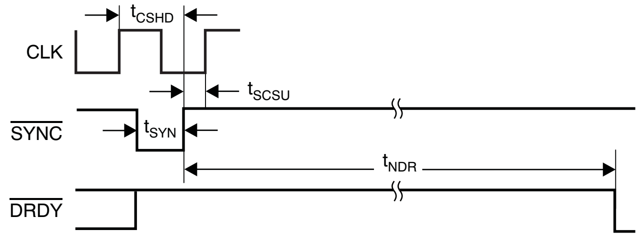


Figure 69. Synchronization Timing (SPI Protocol)

Table 9. SPI Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{\text{SYNC}}$ hold time	10			ns
t_{SCSU}	$\overline{\text{SYNC}}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready			129	Conversions ($1/f_{DATA}$)

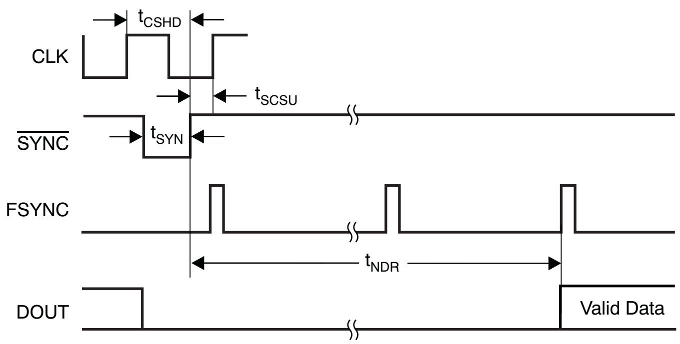


Figure 70. Synchronization Timing (Frame-Sync Protocol)

Table 10. Frame-Sync Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{\text{SYNC}}$ hold time	10			ns
t_{SCSU}	$\overline{\text{SYNC}}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready	127		128	Conversions ($1/f_{DATA}$)

POWER-DOWN (PWDN)

The channels of the ADS1278 can be independently powered down by use of the PWDN inputs. To enter the power-down mode, hold the respective PWDN pin low for at least two CLK cycles. To exit power-down, return the corresponding PWDN pin high. Note that when all channels are powered down, the ADS1278 enters a microwatt (μW) power state where all internal biasing is disabled. In this state, the TEST[1:0] input pins must be driven; all other input pins can float. The ADS1278 outputs remain driven.

As shown in Figure 71 and Table 11, a maximum of 130 conversion cycles must elapse for SPI interface, and 129 conversion cycles must elapse for Frame-Sync, before reading data after exiting power-down. Data from channels already running are not affected. The user software can perform the required delay time in any of the following ways:

1. Count the number of data conversions after taking the PWDN pin high.
2. Delay $129/f_{DATA}$ or $130/f_{DATA}$ after taking the PWDN pins high, then read data.
3. Detect for non-zero data in the powered-up channel.

After powering up one or more channels, the channels are synchronized to each other. It is not necessary to use the SYNC pin to synchronize them.

When a channel is powered down in TDM data format, the data for that channel are either forced to zero (fixed-position TDM data mode) or replaced by shifting the data from the next channel into the vacated data position (dynamic-position TDM data mode).

In Discrete data format, the data are always forced to zero. When powering-up a channel in dynamic-position TDM data format mode, the channel data remain packed until the data are ready, at which time the data frame is expanded to include the just-powered channel data. See the Data Format section for details.

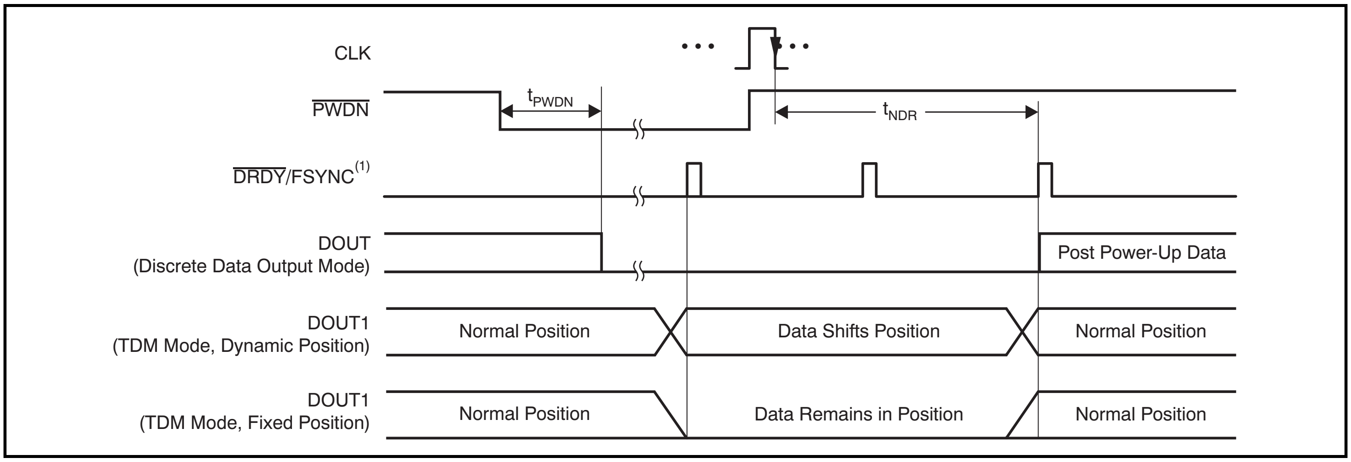


Figure 71. Power-Down Timing

Table 11. Power-Down Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PWDN}	PWDN pulse width to enter Power-Down mode	2			CLK periods
t_{NDR}	Time for new data ready (SPI)	129		130	Conversions ($1/f_{DATA}$)
t_{NDR}	Time for new data ready (Frame-Sync)	128		129	Conversions ($1/f_{DATA}$)

Copyright © 2009, Texas Instruments Incorporated

FORMAT[2:0]

Data can be read from the ADS1278 with two interface protocols (SPI or Frame-Sync) and several options of data formats (TDM/Discrete and Fixed/Dynamic data positions). The FORMAT[2:0] inputs are used to select among the options. Table 12 lists the available options. See the *DOUT Modes* section for details of the DOUT Mode and Data Position.

Table 12. Data Output Format

FORMAT[2:0]	INTERFACE PROTOCOL	DOUT MODE	DATA POSITION
000	SPI	TDM	Dynamic
001	SPI	TDM	Fixed
010	SPI	Discrete	—
011	Frame-Sync	TDM	Dynamic
100	Frame-Sync	TDM	Fixed
101	Frame-Sync	Discrete	—
110	Modulator Mode	—	—

SERIAL INTERFACE PROTOCOLS

Data are retrieved from the ADS1278 using the serial interface. Two protocols are available: SPI and Frame-Sync. The same pins are used for both interfaces: SCLK, DRDY/FSYNC, DOUT[8:1], and DIN. The FORMAT[2:0] pins select the desired interface protocol.

SPI SERIAL INTERFACE

The SPI-compatible format is a read-only interface. Data ready for retrieval are indicated by the falling DRDY output and are shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple devices. See the *Daisy-Chaining* section for more information.

NOTE: The SPI format is limited to a CLK input frequency of 27 MHz, maximum. For CLK input operation above 27 MHz (High-Speed mode only), use Frame-Sync format.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user normally shifts this data in on the rising edge.

Even though the SCLK input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data.

SCLK may be run as fast as the CLK frequency. SCLK may be either in free-running or stop-clock operation between conversions. Note that one f_{CLK} is required after the falling edge of DRDY until the first rising edge of SCLK. For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

DRDY/FSYNC (SPI Format)

In the SPI format, this pin functions as the DRDY output. It goes low when data are ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data are not retrieved (that is, SCLK is held low), DRDY pulses high just before the next conversion data are ready, as shown in Figure 72. The new data are loaded within one CLK cycle before DRDY goes low. All data must be shifted out before this time to avoid being overwritten.

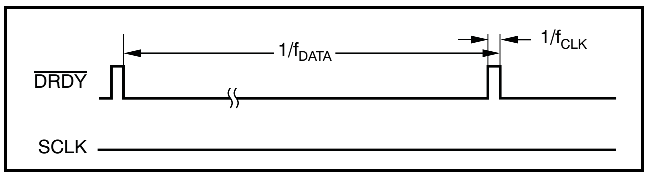


Figure 72. DRDY Timing with No Readback

DOUT

The conversion data are output on DOUT[8:1]. The MSB data are valid on DOUT[8:1] after DRDY goes low. Subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT after all channel data have been shifted out. When the device is configured for modulator output, DOUT[8:1] becomes the modulator data output for each channel (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1278s are to be daisy-chained together. The DOUT1 pin of the first device connects to the DIN pin of the next, etc. It can be used with either the SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278, tie DIN low. See the *Daisy-Chaining* section for more information.

FRAME-SYNC SERIAL INTERFACE

Frame-Sync format is similar to the interface often used on audio ADCs. It operates in slave fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data are output MSB first or *left-justified* on the rising edge of FSYNC. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the relationships shown in the Frame-Sync Timing Requirements.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously. If it is shut down, the data readback will be corrupted. The number of SCLKs within a frame period (FSYNC clock) can be any power-of-2 ratio of CLK cycles (1, 1/2, 1/4, etc), as long as the number of cycles is sufficient to shift the data output from all channels within one frame. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

DRDY/FSYNC (Frame-Sync Format)

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period, which must be the same as the data rate. The required number of f_{CLK} cycles to each FSYNC period depends on the mode selection and the CLKDIV input. Table 6 indicates the number of CLK cycles to each frame (f_{CLK}/f_{DATA}). If the FSYNC period is not the proper value, data readback will be corrupted.

DOUT

The conversion data are shifted out on DOUT[8:1]. The MSB data become valid on DOUT[8:1] after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT[8:1] after all channel data have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1278s are to be daisy-chained together. It can be used with either SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278, tie DIN low. See the *Daisy-Chaining* section for more information.

DOUT MODES

For both SPI and Frame-Sync interface protocols, the data are shifted out either through individual channel DOUT pins, in a parallel data format (Discrete mode), or the data for all channels are shifted out, in a serial format, through a common pin, DOUT1 (TDM mode).

TDM Mode

In TDM (time-division multiplexed) data output mode, the data for all channels are shifted out, in sequence, on a single pin (DOUT1). As shown in Figure 73, the data from channel 1 are shifted out first, followed by channel 2 data, etc. After the data from the last channel are shifted out, the data from the DIN input follow. The DIN is used to daisy-chain the data output from an additional ADS1278 or other compatible device. Note that when all channels of the ADS1278 are disabled, the interface is disabled, rendering the DIN input disabled as well. When one or more channels of the device are powered down, the data format of the TDM mode can be fixed or dynamic.

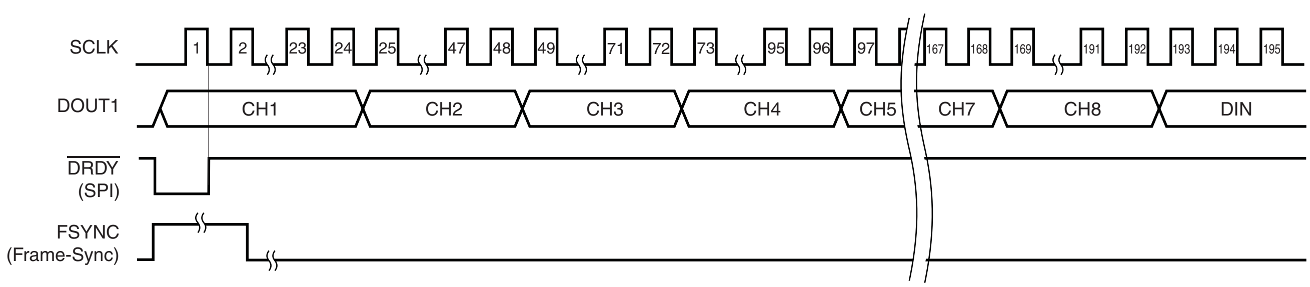


Figure 73. TDM Mode (All Channels Enabled)

 Copyright © 2009, Texas Instruments Incorporated

TDM Mode, Fixed-Position Data

In this TDM data output mode, the data position of the channels remain fixed, regardless of whether the channels are powered down. If a channel is powered down, the data are forced to zero but occupy the same position within the data stream. Figure 74 shows the data stream with channel 1 and channel 3 powered down.

TDM Mode, Dynamic Position Data

In this TDM data output mode, when a channel is powered down, the data from higher channels shift one position in the data stream to fill the vacated data slot. Figure 75 shows the data stream with channel 1 and channel 3 powered down.

Discrete Data Output Mode

In Discrete data output mode, the channel data are shifted out in parallel using individual channel data output pins DOUT[8:1]. After the 24th SCLK, the channel data are forced to zero. The data are also forced to zero for powered down channels. Figure 76 shows the discrete data output format.

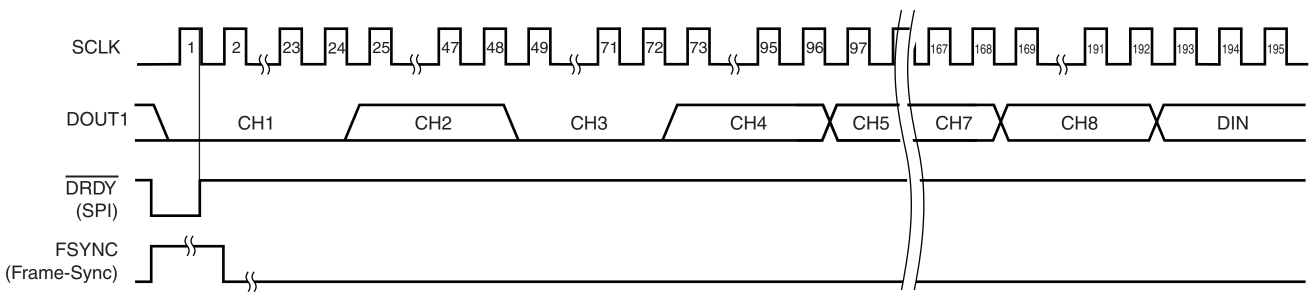


Figure 74. TDM Mode, Fixed-Position Data (Channels 1 and 3 Shown Powered Down)

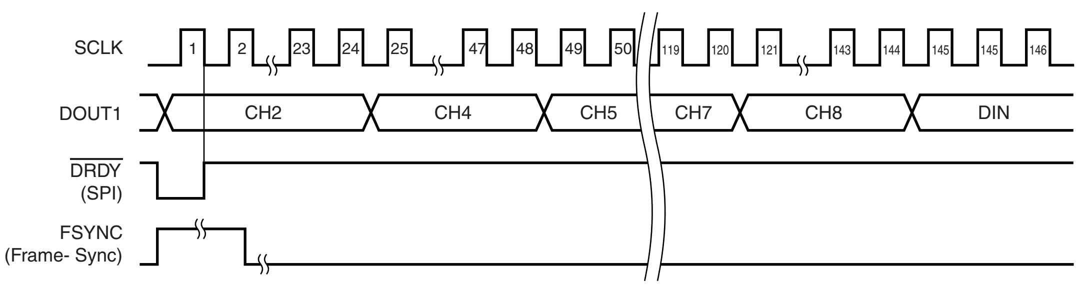


Figure 75. TDM Mode, Dynamic Position Data (Channels 1 and 3 Shown Powered Down)

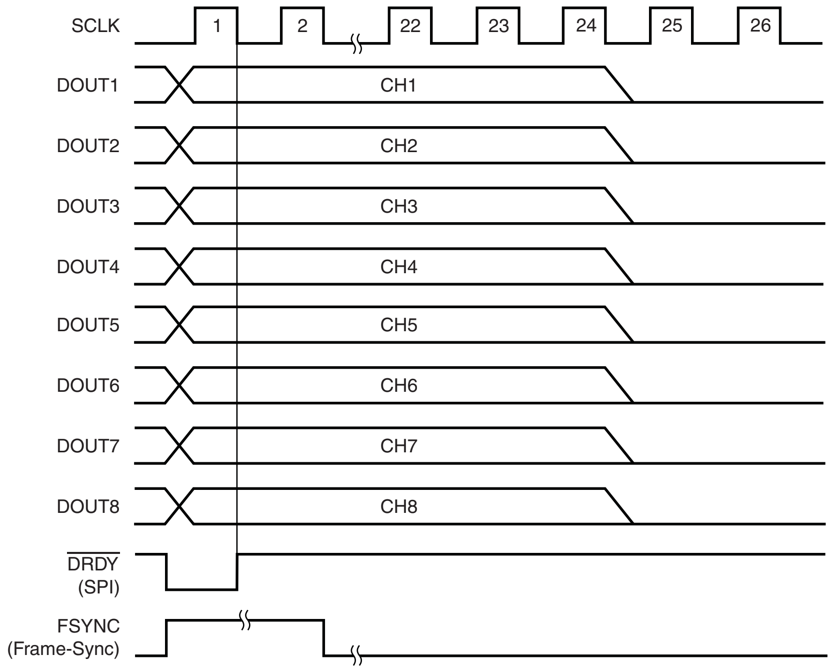


Figure 76. Discrete Data Output Mode

DAISY-CHAINING

Multiple ADS1278s can be daisy-chained together to output data on a single pin. The DOUT1 data output pin of one device is connected to the DIN of the next device. As shown in Figure 77, the DOUT1 pin of device 1 provides the output data to a controller, and the DIN of device 2 is grounded. Figure 78 shows the data format when reading back data.

The maximum number of channels that may be daisy-chained in this way is limited by the frequency of f_{SCLK}, the mode selection, and the CLKDIV input. The frequency of f_{SCLK} must be high enough to completely shift the data out from all channels within one f_{DATA} period. Table 13 lists the maximum number of daisy-chained channels when $f_{SCLK} = f_{CLK}$.

To increase the number of data channels possible in a chain, a segmented DOUT scheme may be used, producing two data streams. Figure 79 illustrates four ADS1278s, with pairs of ADS1278s daisy-chained together. The channel data of each daisy-chained pair are shifted out in parallel and received by the processor through independent data channels.

Table 13. Maximum Channels in a Daisy-Chain ($f_{SCLK} = f_{CLK}$)

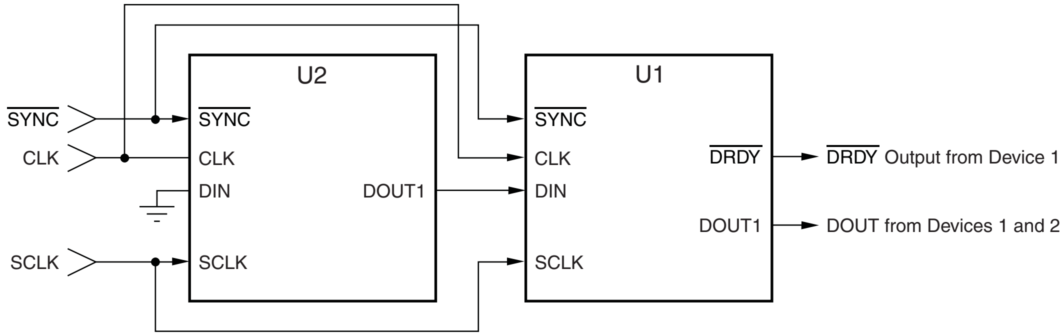
MODE SELECTION	CLKDIV	MAXIMUM NUMBER OF CHANNELS
High-Speed	1	10
High-Resolution	1	21
Low-Power	1	21
	0	10
Low-Speed	1	106
	0	21

Whether the interface protocol is SPI or Frame-Sync, it is recommended to synchronize all devices by tying the SYNC inputs together. When synchronized in SPI protocol, it is only necessary to monitor the DRDY output of one ADS1278.

In Frame-Sync interface protocol, the data from all devices are ready after the rising edge of FSYNC.

Since DOUT1 and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT1 creates a setup time on DIN. Minimize the skew in SCLK to avoid timing violations.

Copyright © 2009, Texas Instruments Incorporated



Note: The number of chained devices is limited by the SCLK rate and device mode.

Figure 77. Daisy-Chaining of Two Devices, SPI Protocol (FORMAT[2:0] = 000 or 001)

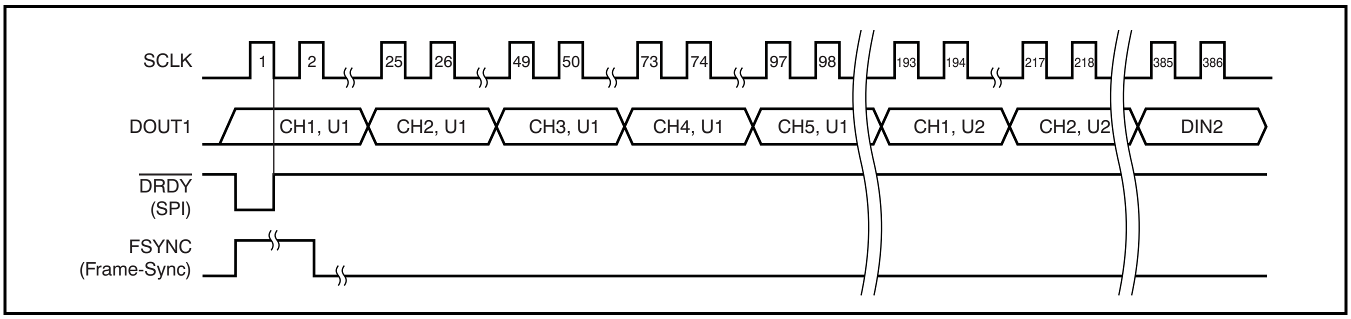
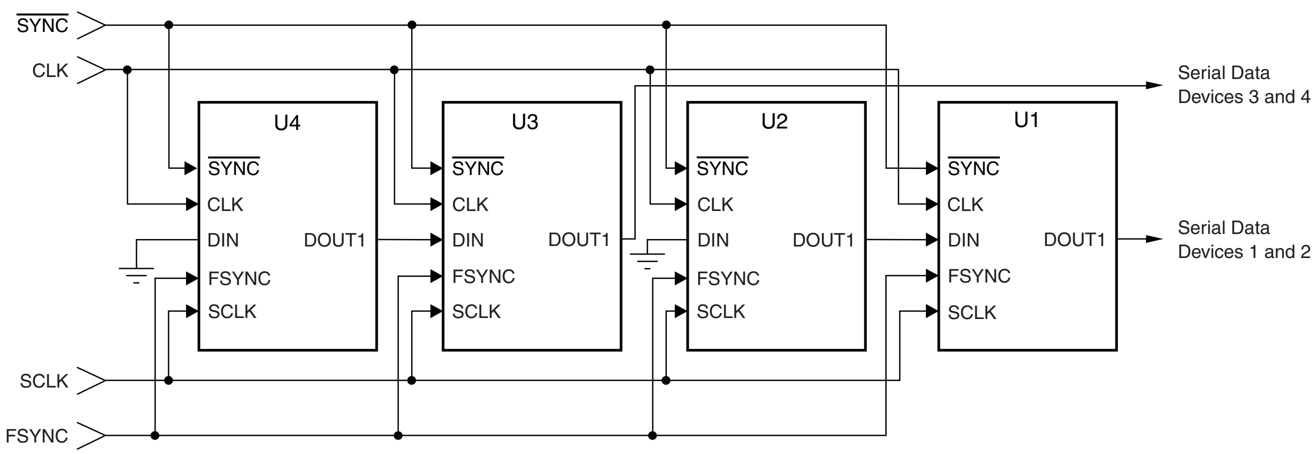


Figure 78. Daisy-Chain Data Format of Figure 77



Note: The number of chained devices is limited by the SCLK rate and device mode.

Figure 79. Segmented DOUT Daisy-Chain, Frame-Sync Protocol (FORMAT[2:0] = 011 or 100)

POWER SUPPLIES

The ADS1278 has three power supplies: AVDD, DVDD, and IOVDD. AVDD is the analog supply that powers the modulator, DVDD is the digital supply that powers the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be tied together if desired (1.8 V). To achieve rated performance, it is critical that the power supplies are bypassed with 0.1-µF and 10-µF capacitors placed as close as possible to the supply pins. A single 10-µF ceramic capacitor may be substituted in place of the two capacitors.

Figure 80 shows the start-up sequence of the ADS1278. At power-on, bring up the DVDD supply first, followed by IOVDD and then AVDD. Check the power-supply sequence for proper order, including the ramp rate of each supply. DVDD and IOVDD may be sequenced at the same time if the supplies are tied together. Each supply has an internal reset circuit whose outputs are summed together to generate a global power-on reset. After the supplies have exceeded the reset thresholds, 2^{18} f_{CLK} cycles are counted before the converter initiates the conversion process. Following the CLK cycles, the data for 129 conversions are suppressed by the ADS1278 to allow output of fully-settled data. In SPI protocol, $\overline{DRDY}$ is held high during this interval. In frame-sync protocol, DOUT is forced to zero. The power supplies should be applied before any analog or digital pin is driven. For consistent performance, assert $\overline{SYNC}$ after device power-on when data first appear.

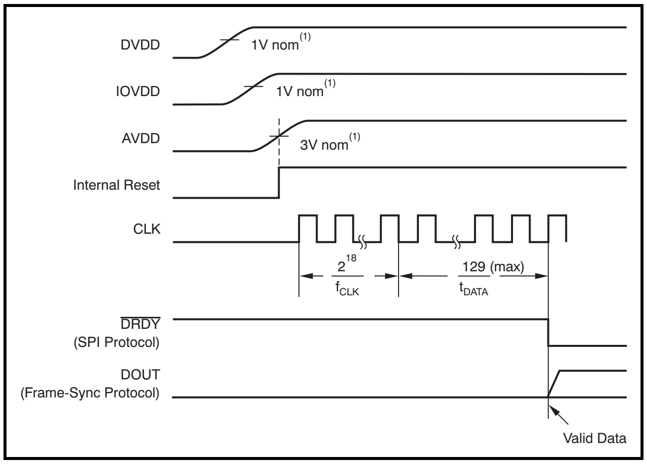


Figure 80. Start-Up Sequence

MODULATOR OUTPUT

The ADS1278 incorporates a 6th-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter that yields the conversion results. The data stream output of the modulator is available directly, bypassing the internal digital filter. The digital filter is disabled, reducing the DVDD current, as shown in Table 14. In this mode, an external digital filter implemented in an ASIC, FPGA, or similar device is required. To invoke the modulator output, tie FORMAT[2:0], as shown in Figure 81. DOUT[8:1] then becomes the modulator data stream outputs for each channel and SCLK becomes the modulator clock output. The $\overline{DRDY}$/FSYNC pin becomes an unused output and can be ignored. The normal operation of the Frame-Sync and SPI interfaces is disabled, and the functionality of SCLK changes from an input to an output, as shown in Figure 81.

Table 14. Modulator Output Clock Frequencies

MODE [1:0]	CLKDIV	MODULATOR CLOCK OUTPUT (SCLK)	DVDD (mA)
00	1	$f_{CLK}/4$	8
01	1	$f_{CLK}/4$	7
10	1	$f_{CLK}/8$	4
	0	$f_{CLK}/4$	4
11	1	$f_{CLK}/40$	1
	0	$f_{CLK}/8$	1

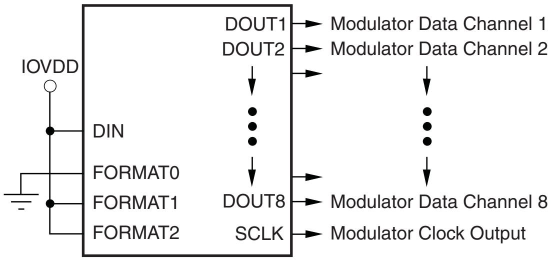


Figure 81. Modulator Output

Copyright © 2009, Texas Instruments Incorporated

In modulator output mode, the frequency of the modulator clock output (SCLK) depends on the mode selection of the ADS1278. Table 14 lists the modulator clock output frequency and DVDD current versus device mode.

Figure 82 shows the timing relationship of the modulator clock and data outputs.

The data output is a modulated 1s density data stream. When V_{IN} = $+V_{REF}$, the 1s density is approximately 80% and when V_{IN} = $–V_{REF}$, the 1s density is approximately 20%.

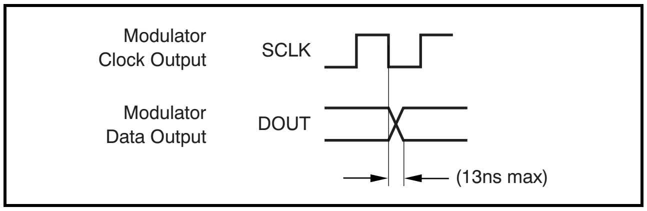


Figure 82. Modulator Output Timing

PIN TEST USING TEST[1:0] INPUTS

The test mode feature of the ADS1278 allows continuity testing of the digital I/O pins. In this mode, the normal functions of the digital pins are disabled and routed to each other as pairs through internal logic, as shown in Table 15. The pins in the left column drive the output pins in the right column. **Note:** some of the digital input pins become outputs; these outputs must be accommodated in the design. The analog input, power supply, and ground pins all remain connected as normal. The test mode is engaged by setting the pins TEST [1:0] = 11. For normal converter operation, set TEST[1:0] = 00. Do not use '01' or '10'.

Table 15. Test Mode Pin Map (TEST[1:0] = 11)

TEST MODE PIN MAP	
INPUT PINS	**OUTPUT PINS**
$\overline{\text{PWDN1}}$	DOUT1
$\overline{\text{PWDN2}}$	DOUT2
$\overline{\text{PWDN3}}$	DOUT3
$\overline{\text{PWDN4}}$	DOUT4
$\overline{\text{PWDN5}}$	DOUT5
$\overline{\text{PWDN6}}$	DOUT6
$\overline{\text{PWDN7}}$	DOUT7
$\overline{\text{PWDN8}}$	DOUT8
MODE0	DIN
MODE1	$\overline{\text{SYNC}}$
FORMAT0	CLKDIV
FORMAT1	FSYNC/$\overline{\text{DRDY}}$
FORMAT2	SCLK

VCOM OUTPUT

The VCOM pin provides a voltage output equal to AVDD/2. The intended use of this output is to set the output common-mode level of the analog input drivers. The drive capability of the output is limited; therefore, the output should only be used to drive high-impedance nodes (> 1 MΩ). In some cases, an external buffer may be necessary. A 0.1-μF bypass capacitor is recommended to reduce noise pickup.

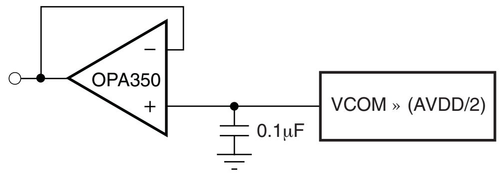


Figure 83. VCOM Output

APPLICATION INFORMATION

To obtain the specified performance from the ADS1278, the following layout and component guidelines should be considered.

1. **Power Supplies:** The device requires three power supplies for operation: DVDD, IOVDD, and AVDD. The allowed range for DVDD is 1.65 V to 1.95 V; the range of IOVDD is 1.65 V to 3.6 V; AVDD is restricted to 4.75 V to 5.25 V. For all supplies, use a 10-µF tantalum capacitor, bypassed with a 0.1-µF ceramic capacitor, placed close to the device pins. Alternatively, a single 10-µF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power-supply source is used, the voltage ripple should be low (less than 2 mV) and the switching frequency outside the passband of the converter.
2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
3. **Digital Inputs:** It is recommended to source-terminate the digital inputs to the device with 50-Ω series resistors. The resistors should be placed close to the driving end of digital source (oscillator, logic gates, DSP, etc.) This placement helps to reduce ringing on the digital lines (ringing may lead to degraded ADC performance).
4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
5. **Reference Inputs:** It is recommended to use a minimum 10-µF tantalum with a 0.1-µF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should have less than 3 μV_{RMS} in-band noise. For references with noise higher than this level, external reference filtering may be necessary.
6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 1-nF to 10-nF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground can be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100 pF) to preserve the ac common-mode performance.
7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This layout is particularly important for small-value ceramic capacitors. Larger (bulk) decoupling capacitors can be located farther from the device than the smaller ceramic capacitors.

Copyright © 2009, Texas Instruments Incorporated

PowerPAD THERMALLY-ENHANCED PACKAGING

The PowerPAD concept is implemented in standard epoxy resin package material. The integrated circuit is attached to the leadframe die pad using thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This design provides an extremely low thermal resistance to the path between the IC junction and the exterior case. The external surface of the leadframe die pad is located on the printed circuit board (PCB) side of the package, allowing the die pad to be attached to the PCB using standard flow soldering techniques. This configuration allows efficient attachment to the PCB and permits the board structure to be used as a heatsink for the package. Using a thermal pad identical in size to the die pad and vias connected to the PCB ground plane, the board designer can now implement power packaging without additional thermal hardware (for example, external heatsinks) or the need for specialized assembly instructions.

Figure 84 illustrates a cross-section view of a PowerPAD package.

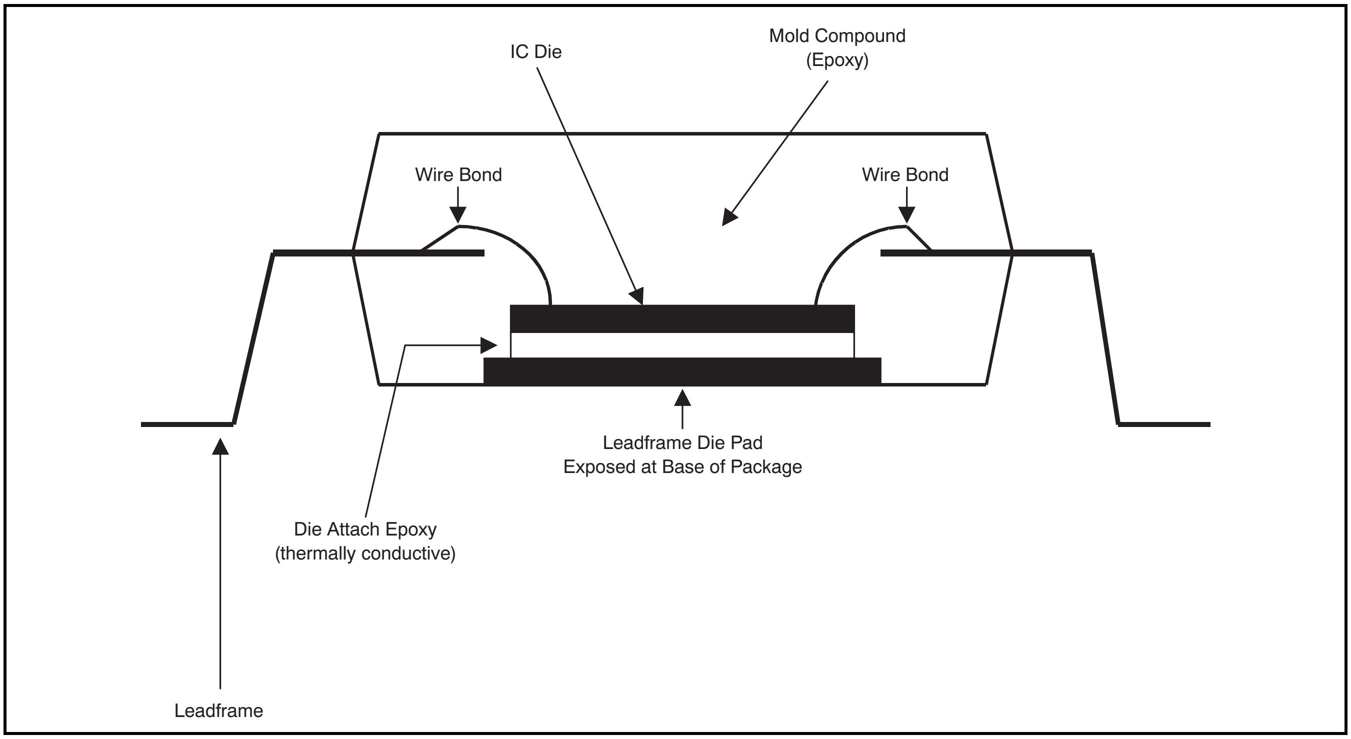


Figure 84. Cross-Section View of a PowerPAD Thermally-Enhanced Package

PowerPAD PCB Layout Considerations

Figure 85 shows the recommended layer structure for thermal management when using a PowerPad package on a 4-layer PCB design. Note that the thermal pad is placed on both the top and bottom sides of the board. The ground plane is used as the heatsink, while the power plane is thermally isolated from the thermal vias.

Additional PowerPAD Package Information

Texas Instruments publishes the PowerPAD Thermally Enhanced Package Application Report (TI literature number SLMA002), available for download at www.ti.com, that provides a more detailed discussion of PowerPAD design and layout considerations.

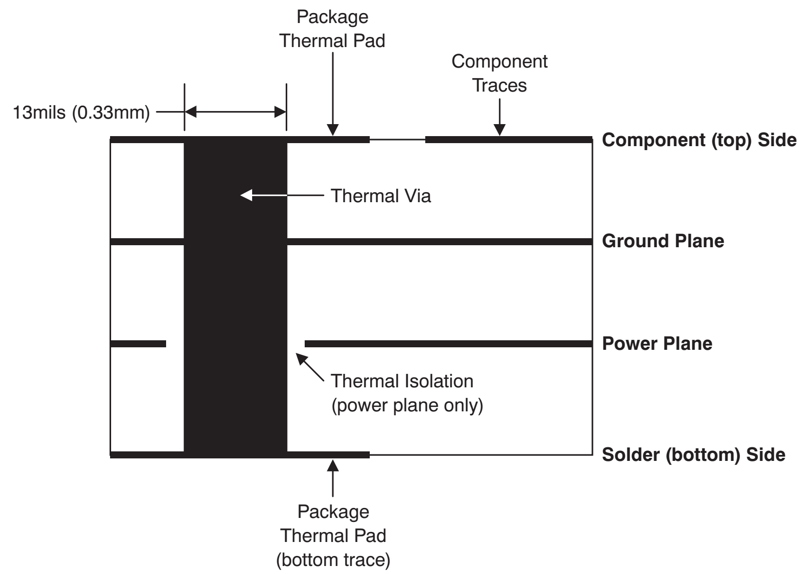


Figure 85. Recommended PCB Structure for a 4-Layer Board

Copyright © 2009, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS1278SKGDA	ACTIVE	XCEPT	KGD	0	180	TBD	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated