



STW26NM50

N-CHANNEL 500V - 0.10Ω - 30A TO-247 MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW26NM50	500 V	< 0.120 Ω	30 A

- TYPICAL R_{DS(on)} = 0.10 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW26NM50	W26NM50	TO-247	TUBE

Figure 1: Package

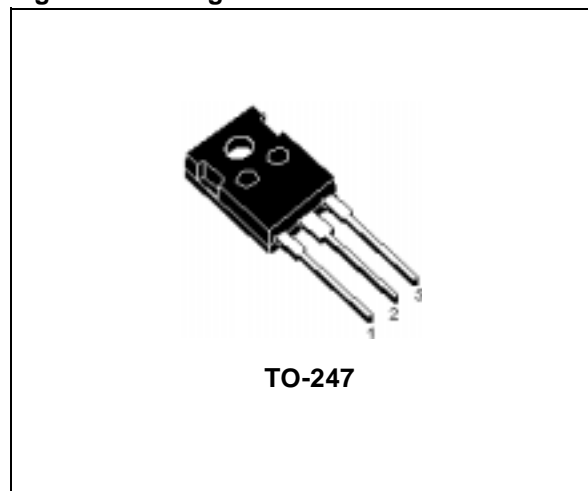


Figure 2: Internal Schematic Diagram

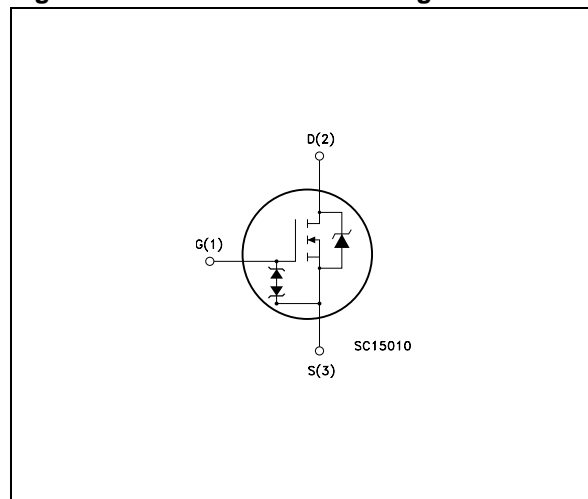


Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	30	A
I _D	Drain Current (continuous) at T _C = 100°C	18.9	A
I _{DM} (•)	Drain Current (pulsed)	120	A
P _{TOT}	Total Dissipation at T _C = 25°C	313	W
	Derating Factor	2.5	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 26A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

Table 4: Thermal Data

R _{thj-case}	Thermal Resistance Junction-case Max	0.4	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	13	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	740	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED)

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gss} = ± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Table 7: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \text{ mA}, V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^\circ\text{C}$			10 100	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 13 \text{ A}$		0.10	0.12	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 13 \text{ A}$		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$		3000 700 50		pF pF pF
$C_{OSS \text{ eq}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ to } 400 \text{ V}$		300		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 250 \text{ V}, I_D = 13 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 15)		28 15 13 19		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 \text{ V}, I_D = 26 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 18)		76 20 36	106	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				26 104	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 26 \text{ A}, V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 26 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100\text{V}$ (see Figure 16)		400 5.5 27.8		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 26 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100\text{V}, T_j = 150^\circ\text{C}$ (see Figure 16)		492 7 28.8		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3) $C_{OSS \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area

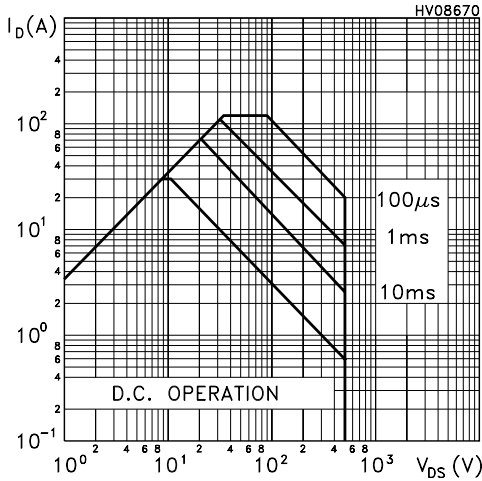


Figure 4: Output Characteristics

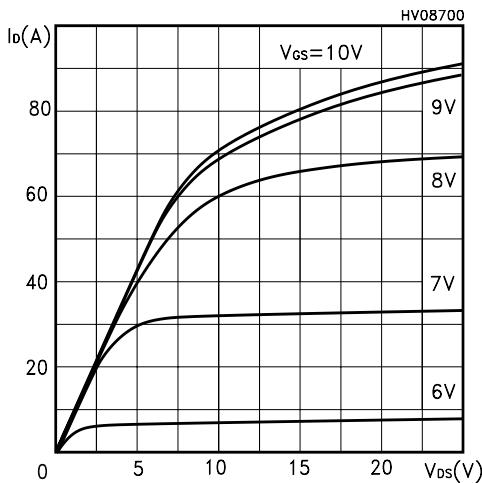


Figure 5: Transconductance

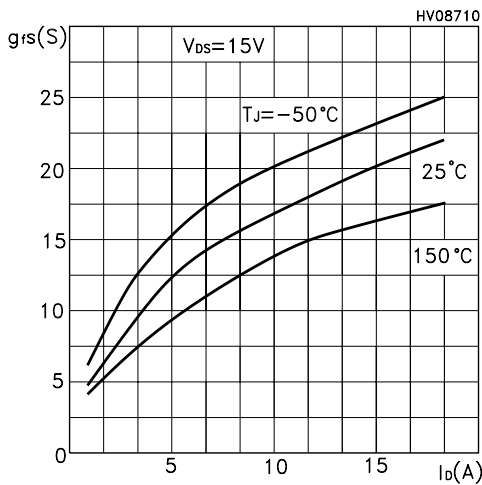


Figure 6: Thermal Impedance

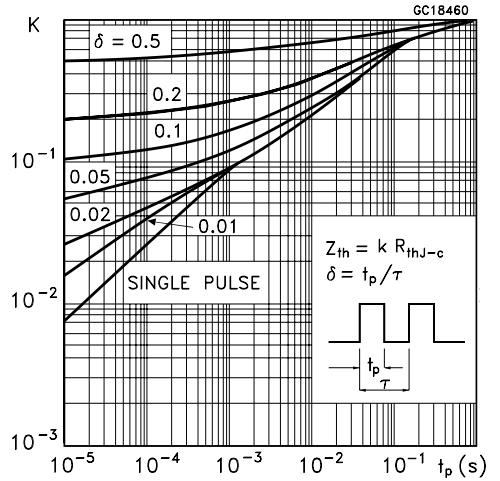


Figure 7: Transfer Characteristics

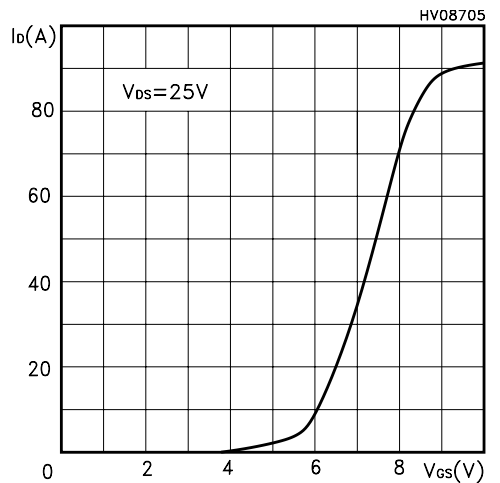


Figure 8: Static Drain-source On Resistance

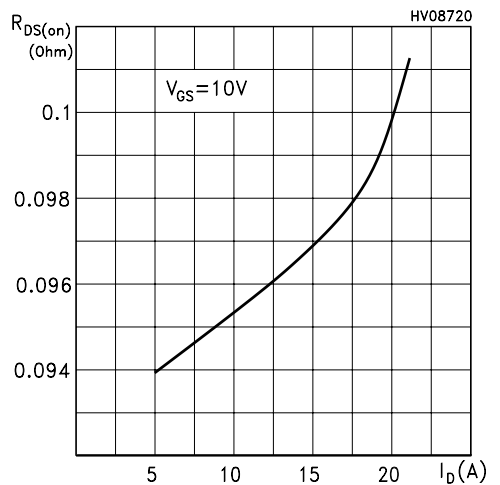


Figure 9: Gate Charge vs Gate-source Voltage

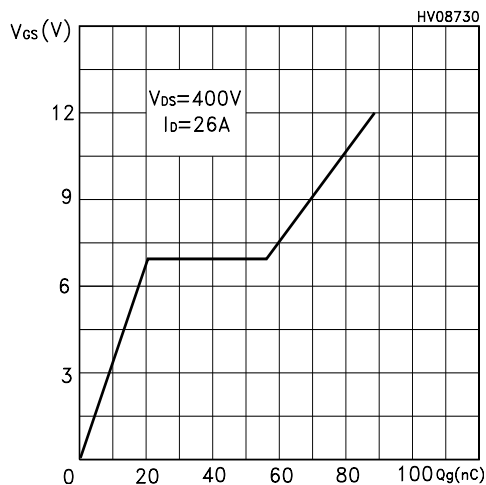


Figure 10: Normalized Gate Threshold Voltage vs Temperature

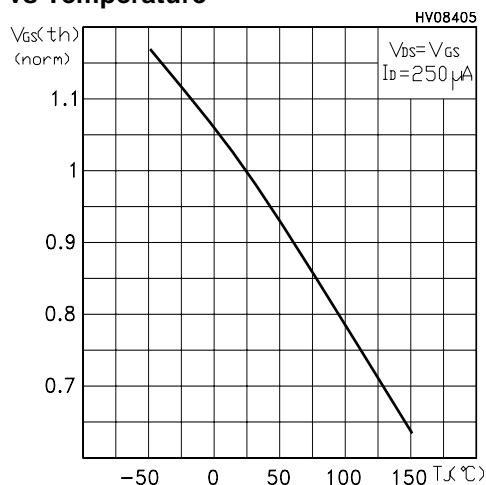


Figure 11: Dource-Drain Diode Forward Characteristics

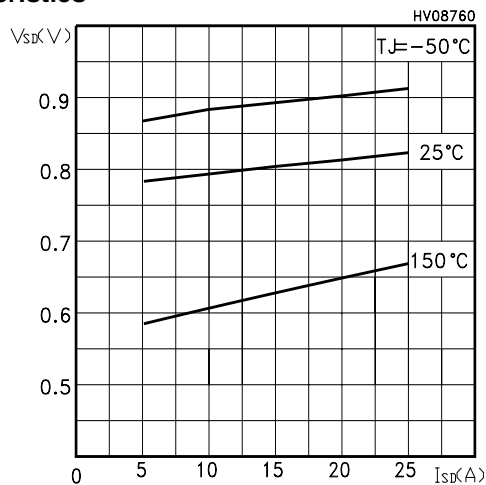


Figure 12: Capacitance Variations

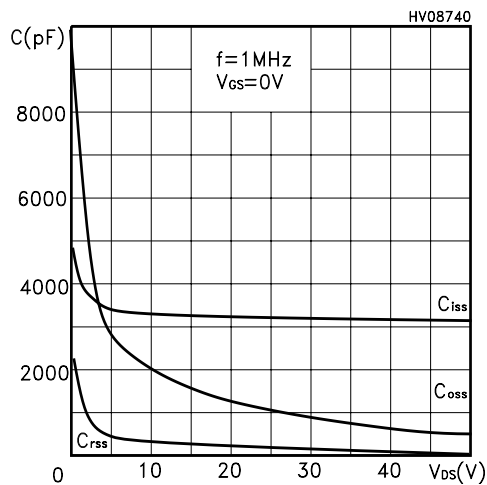


Figure 13: Normalized On Resistance vs Temperature

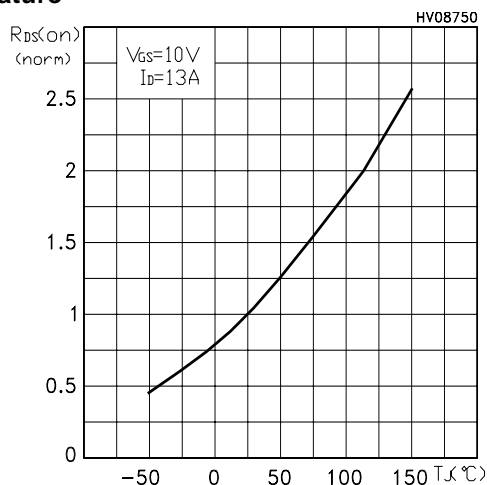


Figure 14: Unclamped Inductive Load Test Circuit

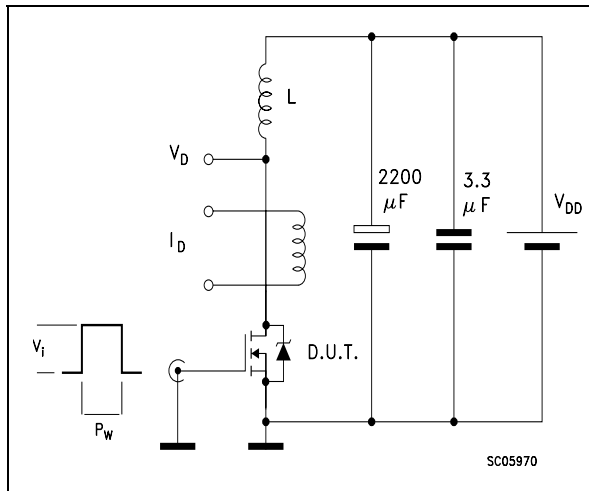


Figure 15: Switching Times Test Circuit For Resistive Load

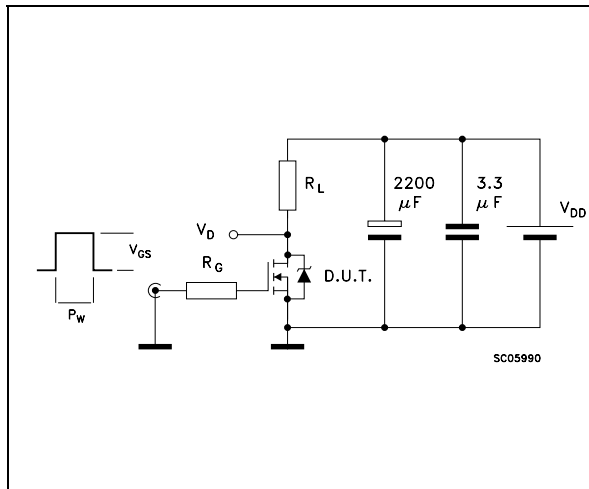


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

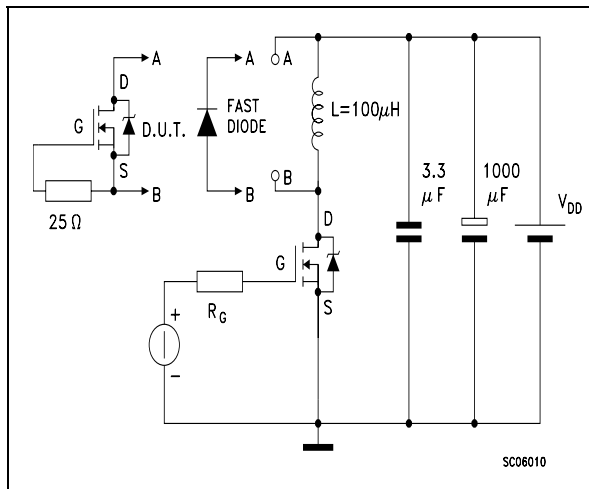


Figure 17: Unclamped Inductive Waferform

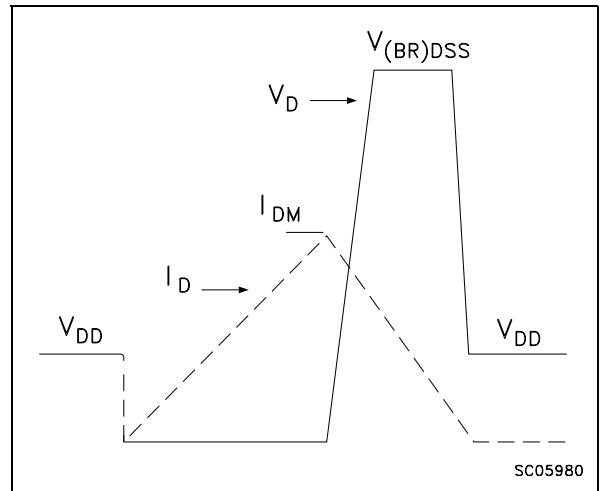
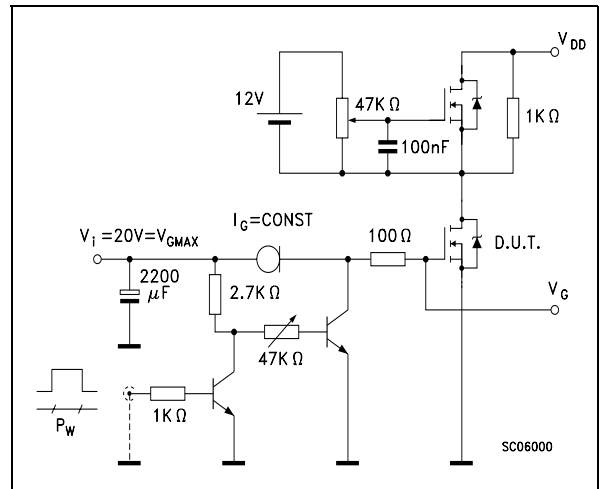


Figure 18: Gate Charge Test Circuit



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

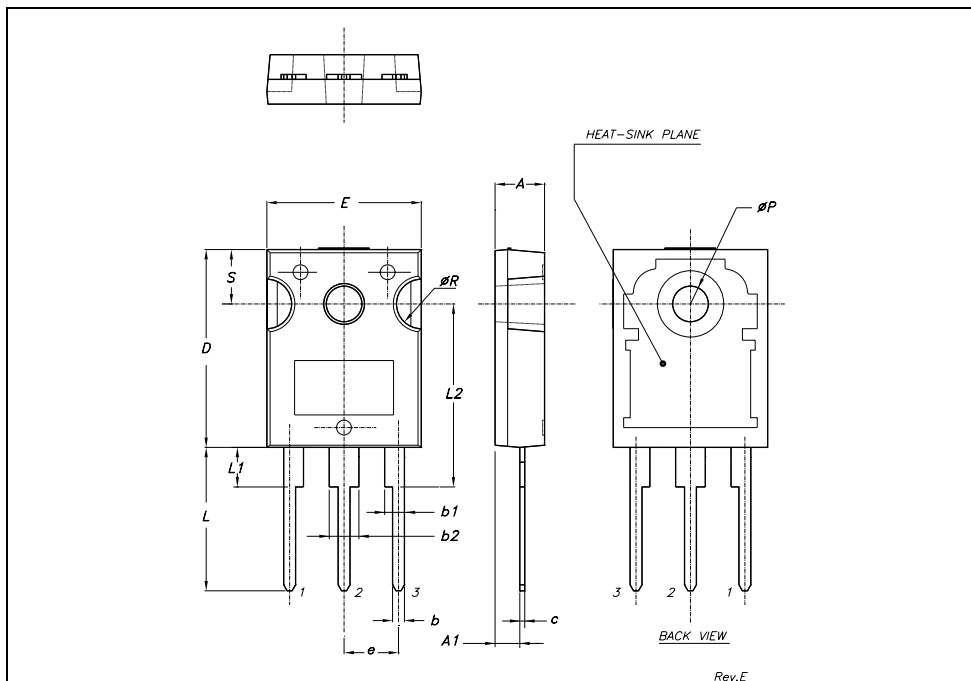


Table 10: Revision History

Date	Revision	Description of Changes
24-June-2004	9	New Stylesheet.

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