

### STS14N3LLH5

## N-channel 30 V, 0.005 Ω 14 A - SO-8 STripFET™ V Power MOSFET

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS14N3LLH5	30 V	<0.006 Ω	14 A <sup>(1)</sup>

- 1. The value is rated according  $R_{thj-pcb}$
- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



■ Switching applications



This product utilizes the 5<sup>th</sup> generation of design rules of ST's proprietary STripFET<sup>TM</sup> technology. The lowest available  $R_{DS(on)}^*Q_g$ , in SO-8 package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

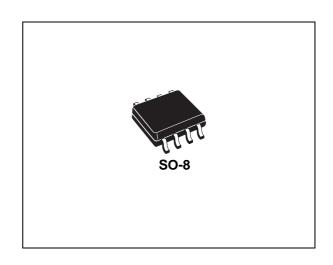


Figure 1. Internal schematic diagram

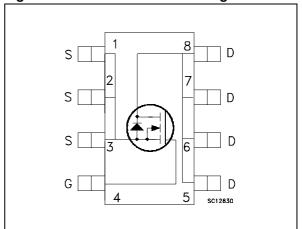


Table 1. Device summary

Order code	Marking	Package	Packaging
STS14N3LLH5	14D3L	SO-8	Tape and reel

Contents STS14N3LLH5

## **Contents**

1	Electrical ratings
2	Electrical characteristics
	2.1 Electrical characteristics (curves)
3	Test circuit
4	Package mechanical data
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STS14N3LLH5 Electrical ratings

## 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage (V <sub>GS</sub> = 0)	30	V
V <sub>GS</sub>	Gate-source voltage	± 22	٧
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	14	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> =100 °C	8.75	Α
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	56	Α
P <sub>TOT</sub> (2)	Total dissipation at T <sub>C</sub> = 25 °C	2.7	W
	Derating factor	0.02	W/°C
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150	°C

<sup>1.</sup> The value is rated according  $R_{\mbox{\scriptsize thj-pcb}}$ 

Table 3. Thermal resistance

	Symbol	Parameter	Value	Unit
ſ	R <sub>thj-pcb</sub> (1)	Thermal resistance junction-ambient	47	°C/W

<sup>1.</sup> When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I <sub>AV</sub>	Not-repetitive avalanche current, (pulse width limited by Tj Max)	8.5	Α
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AV}$ , $V_{DD} = 24$ V)	180	mJ

<sup>2.</sup> Pulse width limited by safe operating area

Electrical characteristics STS14N3LLH5

## 2 Electrical characteristics

( $T_{CASE}$ =25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = max rating, V <sub>DS</sub> =max rating @ 125 °C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±22 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			V
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS}$ = 10 V, $I_{D}$ = 7 A $V_{GS}$ = 4.5 V, $I_{D}$ = 7 A		0.005 0.0062	0.006 0.0077	$\Omega$

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V, f=1 MHz,}$ $V_{GS} = 0$		1500 295 39		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ =15 V, $I_{D}$ = 14 A $V_{GS}$ = 4.5 V (see Figure 14)		12 4 4.7		nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ =15 V, $I_{D}$ = 7 A, $R_{G}$ =4.7 $\Omega$ , $V_{GS}$ =10 V (see Figure 13)		9.3 14.5 22.7 4.5		ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current				14	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)				56	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 14 A, V <sub>GS</sub> =0			1.1	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 14 \text{ A},$ $di/dt = 100 \text{ A/}\mu\text{s},$ $V_{DD} = 25 \text{ V}, \text{ Tj} = 150 ^{\circ}\text{C}$		25 17.5 1.4		ns nC A

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300µs, duty cycle 1.5%

Electrical characteristics STS14N3LLH5

#### 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

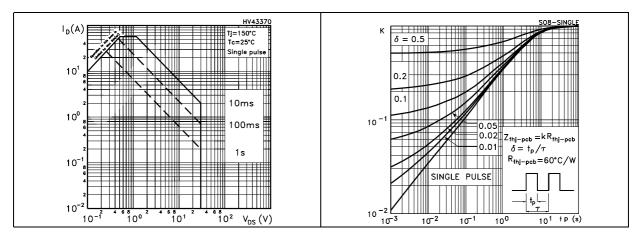


Figure 4. Output characteristics

Figure 5. Transfer characteristics

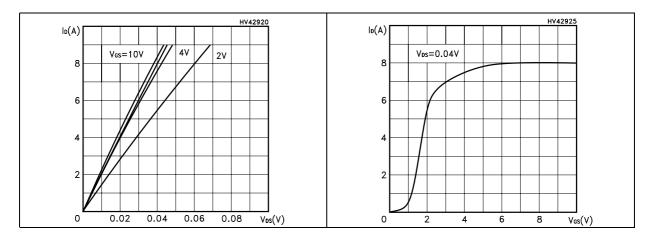
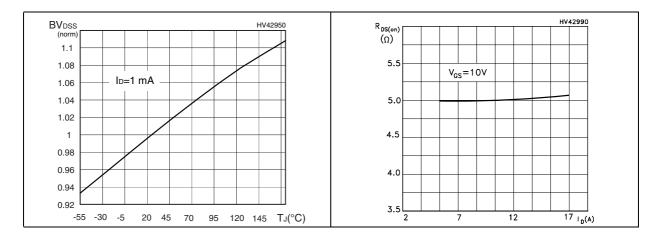


Figure 6. Normalized B<sub>VDSS</sub> vs temperature

Figure 7. Static drain-source on resistance



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C(pF)

HV42930 HV42940 C(pF) Vgs(V) f=1MHz 12 Vgs=0 2000 ID=14 A 10 Ciss 1500 8 6 1000 4 500 Coss Crss 2 0 5 0 10 15 20 Qg(nC)

Gate charge vs gate-source voltage Figure 9. **Capacitance variations** Figure 8.

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

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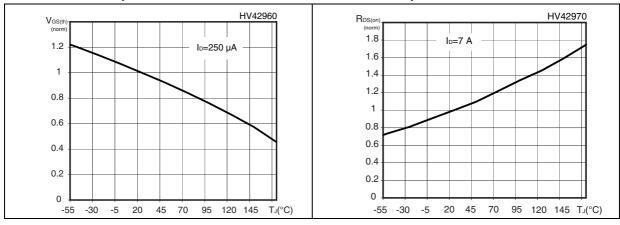
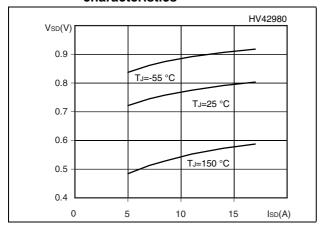


Figure 12. Source-drain diode forward characteristics



Test circuit STS14N3LLH5

#### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

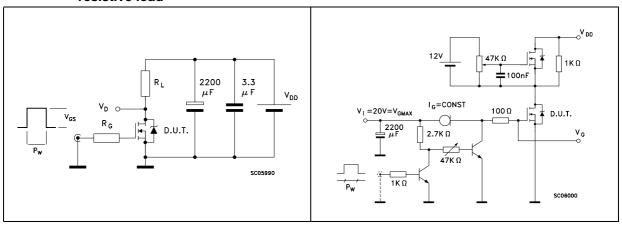


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

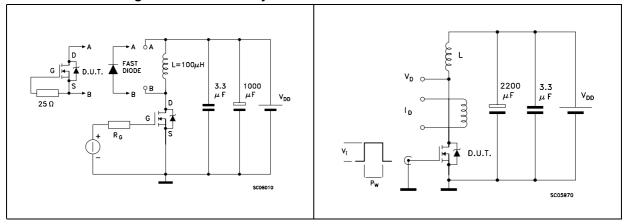
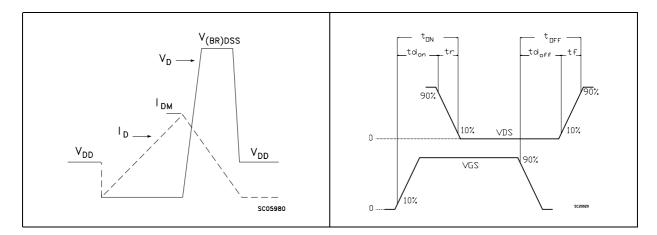


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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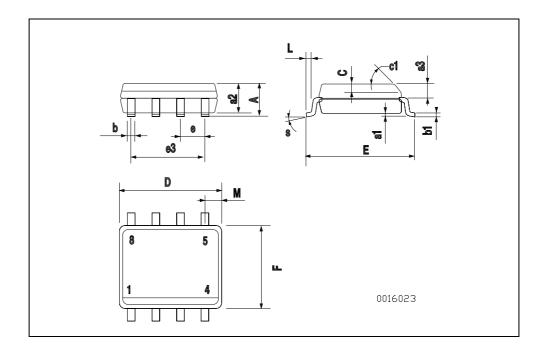
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>

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SO-8 MECHANICAL DA
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DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45 (	(typ.)		
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8 (n	nax.)	•	•



STS14N3LLH5 Revision history

# 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Nov-2007	1	First release
15-Apr-2008	2	<ul> <li>Updated Figure 1: Internal schematic diagram</li> <li>Document status promoted from preliminary data to datasheet.</li> </ul>
23-Sep-2008	3	V <sub>GS</sub> value has been changed on <i>Table 2</i> and <i>Table 5</i>

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